Triac Control Using the COP400 Microcontroller Family

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1.0 Triac Control

The COP400 single-chip controller family members provide computational ability and speed which is more than adequate to intelligently manage power control. These controllers provide digital control while low cost and short turn-around enhance COPSTM desirability. The COPS controllers are capable of 4 μs cycle times which can provide more than adequate computational ability when controlling 60 Hz line voltage. Input and output options available on the COPS devices can contour the device to apply in many electrical situations. A more detailed description of COPS qualifications is available in the COP400 data sheets.

The COPS controller family may be utilized to manage power in many ways. This paper is devoted to the investigation of low cost triac interfaces with the COP400 family microcontroller and software techniques for power control applications.

1.1 BASIC TRIAC OPERATION

A triac is basically a bidirectional switch which can be used to control AC power. In the high-impedance state, the triac blocks the principal voltage across the main terminals. By pulsing the gate or applying a steady state gate signal, the triac may be triggered into a low impedance state where conduction across the main terminals will occur. The gate signal polarity need not follow the main terminal polarity; however, this does affect the gate current requirements. Gate current requirements vary depending on the direction of the main terminal current and the gate current. The four trigger modes are illustrated in Figure 1.

The breakover voltage ($V_{BO}$) is specified with the gate current ($I_{GT}$) equal to zero. By increasing the gate current supplied to the triac, $V_{BO}$ can be reduced to cause the triac to go into the conduction or on state. Once the triac has entered the on state the gate signal need not be present to sustain conduction. The triac will turn itself off when the main terminal current falls below the minimum holding current required to sustain conduction ($I_{th}$).

A typical current and voltage characteristic curve is given in Figure 2. As can be seen, when the gate voltage and the main terminal 2 (MT2) voltages are positive with respect to MT1 the triac will operate in quadrant 1. In this case the trigger circuit sources current to the triac ($I_{GT}$) equal to zero. By increasing the gate current supplied to the triac, $V_{BO}$ can be reduced to cause the triac to go into the conduction or on state. Once the triac has entered the on state the gate signal need not be present to sustain conduction. The triac will turn itself off when the main terminal current falls below the minimum holding current required to sustain conduction ($I_{th}$).

Digital logic circuits, without large buffers, may not have the drive capabilities to efficiently turn on a triac. To insure proper operation in all firing situations, external trigger circuitry might become necessary. Also, to prevent noise from disturbing the logic levels, AC/DC isolation or coupling techniques must be utilized. Sensitive gate triacs which require minimal gate input signal and provide a limited amount of main terminal current may be driven directly. This paper will focus on 120VAC applications of power control.

1.3 ZERO VOLTAGE DETECTION

In many applications it is advantageous to switch power at the AC line zero voltage crossing. In doing this, the device being controlled is not subjected to inherent AC transients. By utilizing this technique, greater dependability can be obtained from the switching device and the device being switched. It is also sometimes desirable to reference an event on a cyclic basis corresponding to the AC line frequency. Depending on the load characteristics, switching times need to be chosen carefully to insure optimal performance. Triac controlled AC switching referenced to the AC 60 Hz line frequency enables precise control over the conduction angle at which the triac is fired. This enables the COPS device to control the power output by increasing or decreasing the conduction angle in each half cycle.

A wide variety of zero voltage detection circuits are available in various levels of sophistication. COPS devices, in most cases, can compensate for noisy or semi-accurate ZVD circuits. Some software considerations are presented in the software section and are commented upon. The minimal detection circuit is shown in Figure 8.

1.4 DIRECT COUPLE

Isolation associated problems can be overcome by means of direct AC coupling. One such method is illustrated in Figure 3. This circuit incorporates a half-wave rectifier in conjunction with a filter capacitor to provide the logic power supply. The positive half-cycle is allowed to drop across the zener diode and be filtered by the capacitor. This creates a low cost line interface; however, only a limited supply current is available. In order to control the current capabilities of this circuit the series resistor must be modified. However, as more current is required, the power that must be dissipated in the series resistor increases. This increases the power dissipation requirements of the series resistor and the system cost. For applications which require large current sources an alternative method is advisable. In order to assure consistent operation, power supply ripple must be mini-
mized. COPS devices can be operated over a relatively wide power supply range. However, excessive ripple may cause an inadvertent reset operation of the device.

1.5 PULSE TRANSFORMER INTERFACE

Digital logic control of triacs is easily accomplished by triggering through pulse transformers or optical coupling. The energy step-up gained by using a pulse transformer should provide a more than adequate gate trigger signal. This complies with manufacturers’ suggested gate signal requirements. Pulse transformers also provide AC/DC isolation necessary in control logic interfaces. Minimal circuit interface to the pulse transformer is required as shown in Figure 4. Optical coupling circuits provide isolation, and in some cases adequate gate drive capabilities.

1.6 FALSE TURN-ON

When switching an inductive load, voltage spikes may be generated across the main terminals of the triac which have the potential of a non-gated turn-on of the triac. This creates the undesirable situation of limited control of the system. In a system with an inductive load the voltage leads the current by a phase shift corresponding to the amount of inductance in the motor. As the current passes near zero, the voltage is at a non-zero value, offset due to the phase shift. When the principal current through the triac pellet decreases to a value not capable of sustaining conduction the triac will turn off. At this point in time the voltage across the terminals will instantaneously attain a value corresponding to the phase shift caused by the inductive load. The rapid decay of current in the inductor causes an L dI/dT voltage applied across the terminals of the triac. Should this voltage exceed the blocking voltage specified for the triac, a false turn-on will occur.

In order to avoid false turn-on, a snubber network must be added across the terminals to absorb the excess energy generated by this situation. A common form of this network is a simple RC in series across the terminals. In order to select the values of the network it is necessary to determine the peak voltage allowable in the system and the maximum dV/dT stress the triac can withstand. One approach to obtaining the optimal values for R_S and C_S is to model the effective circuit and solve for the triac voltage. The snubber in conjunction with the load can now be modeled as an RLC network. Due to the two storage elements (L motor, C snubber) a second order differential equation is generated. Rather than approach this problem from a computer standpoint it becomes much easier to obtain design curves generated for rapid solution of this problem. These design curves are available in many triac publications. (For instance, see RCA application note AN 4745.)

2.0 Software Techniques

2.1 ZERO VOLTAGE DETECTION

In order to intelligently control triacs on a cyclic basis, an accurate time base must be defined. This may be in the form of an AC, 60 Hz sync pulse generated by a zero voltage detection circuit or a simple real time clock. The COP400 series microcontrollers are suited to accommodate either of these time base schemes while accomplishing auxiliary tasks.

Zero voltage detection is the most useful scheme in AC power control because it affords a real time clock base as well as a reference point in the AC waveform. With this information it is possible to minimize RFI by initiating power-on operations near the AC line voltage zero crossing. It is also possible to fire the triac for only a portion of the cycle, thus utilizing conduction angle manipulation. This is useful in both motor control and light intensity control.

Sophisticated zero voltage detection circuits which are capable of discriminating against noise and switch precisely at zero crossing are not necessary when used in conjunction with a COPS device. COPS software is capable of compensating for noisy or semi-accurate zero voltage detection circuits. This can be accomplished by introducing delays and debounce techniques in the software routines. With a given reference point in the AC waveform it now becomes easy...
to divide the waveform to efficiently allocate processing time. These techniques are illustrated in the code listing at the end of this paper.

2.2 PROCESSING TIME ALLOCATIONS

Half Cycle Approach

In order to accomplish more than triac timing, dead delay time must be turned into computation time. It appears that the controller is occupied totally by time delays, which leaves a very limited amount of additional control capability. There are, however, many ways to accomplish auxiliary tasks simultaneously.

On each half cycle an initial delay is incorporated to space into the cycle. This dead time may be put to use and very little voltage to the load is sacrificed. For example, if the load is switched on at \( \pi/4 \) RAD, the maximum applied RMS voltage to the load is 114 V RMS (assuming \( V_{\text{SUPPLY}} = 120 \text{ V RMS} \)). This is illustrated in the figure below.

Full Cycle Approach

The methods of half cycle and full cycle triggering are very similar in procedure. The main difference is that all timing is referenced from only one (of the two) zero voltage detection transition in each full AC cycle. For most all applications, when varying the conduction angle it is desirable to fire at the same conduction angle each half cycle to maintain a symmetric applied voltage. In order to accomplish this the triac may be fired twice from one reference point. When applying this technique an 8.33 ms delay must be executed to maintain the symmetric applied voltage. This approach provides the most auxiliary computation time in that the 8.33 ms delay may be turned into computational time. The basic flow for this technique is illustrated below.

If a delay of \( \pi/4 \) RAD (45 degrees) is inserted after each zero crossing detection the RMS voltage to the load can be determined in the following manner:

\[
V_{\text{LOAD}} = \sqrt{\left(\frac{120}{2}\right)^2 \frac{\pi}{\pi/4}} \sin^2 (a) \, da
\]

\[
V_{\text{LOAD}} = \sqrt{\left(\frac{120}{2}\right)^2 \frac{\pi}{\pi/4}} (1.428)
\]

\[
V_{\text{LOAD}} = 114.4 \text{ V RMS}
\]

\( \pi/4 \) RAD = 45 degrees @60 Hz \( t = 2.08 \text{ ms} \)

As can be seen the dead time on each half cycle can be 2.08 ms and the load will still see 114.4 V RMS of a V SUPPLY of 120 V RMS. If this approach is implemented the initial delay of 2.08 ms can be used as computation time. The number of instructions which can be executed when operating at 4 \( \mu \text{s} \) instruction cycle time is:

\[
\frac{2.08 \text{ ms}}{4 \mu \text{s}} = 520 \text{ instructions}
\]

(130 instructions at 16 \( \mu \text{s} \) cycle time)

FIGURE 6. Full Cycle Approach

In the above example the zero crossing pulse is debounced on the one-to-zero transition, thus marking the beginning of a full cycle. Once this transition has been detected, an ini-
The delay of \( \pi/4\) RAD is incorporated and the triac is fired. At this time exactly 8.33 ms is available until the triac need be triggered again. This will provide a symmetric voltage to the load only if the delay is 8.33 ms. During this period the number of instructions which can be executed when operating at 4 \( \mu\)s is:

\[
\frac{8.33 \text{ ms}}{4 \mu\text{s}} = 2082
\]

(520 instructions at 16 \( \mu\)s)

An alternative approach may be to take the burden from the COPS device by using peripheral devices such as static display controllers, external latches, etc.

### 2.3 STEADY STATE TRIGGERING

It is possible to trigger a triac with a steady state logic level. This is accomplished by allowing the triac gate to sink or source current during the desired on-time. When utilizing this method it becomes easier to trigger the triac and leave it on for many cycles without having to execute code to retrigger. This approach is advantageous when the triac must be fired for relatively long periods and conduction angle firing is not desired, thus more time is available to accomplish auxiliary tasks. A steady state on or off signal and external circuitry can accomplish triac firing and free the processor for other tasks. If it is desired to use a pulse transformer, an external oscillator must be gated to the triac to provide the trigger signal. A pulse train of 10 to 15 kHz is adequate to fire the triac each half cycle. This calls for external components and is relatively costly. If isolation associated problems can be tolerated or overcome (dual power supply transformers, direct AC coupling, etc.), a simple buffer may be utilized in triggering the triac. This method is illustrated in Figure 8. The National Semiconductor DS8863 display driver is capable of steady state firing of the triac. National offers many buffers capable of driving several hundred milliamps, which are suitable for driving triacs. On the market today there are many suppliers of sensitive gate triacs which may be triggered directly from a COPS device or in conjunction with a smaller external buffer.

The DS8863 display driver is capable of sinking up to 500 mA, which is adequate to drive a standard triac. In the off state the driver will not sink current. When a logic “1” is applied to the input the device will turn on. Keeping the device off (output “1”) will prevent the triac from turning on because the buffer does not have the capability of sourcing current. A series resistor limits the current from the triac gate and the diode isolates the negative spikes from the gate. Since the drive circuit will only sink current in this configuration, the triac will be operating in the I- and III- modes.
3.0 Triac Light Intensity
Control Code

The following code is not intended to be a final functional
program. In order to utilize this program, modifications must
be made to specialize the routines. This is intended to illus-
trate the method and is void of control code to command a
response such as intensity or deintensify. The control is up
to the user and full understanding of the program must be
attained before modifications can be implemented.

This program is a general purpose light intensifying routine
which may be modified to suit light dimmer applications. The
delay routines require a 4.469 \( \mu \text{s} \) cycle time which can be
attained with a 3.578 MHz crystal (CKI/16 option). This pro-
gram divides the half cycle of a 60 Hz power line into 16
levels. Intensity is varied by increasing or decreasing the
conduction angle by firing the triac at various levels. The
program will increase the conduction angle to a maximum
specified intensity in a fixed amount of time. The time re-
quired to intensity to the maximum level is dependent on the
number of fire-times per level that is specified (FINO). This
code illustrates a half cycle approach and relies on the pa-
rameters specified by the programmer in the control selec-
tion.

Zero crossings of the 60 Hz line are detected and software
debounced to initiate each half cycle; thus the triac is serv-
icd on every half cycle of the power line. A level/sublevel
approach is utilized to vary the conduction angle and pro-
vide a prolonged intensifying period. The maximum intensity
is specified by the "LEVEL" RAM location and time required
to get to that level is specified by the "FINO" RAM location.

Once a level has been specified, the remaining time in the
half cycle is then divided into sublevels. The sublevels are
increased in steps to the maximum level. The "FINO" RAM
location contains the number of times that the triac will be
fired per sublevel, thus creating the intensity time base. There
are 15 valid sublevels and up to 15 fire-times per
sublevel. Both these parameters may be increased to pro-
vide better resolution and longer intensity periods. To make
the triac de-intensity (dim) the sublevels need only to be
decremented rather than incremented. If this is done, the
conduction angle will start out at the maximum level and dim
by means of stepping down the sublevels. When modifying
this routine to incorporate more resolution or increased ver-
satility, care must be taken to account for transfer of control
instructions to and from the delay routines.

The following is a schematic diagram of the COPS interface
to 120VAC lamps. The program will intensify or de-intensify
the lamps under program control.

3.1 TRIAC LIGHT INTENSIFY ROUTINE

This program intensifies a light source by varying the con-
duction angle applied to the load. The maximum level of
intensity is stored in "LEVEL," and the time to get to that
level is specified by "FINO." Both these parameters may be
altered to suit specific applications. To cause the program
to de-intensify the light source, the sublevels must be de-
cremented rather than incremented.
TRIAC LIGHT INTENSIFY ROUTINE

; THIS PROGRAM INTENSIFIES A LIGHT SOURCE BY VARYING THE CONDUCTION ANGLE APPLIED TO THE LOAD. THE MAX LEVEL OF INTENSITY IS STORED IN 'LEVEL' AND THE TIME TO GET TO THAT LEVEL IS SPECIFIED BY 'FIND'. BOTH THESE PARAMETERS MAY BE ALTERED TO SUIT SPECIFIC APPLICATIONS. TO CAUSE THE PROGRAM TO DE-INTENSIFY THE LIGHT SOURCE, THE SUBLLEVS MUST BE DECREMENTED RATHER THAN INCORPORATED.

; INITIATION IS SPECIFIED

INT: CLRA
ADT ; DELAY INTO WAVEFORM
LBI TEMP ; USE TEMP REG
PAGE 0
X
JSRP PORT ; DO DELAY

CLRAM: LBI 3,15 ; ROUTINE TO CLEAR ALL RAM
POINT: LDD LEVEL ; POINT TO LEVEL TO INITIATE DELAY
CLR ; DELAY TO MAX LEVEL
XDS
CLR
JP CLR

XABR ; USE TEMP DIGIT TO DELAY TEMP
TAMP: LBI TEMP
LD
AISC 15 ; ARE WE AT THE LEVEL ?
JP ATLEV ; MADE IT TO THE LEVEL
X ; NO
JSRP DEC ; DO SERIES OF .5MS TO GET THERE

ATLEV: LDD SUBLEV ; AT MAX FIRE LEVEL
XAD TEMP ; INIT FOR SUBLEVEL DELAY
JK: LBI TEMP
LD
LEVEL ; SPECIFY MAX LEVEL
STIL 7
JSRP OUT ; COPY TO TEMP1
JP TRE ; NO DO DELAY

TRE: X
JSRP SPDL ; VARIABLE DELAY
JP
JK

THIS SECTION INITIATES CONTROL ON POWER UP OR RESET AND SYNCHRONIZES THE COPS DEVICE TO THE 60 HZ AC LINE.

BEGG: OGI 15 ; OUTPUT 15 TO G PORTS TO PULL UP ZERO CROSSER INPUT
LBI LEVEL ; AT SUB LEVEL ?
STI 7
JSRP OUT ; COPY TO TEMP1
JP TRE ; NO DO DELAY

TRE: X
JSRP SPDL ; VARIABLE DELAY
JP
JK

THIS SECTION PROVIDES THE DEBOUNCE FOR THE ZERO VOLTAGE DETECTION INPUT AND COMPENSATES FOR THE OFFSET OF THE DETECTION CIRCUIT.

Hi: SKGBZ 0 ; TEST GO FOR ZERO CROSS
JP Hi ; HIGH LEVEL

Hi ; READY NOW
TRE: X
JP BEG ; WAIT TILL G IS 1
JSRP SPD1 ; VARIOUS DELAYS

MAXLEV: JMP FIRE ; NO KEEP Firing AT THAT LEVEL
LBI SUBLEV ; YES INC SUBLEVEL
CLRA
AISC 14 ; IS MAX SUBLEVEL REACHED
SKE
JP THERE ; NO INC SUBLEVEL
JP MAXLEV ; YES FIRE IT

MAXLEV: JMP FIRE ; NO KEEP Firing AT THAT LEVEL
LBI SUBLEV ; YES INC SUBLEVEL
CLRA
AISC 14 ; IS MAX SUBLEVEL REACHED
SKE
JP THERE ; NO INC SUBLEVEL
JP MAXLEV ; YES FIRE IT

; Did a little delay, is it still on?

DID A LITTLE DELAY, IS IT STILL 0
THERE: JSRP INC ; GO TO NEXT SUBLEVEL

DO: JMP INT ; VALID TRANSITION, SERVICE
TRIAC
FORM

LO: SKGBZ 0 ; DEBOUNCE IN 0 TO 1
JP LO ; NO WAIT HERE FOR A BIT

LO ; WELL, DO WE HAVE A CLEAN TRANSITION
JP DELL ; YES, GO TO MAIN ROUTINE
FORM

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