EE 330
Integrated Electronics
Spring 2015
COURSE INFORMATION

Room: Lecture - 1312 Hoover
Labs - 2046 Coover

Time: Lecture - MWF 9:00-9:50
Laboratory - Sec A Tues 8:00-10:50 TA: Tyler
- Sec C Thurs 3:10-6:00 TA: Chin-Wen
- Sec D Wed 3:10-6:00 TA: Chin-Wen

Randy Geiger
2133 Coover
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Laboratory Instructors:
Chin-Wen Chen <chinwen@iastate.edu>
Tyler Bohlke <tbohlke@iastate.edu>

Course Description:
Semiconductor technology for integrated circuits. Modeling of integrated devices including diodes, BJTs, and MOSFETs. Physical layout. Circuit simulation. Digital building blocks and digital circuit synthesis. Analysis and design of analog building blocks. Laboratory exercises and design projects with CAD tools and standard cells.

. **Course Web Site:** http://class.ee.iastate.edu/ee330
Homework assignments, lecture notes, laboratory assignments, and other course support materials will be posted on this WEB site. Students will be expected to periodically check the WEB site for information about the course.

Required Texts:

CMOS VLSI Design – A Circuits and Systems Perspective, Fourth Edition
by N. Weste and D. Harris, Addison Wesley, 2011

Reference Texts:

Fundamentals of Microelectronics
by B. Razavi, Wiley, 2008

Microelectronic Circuits (6th Edition)
by Sedra and Smith, Oxford, 2009

CMOS Digital Integrated Circuits Analysis & Design (4th Edition)
by Kang, Leblebici, and Kim, McGraw Hill, 2014

Microelectronic Circuit Design (4th Edition)
by Richard Jaeger and Travis Blalock, McGraw Hill, 2010

Digital Integrated Circuits (2nd Edition)
by Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Prentice Hall, 2003

CMOS Circuit Design, Layout, and Simulation (3rd Edition)
Jacob Baker, Wiley-IEEE Press, 2010.

Analog Integrated Circuit Design (2nd Edition)
by T. Carusone, D. Johns and K. Martin, Wiley, 2011

Principles of CMOS VLSI Design
by N. Weste and K. Eshraghian, Addison Wesley, 1992

VLSI Design Techniques for Analog and Digital Circuits
by Geiger, Allen and Strader, McGraw Hill, 1990

CMOS Analog Circuit Design (3rd Edition)
by Allen and Holberg, Oxford, 2011.

The Art of Analog Layout (2nd Edition)
by Alan Hastings, Prentice Hall, 2005

CMOS IC Layout
by Dan Cline, Newnes, 1999.

Design of Analog Integrated Circuits
by Laker and Sansen, McGraw Hill, 1994

Analysis and Design of Analog Integrated Circuits-Fifth Edition
Gray,Hurst, Lewis and Meyer, Wiley, 2009

Grading: Points will be allocated for several different parts of the course. A letter grade will be assigned based upon the total points accumulated. The points allocated for different parts of the course are as listed below:

3 Exams	100 pts each
1 Final	100 pts
Homework	100 pts total
Quizzes/Attendance	100 pts total
Lab and Lab Reports	100 pts total

Design Project 100 pts

Laboratory:

There will be weekly laboratory experiments. An IC design project will be conducted in which student designs will be eligible for fabrication through the MOSIS program. A separate laboratory handout will be provided that will discuss laboratory policy and procedures. All laboratory experiments must be completed to be eligible for receiving a passing grade in this course per the "Attendance and Equal Access Policy" described below.

You will be using state of the art equipment and software in the laboratory. Please take the initiative to become familiar with how this equipment and software operates. Operators manuals for all of the test equipment which discuss basic operation and the performance specifications are available on line.

Homework:

Homework assignments are due at the beginning of the class period on the designated due dates. Unless announced to the contrary, late homework will be accepted, without penalty, up until 5:00 p.m. on the due date in Room 2133 Coover. When homework is due near an exam date, the late homework option may not be available so solutions can be posted earlier.

Attendance and Equal Access Policy:

Participation in all class functions and provisions for special circumstances will be in accord with ISU policy

Attendance of any classes or laboratories, turning in of homework, or taking any exams or quizzes is optional however grades will be assigned in accord with described grading policy. No credit will be given for any components of the course without valid excuse if students choose to not be present or not to contribute. Successful demonstration of ALL laboratory milestones and submission of complete laboratory reports for ALL laboratory experiments to TA by deadline established by laboratory instructor is, however, required to be eligible to receive a passing grade in this course.

Laboratory Safety:

In the laboratory, you will be using electronic equipment that can cause serious harm or injuries, or even death, if inappropriately used. Fortunately, if this equipment is used as intended by the manufacturers and if good safety procedures are followed, the risks associated with using this equipment will be very small.

Your safety and the safety of fellow students and anyone else that may be in the laboratory is of utmost importance. Laboratory safety guidelines are posted in the laboratories you will be using. Please be aware of and conform to these guidelines. Your TA will go through a laboratory safety procedure and ask you to certify that you have participated in the laboratory safety training.

Additional Comments

I encourage you to take advantage of the e-mail system on campus to communicate about any issues that arise in the course. I typically check my e-mail several times a day. Please try to include “EE 330" in the subject field of any e-mail message that you send so that they stand out from what is often large volumes of routine e-mail messages.