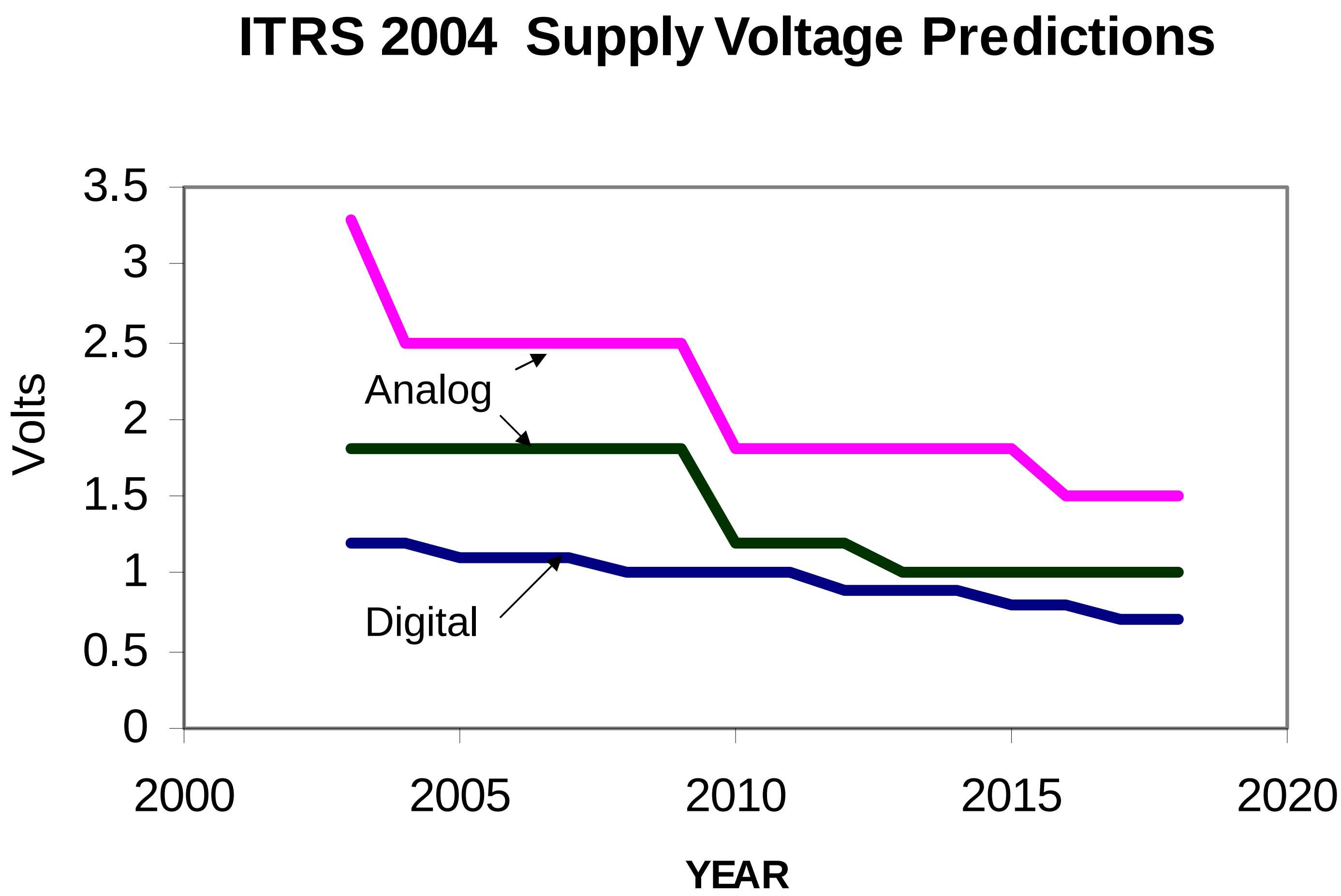
EE 434
Lecture 2

Basic Concepts

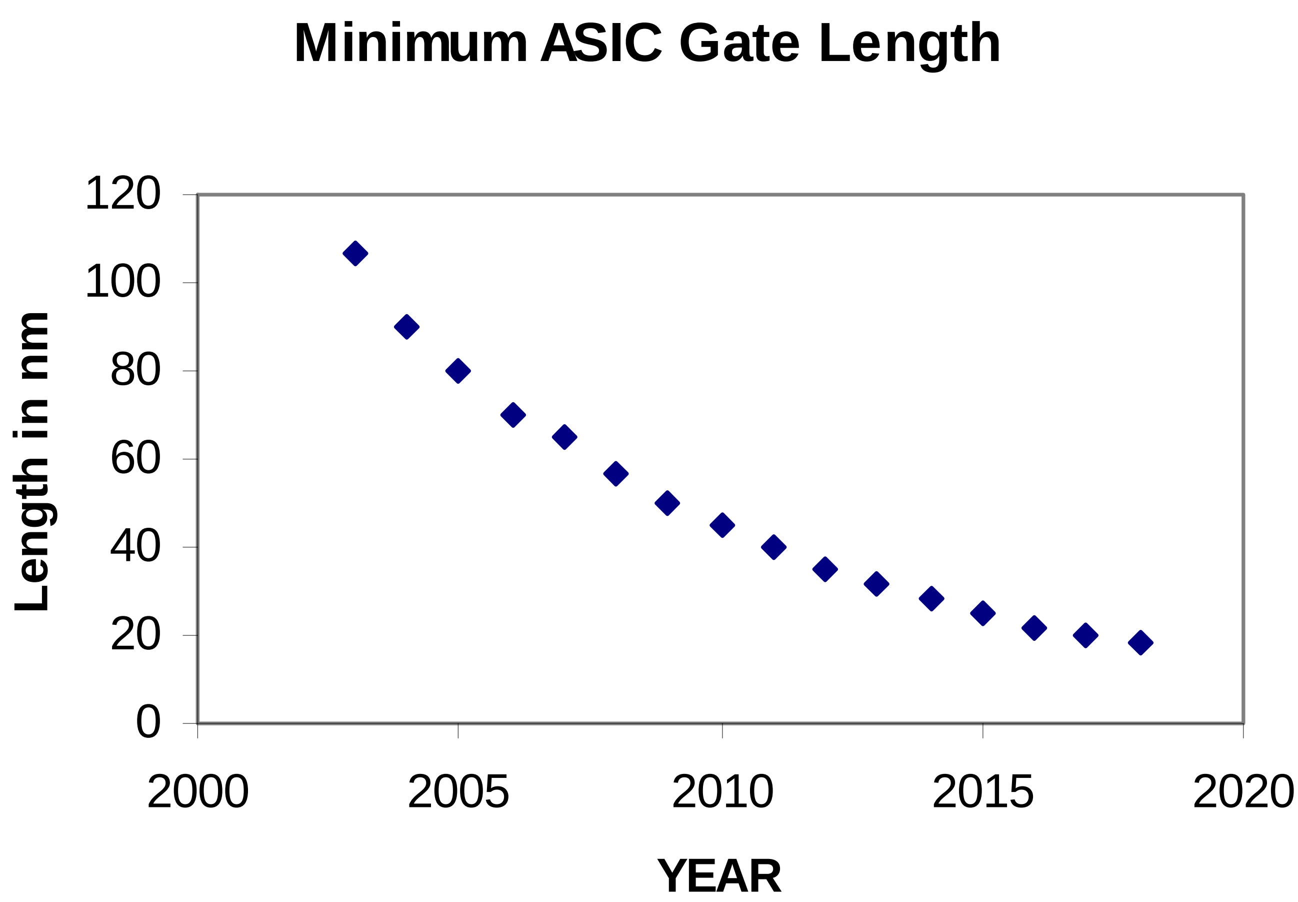
Review from Last Time

- Semiconductor Industry is One of the Largest Sectors in the World Economy and Growing
- All Initiatives Driven by Economic Opportunities and Limitations
- Rapidly Growing Device Count and Rapidly Shrinking Feature Sizes (Moore's Law?)
- Designers Must Handle Incredible Complexity Yet Work in Large Teams and Make Almost No Mistakes
- Understand the Big Picture and Solve the Right Problem

ITRS Technology Predictions



ITRS Technology Predictions

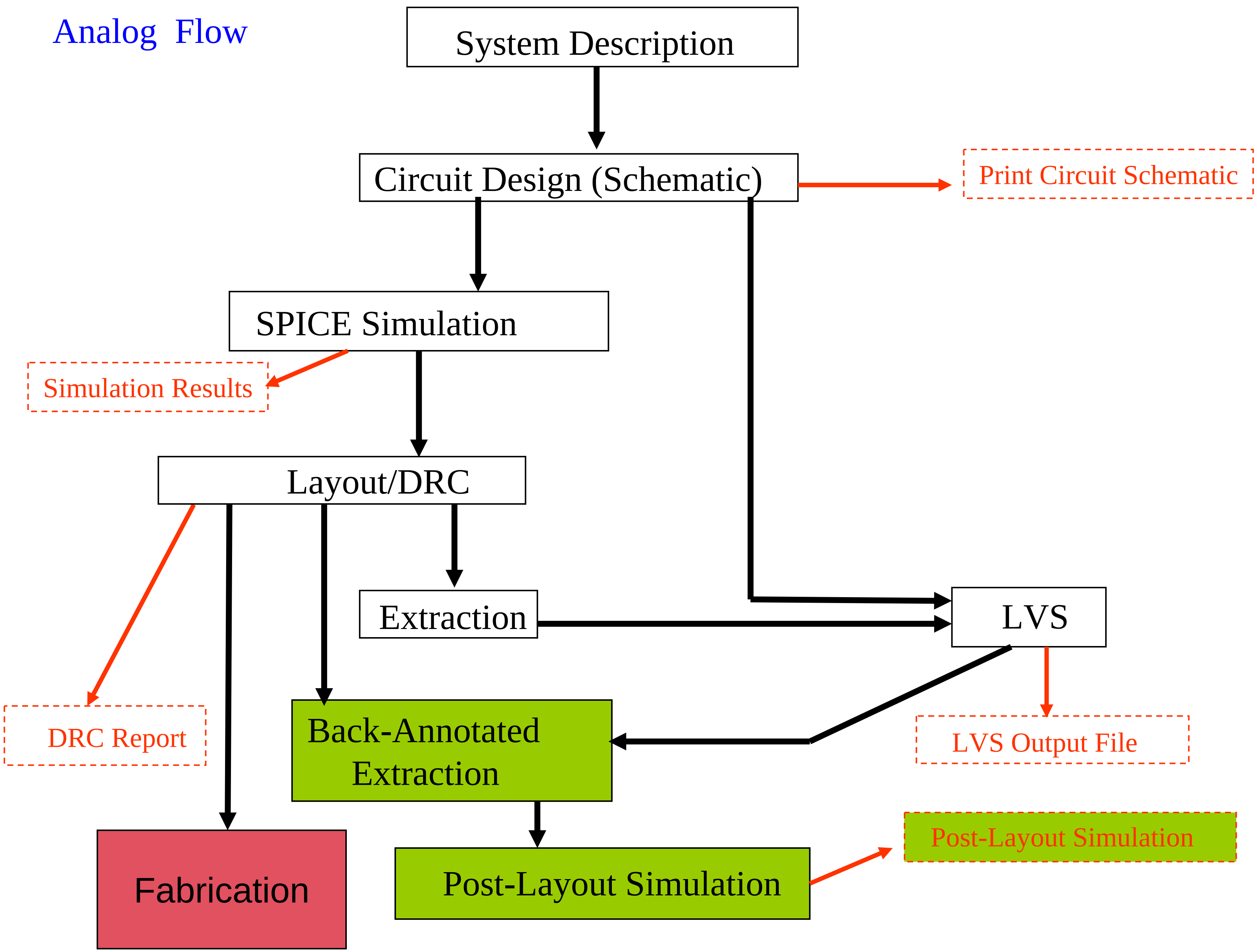


CAD Environment for Integrated Circuit Design

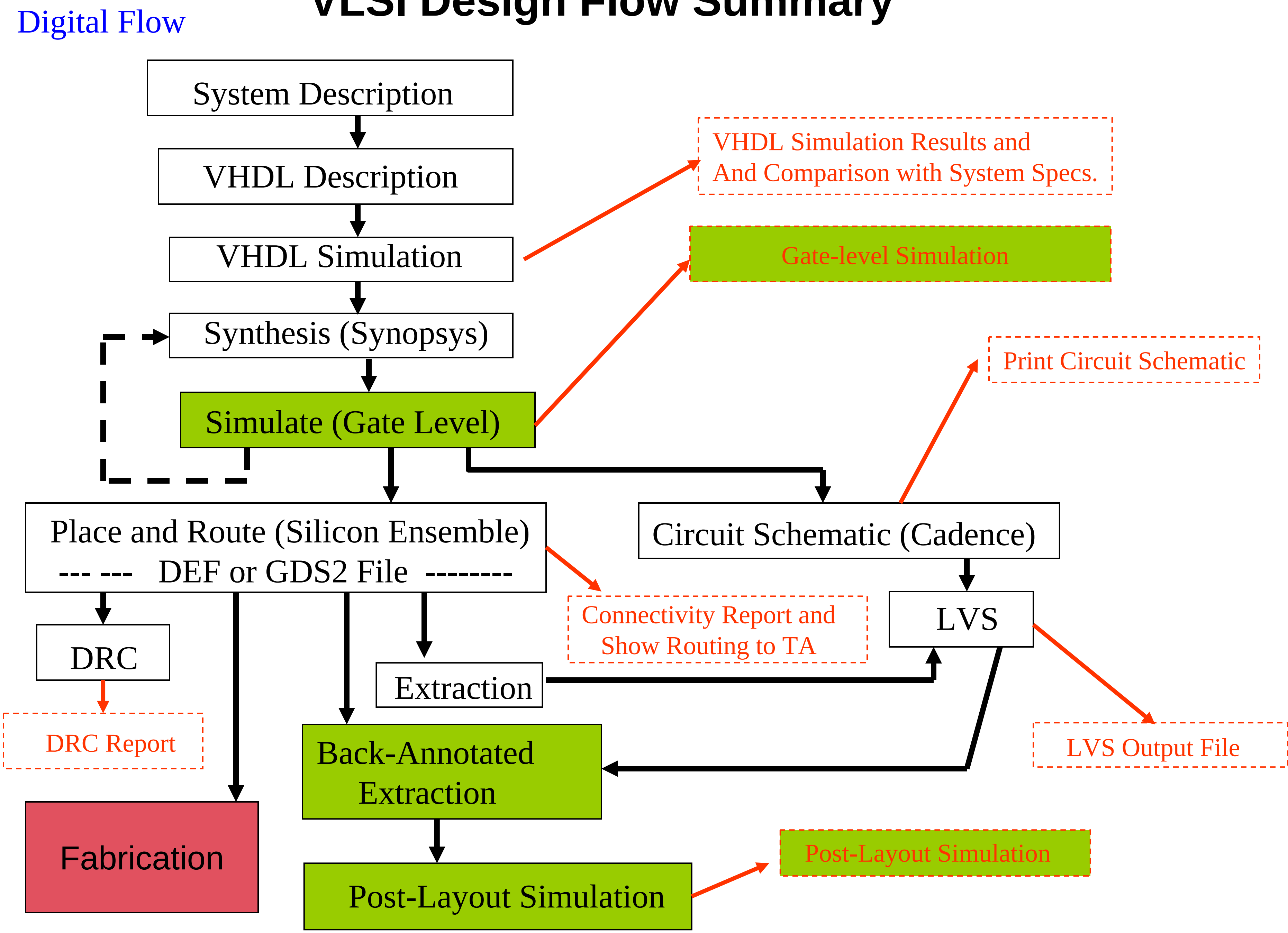
- Typical Tool Flow
  - (See Chapter 8 of Text)

- Laboratory Experiments in Course

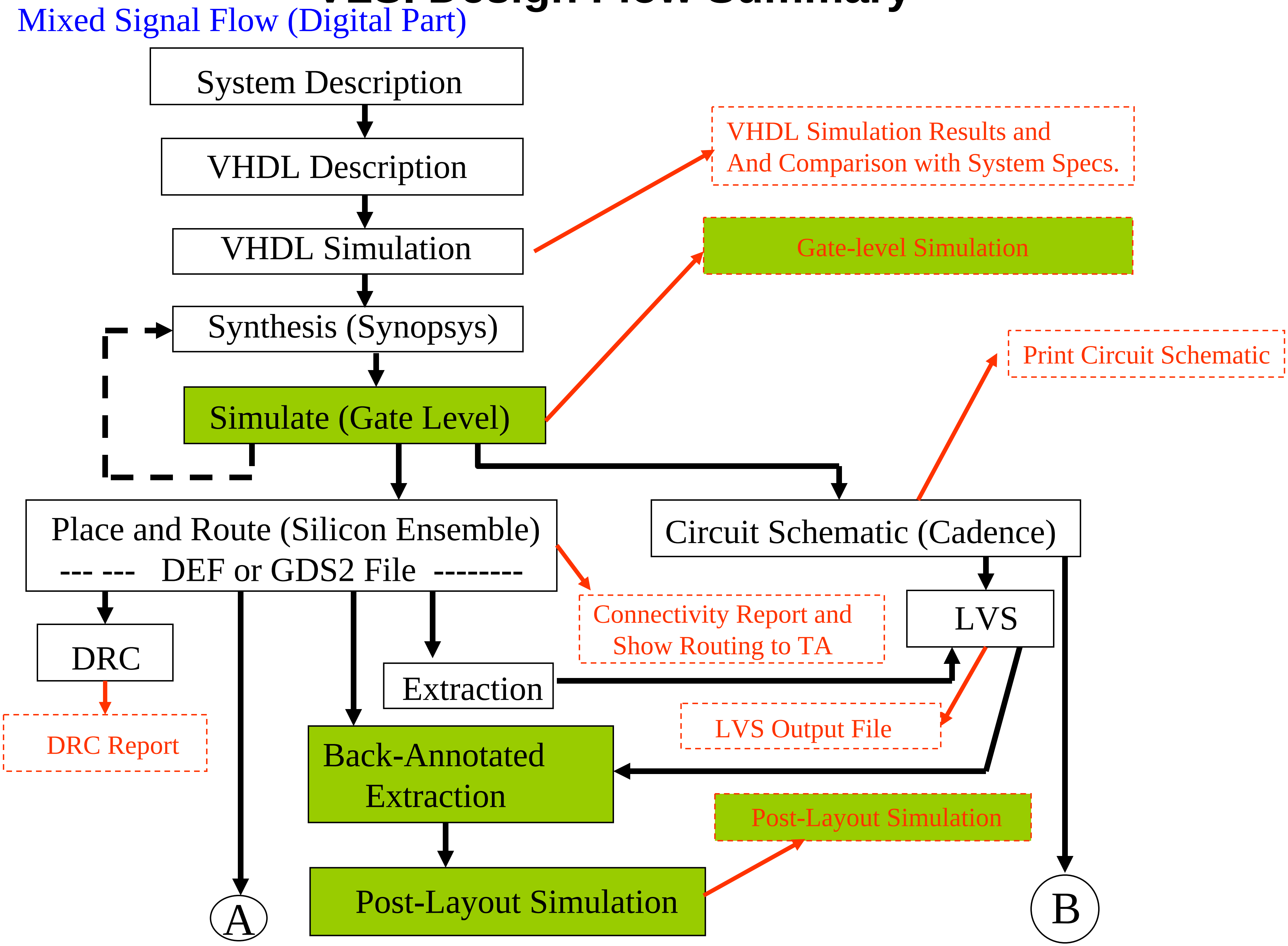
VLSI Design Flow Summary



VLSI Design Flow Summary

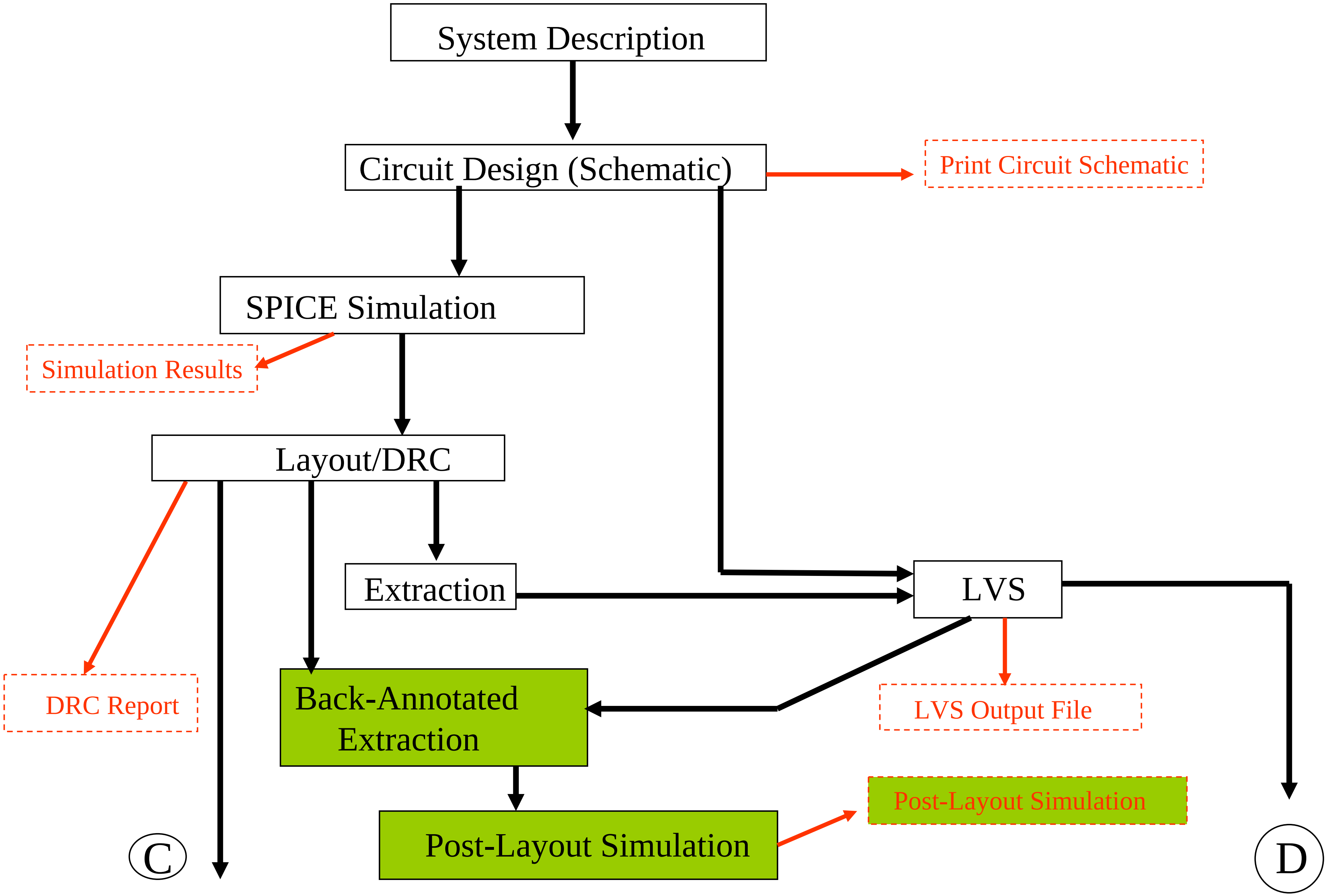


VLSI Design Flow Summary

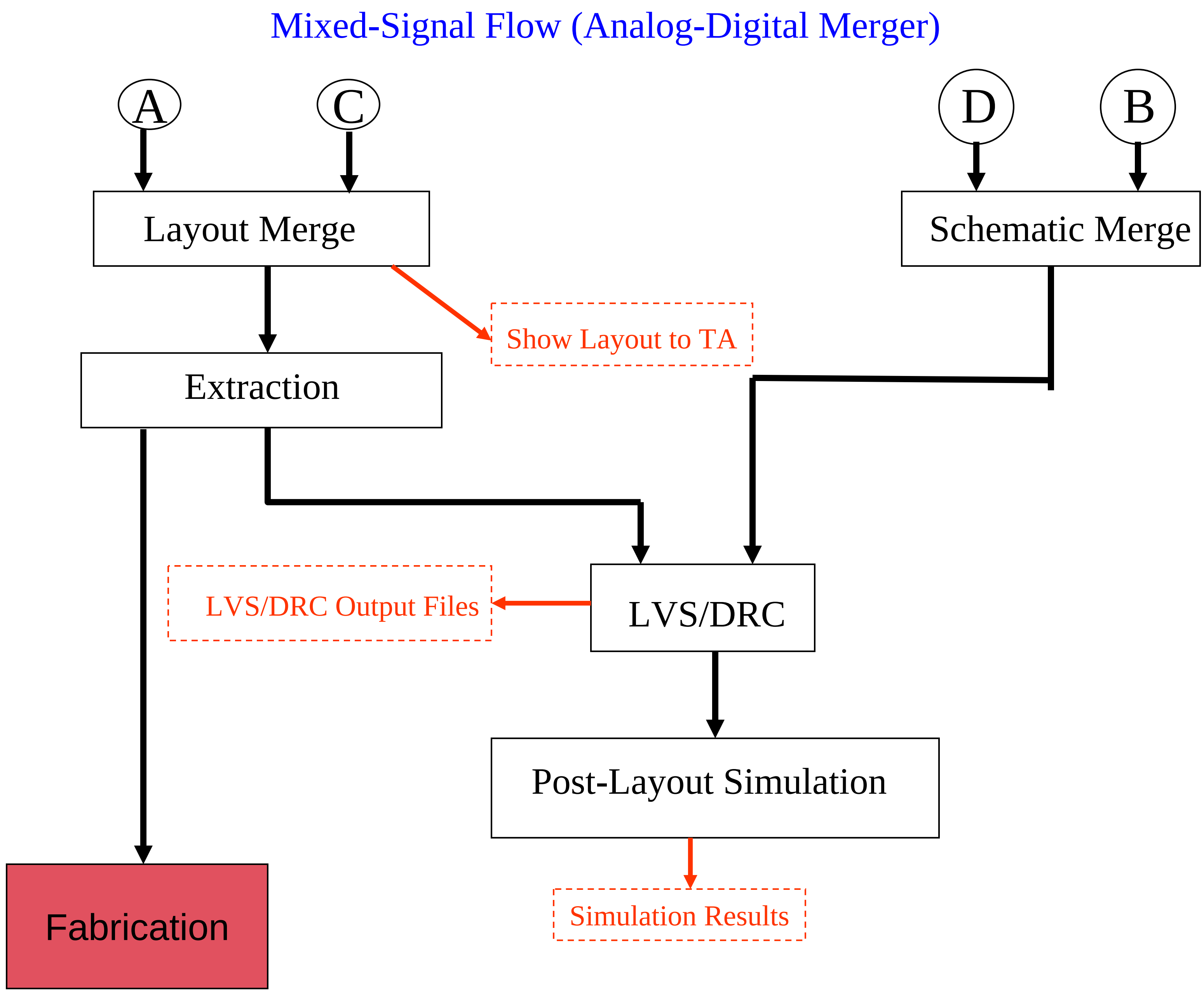


VLSI Design Flow Summary

Mixed-Signal Flow (Analog Part)



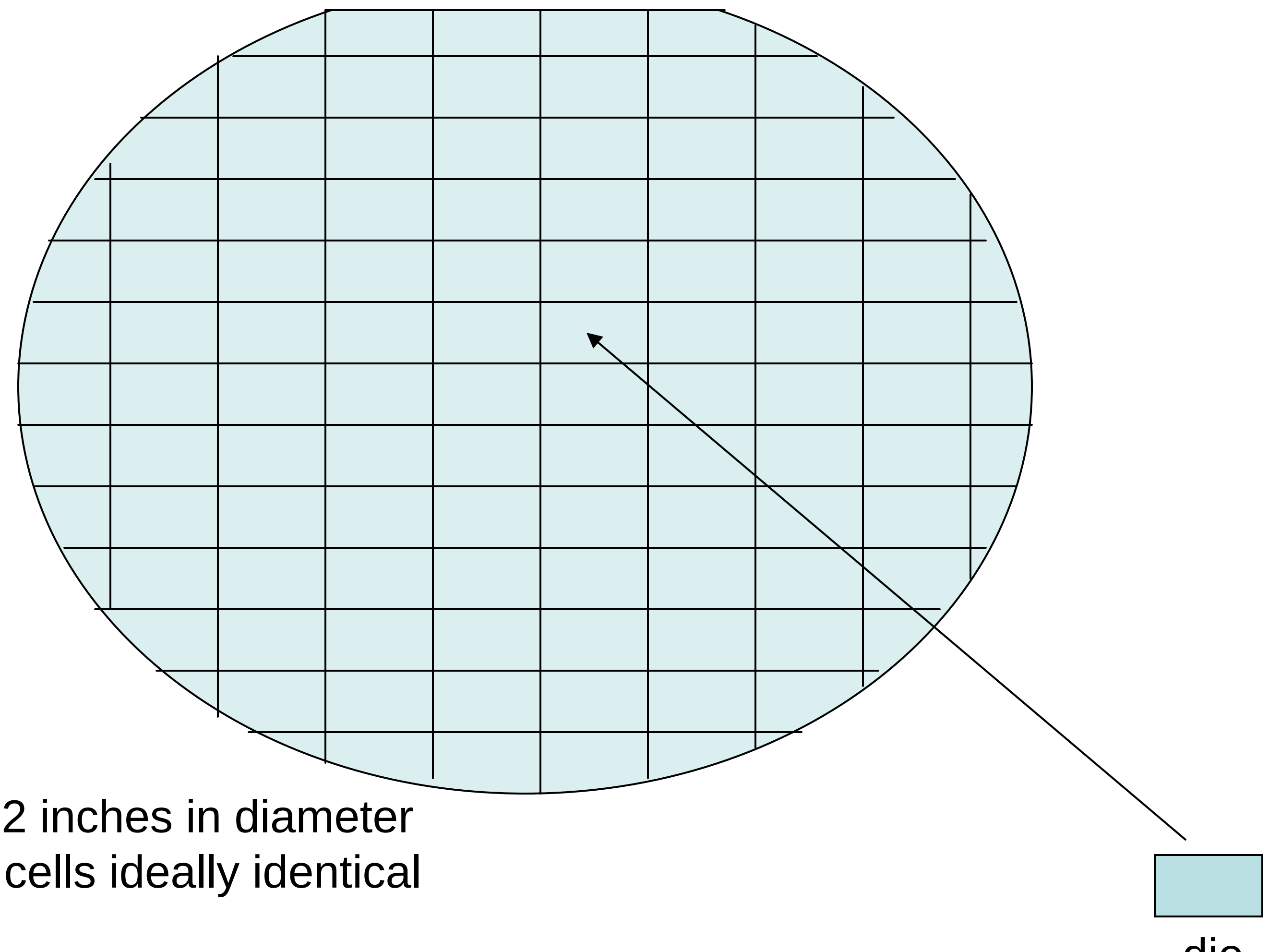
VLSI Design Flow Summary



Comments

- The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems
- Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits

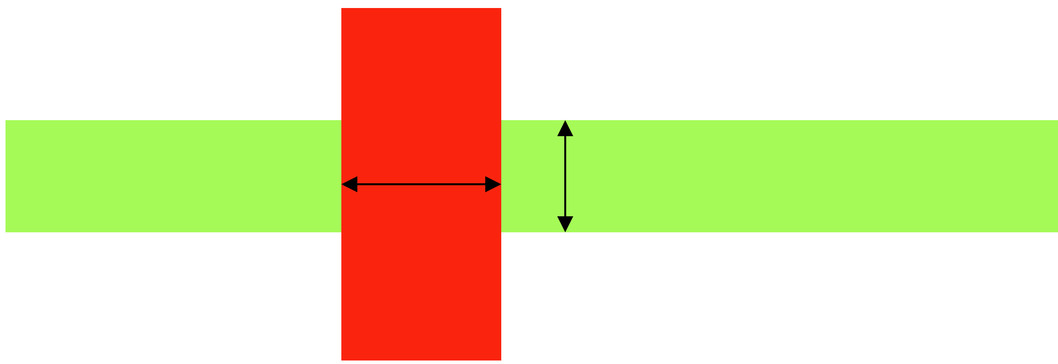
Wafer



- 6 inches to 12 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small

Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured



Often given as either feature size or pitch

Minimum feature size often identical for different features

What is meant by “reliably”

Yield is acceptable if a very large number of these features are made

If P is the probability that a feature is good

n is the number of features on an IC

Y is the yield

$$Y = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$

Example: How reliable must a feature be?

n=5E3

Y=0.9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$ **=0.999979**

But is n=5000 large enough ?

More realistically n=5E9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$ **=0.99999999979**

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes

Feature Size

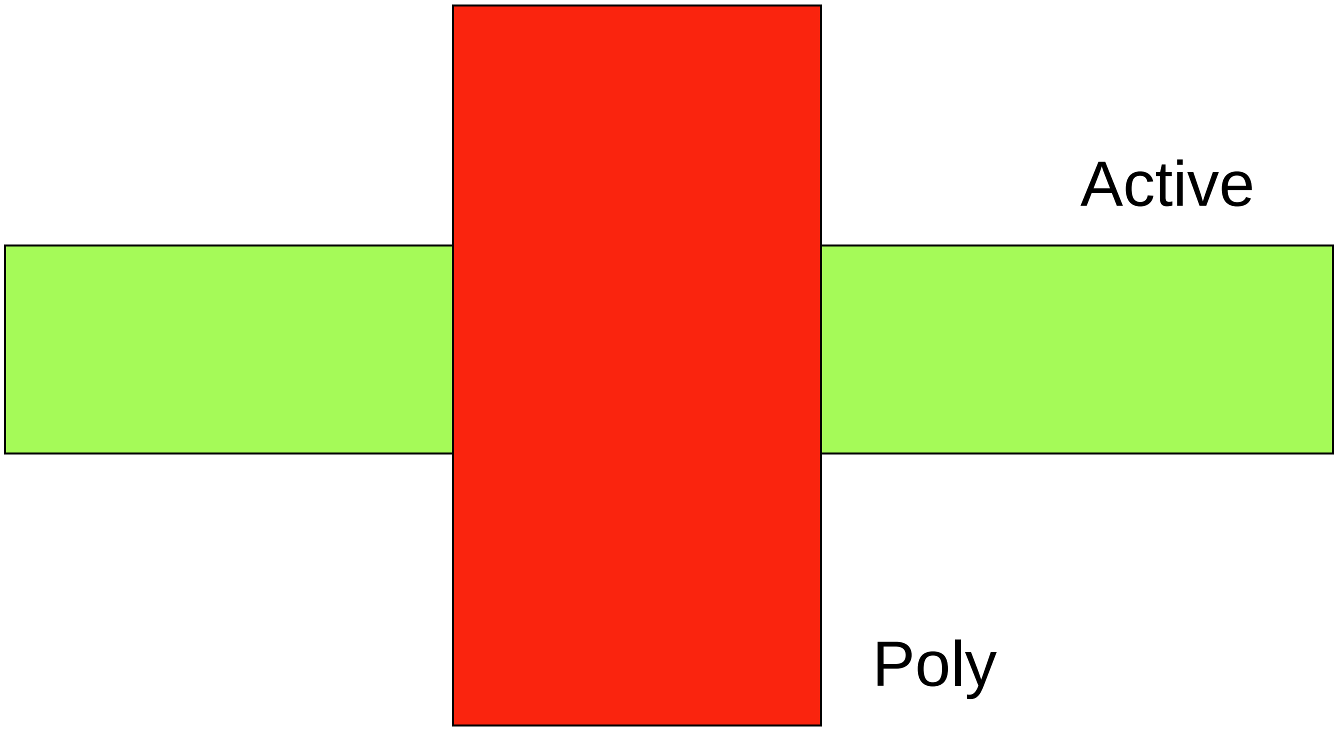
- Typically minimum length of a transistor
- Often minimum width or spacing of a metal interconnect (wire)
- Point of “bragging” by foundries
  - Drawn length and actual length differ
- Often specified in terms of pitch
  - Pitch approximately equal to twice minimum feature size

Feature Size Evolution

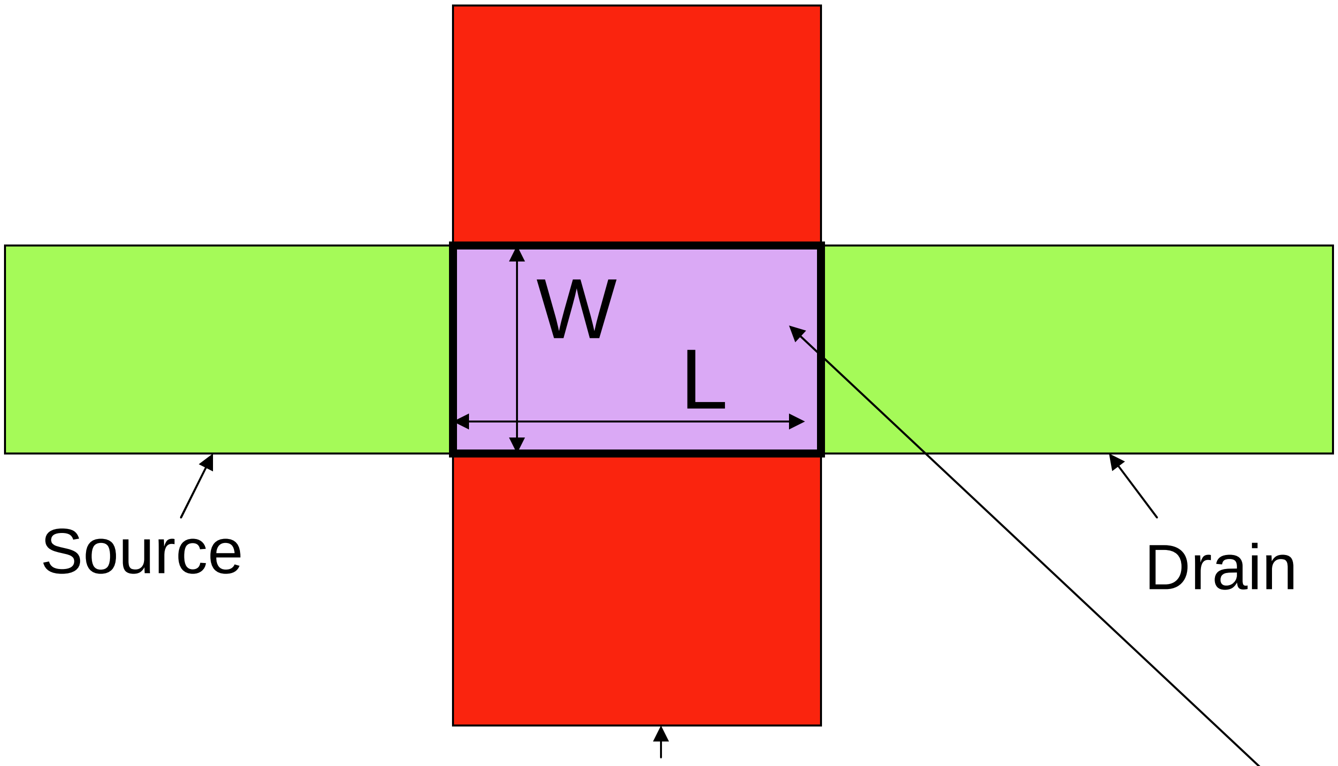
Mid 70's	25µ
2005	90nm
2010	45nm
2020	20nm

$$1\mu = 10^{3} nm = 10^{-6} m = 10^{4} \overset{o}{\mathrm{A}}$$

MOS Transistor

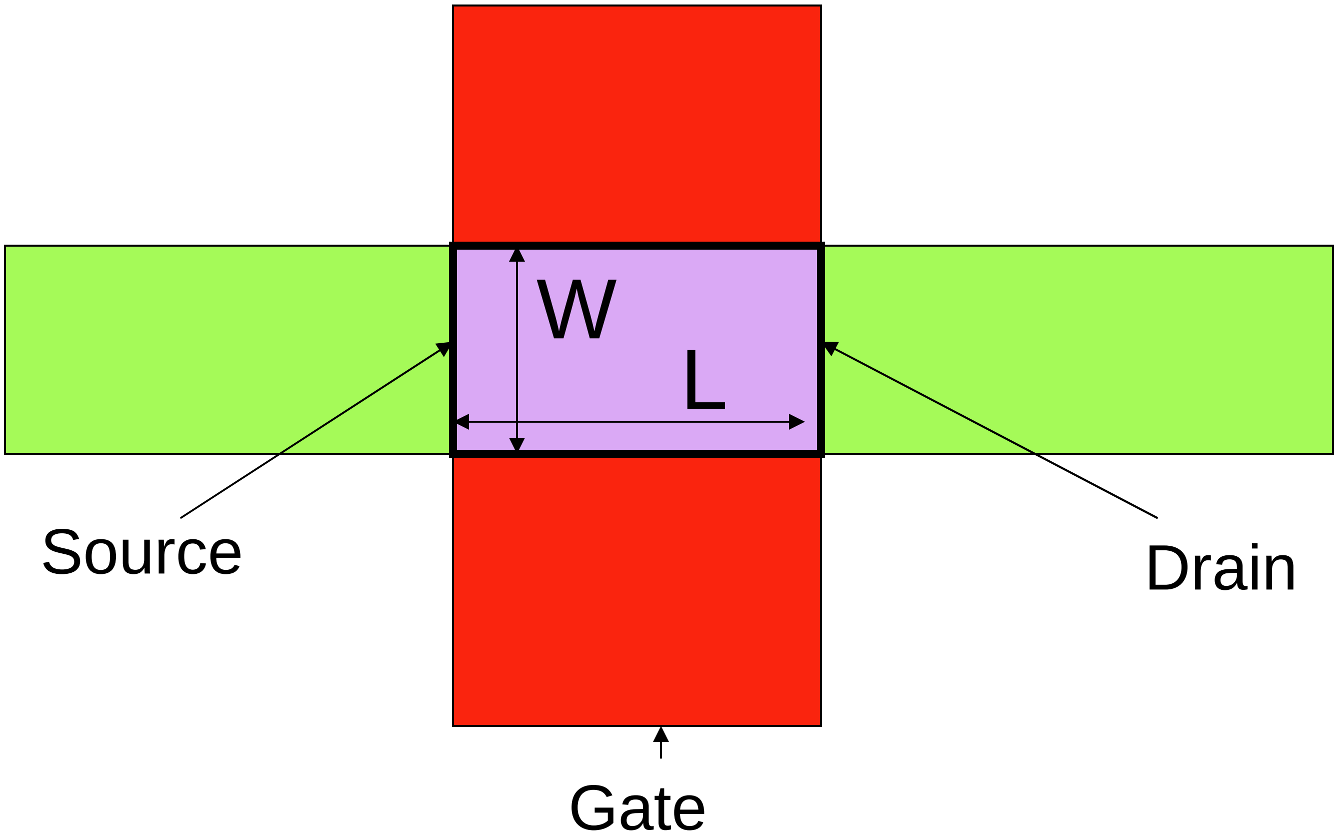


MOS Transistor



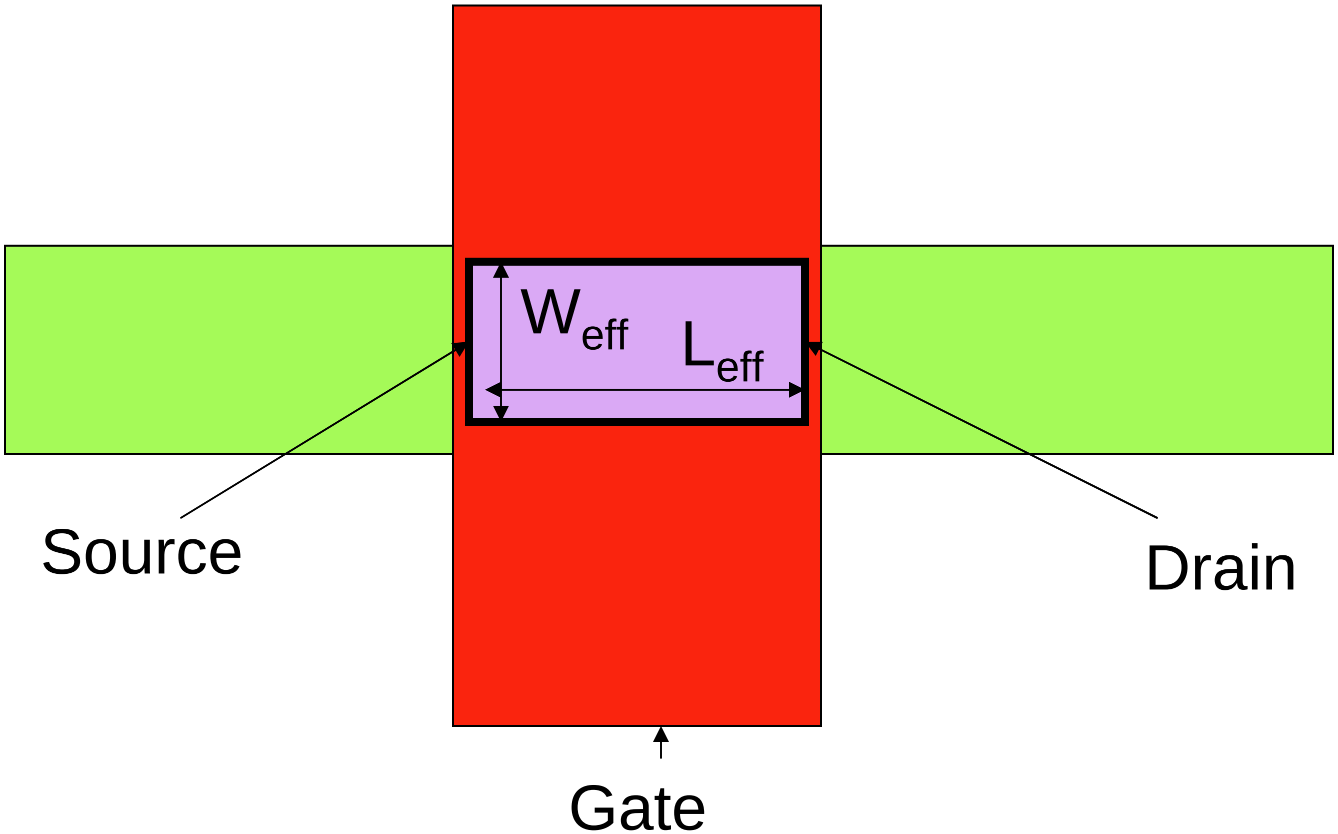
Drawn Length and Width Shown

MOS Transistor



Actual Drain and Source at Edges of Channel

MOS Transistor



Effective Width and Length Generally Smaller than Drawn Width and Length

Technology Nomenclature

- SSI Small Scale Integration 1-100
- MSI Medium Scale Integration $100-10^3$
- LSI Large Scale Integration 10^3-10^5
- VLSI Very Large Scale Integration 10^5-10^6

Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design

Device and Die Costs

Consider the high-volume incremental costs of manufacturing integrated circuits

Example: Assume an 8” wafer in a 0.25µ process costs $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

$$n_{trans} \cong \frac{A_{wafer}}{A_{trans}} = \frac{\pi(4in)^2}{(0.25\mu)^2} = 5.2E11$$

$$C_{trans} = \frac{C_{wafer}}{n_{trans}} = \frac{\$800}{5.2E11} = \$15.4E-9$$

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!

Device and Die Costs

$$C_{per\ unit\ area} \cong \$2.5/cm^2$$

Example: If the die area of the 741 op amp is 1.8mm^2, determine the cost of the silicon needed to fabricate this op amp

$$C_{741} = \$2.5/cm^2 \bullet \left(1.8mm^2\right) \cong \$.05$$

Actual integrated op amp will be dramatically less if bonding pads are not needed

Size of Atoms and Molecules in Semiconductor Processes

Silicon:	Average Atom Spacing	$2.7\,\overset{o}{A}$
	Lattice Constant	$5.4\,\overset{o}{A}$
S_iO_2	Average Atom Spacing	$3.5\,\overset{o}{A}$
	Breakdown Voltage	$5 \text{ to } 10\text{MV/cm} = 5 \text{ to} 10\text{mV}/\overset{0}{A}$
Air		20KV/cm

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches