

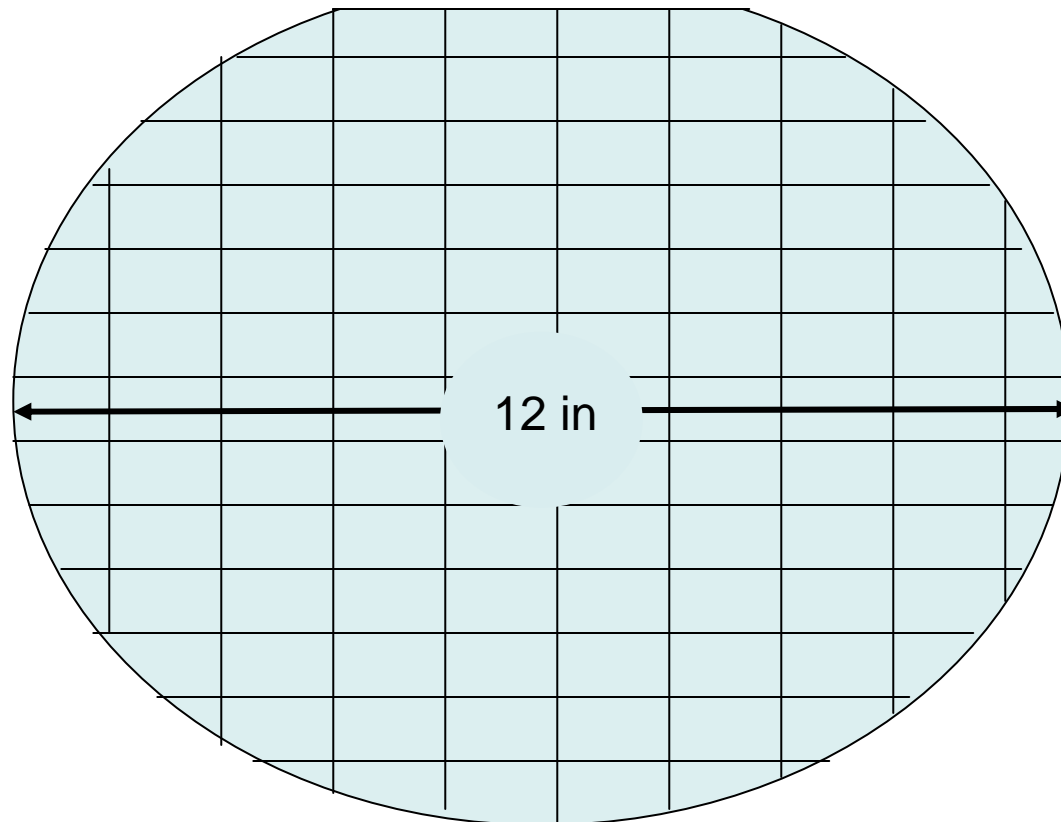
# EE 434

## Lecture 4

### Basic Logic Circuits

## Quiz 2

If the hard yield of a die on a 12 inch wafer in a 180nm process with a defect density of  $1/\text{cm}^2$  is 90%, how many die are there on the wafer?



And the number is ....

1            8            7            5            3  
6            9            4            2

**4**

## Quiz 2

If the hard yield of a die on a 12 inch wafer in a 180nm process with a defect density of  $1/\text{cm}^2$  is 90%, how many die are there on the wafer?

Solution:

$$Y_H = e^{-Ad}$$

$$A = \frac{-\ln(Y_H)}{d} = \frac{-\ln(.9)}{1} = .105\text{cm}^2$$

$$N_{\text{die}} = \frac{A_{\text{WAFER}}}{A_{\text{DIE}}}$$

$$N_{\text{die}} = \frac{A_{\text{WAFER}}}{A_{\text{DIE}}} = \frac{\pi(6\text{in})^2}{.105\text{cm}^2} \left( \frac{2.54\text{cm}}{\text{in}} \right)^2 = 6729$$

## Review from Last Time

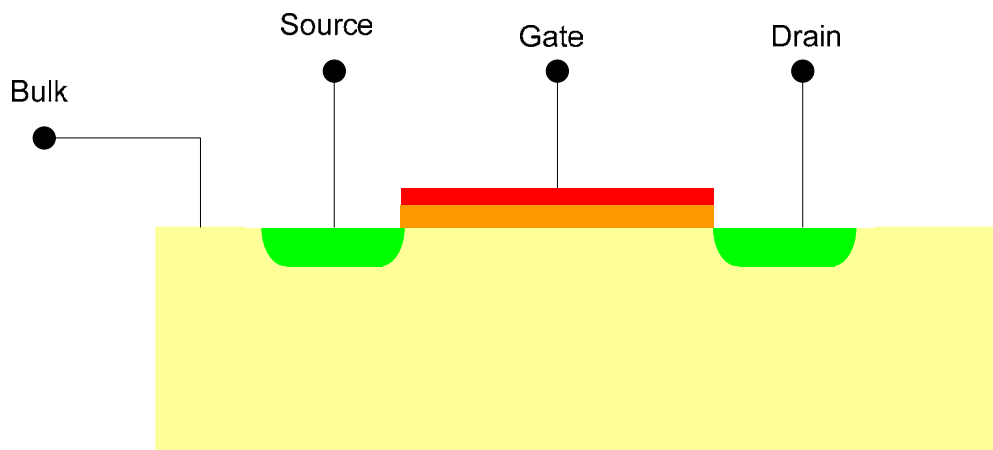
- Hard faults in die place a fundamental limit on practical die size and yield
- Soft faults are of considerable concern in many applications as well
- Arbitrary assignment of yield expectations to any part of a process is an invitation to financial disaster
- Semiconductor industry got its start about 50 years ago but only the growth in the past decade has made it one of major economic forces in the world economy

# Basic Logic Circuits

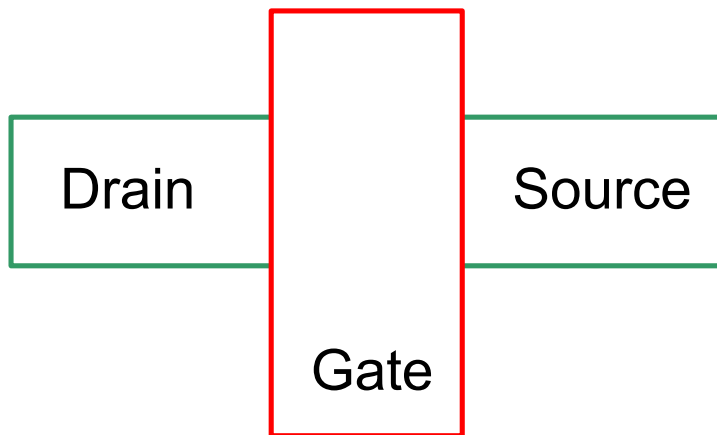
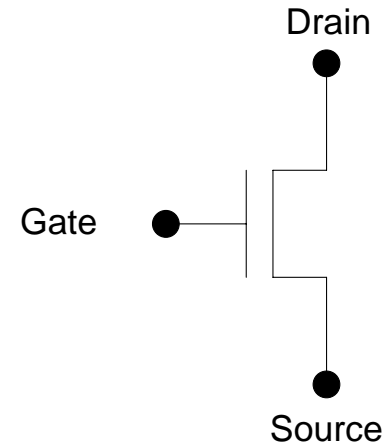
- Will present a brief description of logic circuits based upon simple models and qualitative description of processes
- Will discuss process technology needed to develop better models
- Will provide more in-depth discussion of logic circuits based upon better device models







# MOS Transistor

## Qualitative Discussion of n-channel Operation



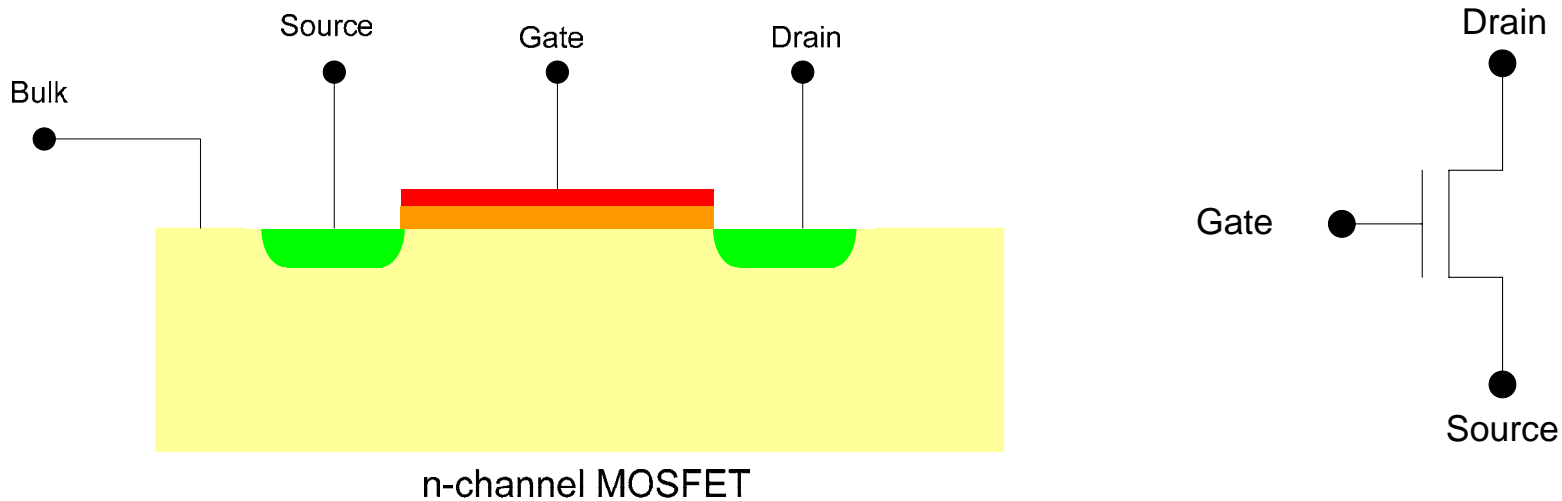
n-channel MOSFET



-  n-type
-  n+-type
-  p-type
-  p+-type
-  SiO<sub>2</sub> (insulator)
-  POLY (conductor)

# MOS Transistor

## Qualitative Discussion of n-channel Operation



### Behavioral Description of Basic Operation

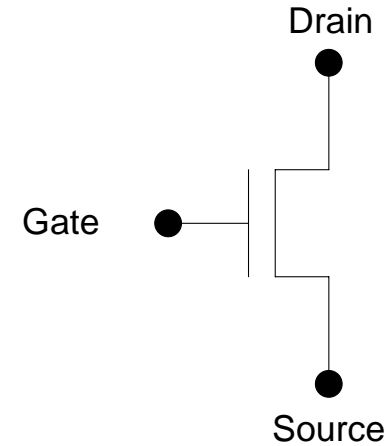
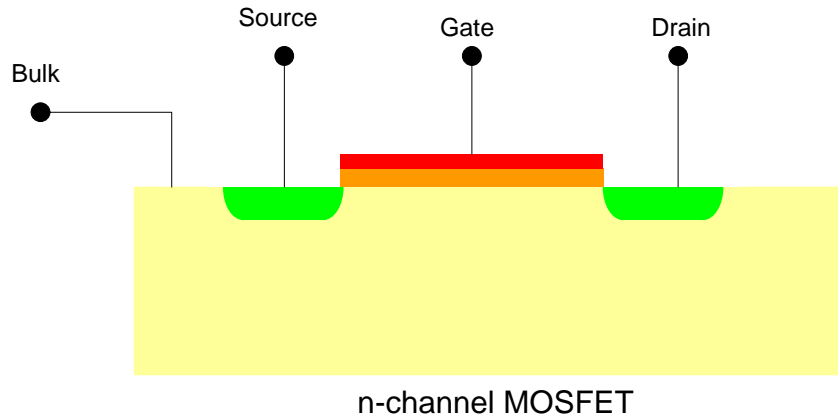
If  $V_{GS}$  is large, short circuit exists between drain and source

If  $V_{GS}$  is small, open circuit exists between drain and source

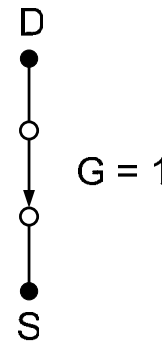
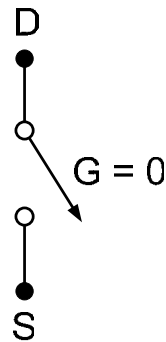


# MOS Transistor

## Qualitative Discussion of n-channel Operation

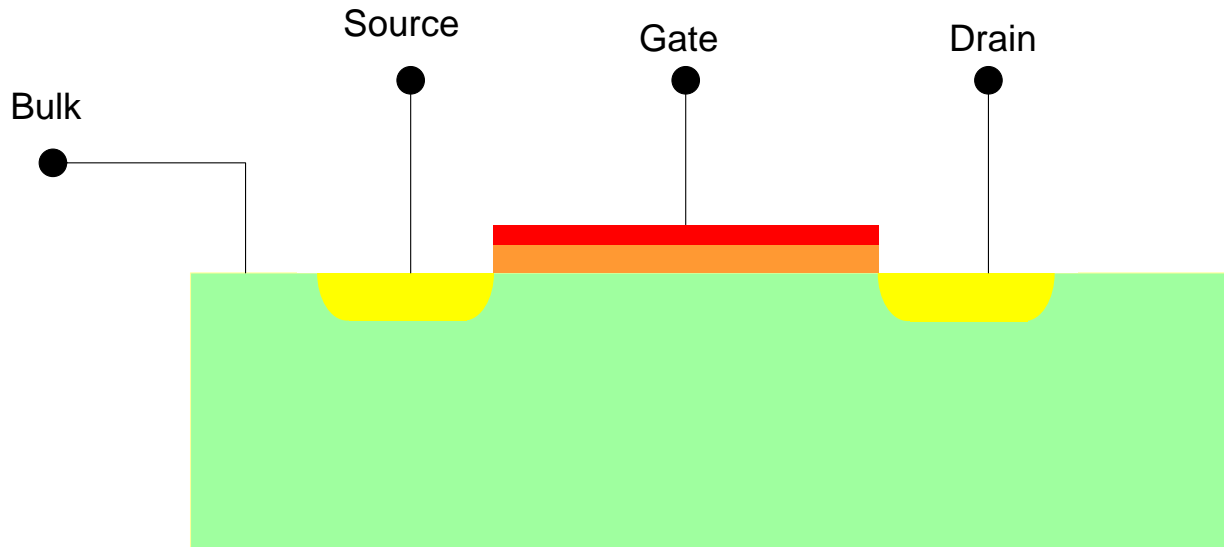


### Equivalent Circuit for n-channel MOSFET

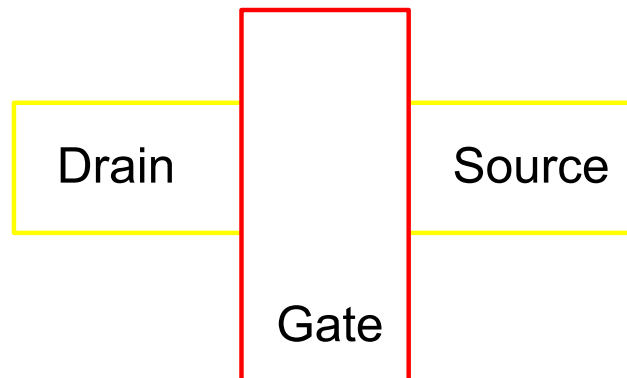
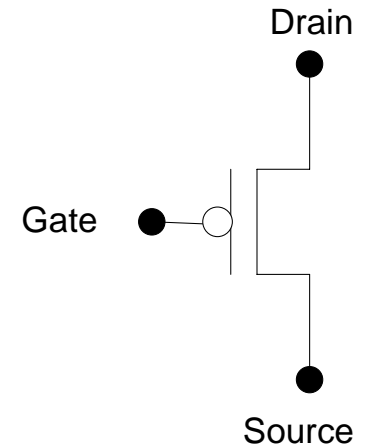








# MOS Transistor

## Qualitative Discussion of p-channel Operation



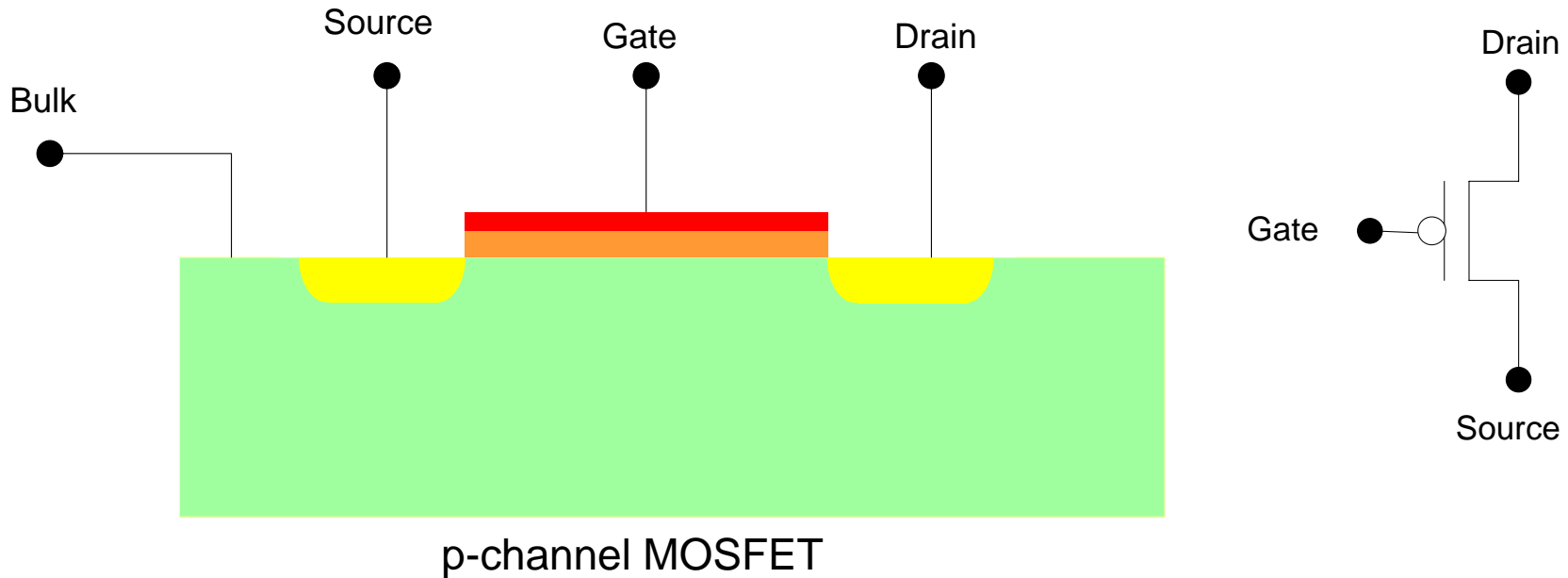
p-channel MOSFET



-  n-type
-  n<sup>+</sup>-type
-  p-type
-  p<sup>+</sup>-type
-  SiO<sub>2</sub> (insulator)
-  POLY (conductor)

# MOS Transistor

## Qualitative Discussion of p-channel Operation



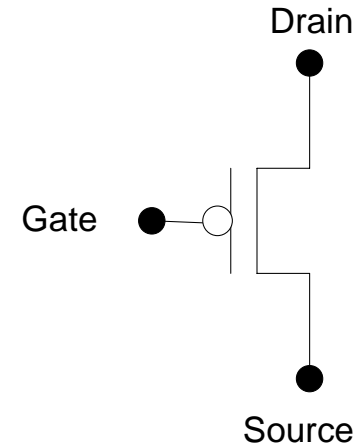
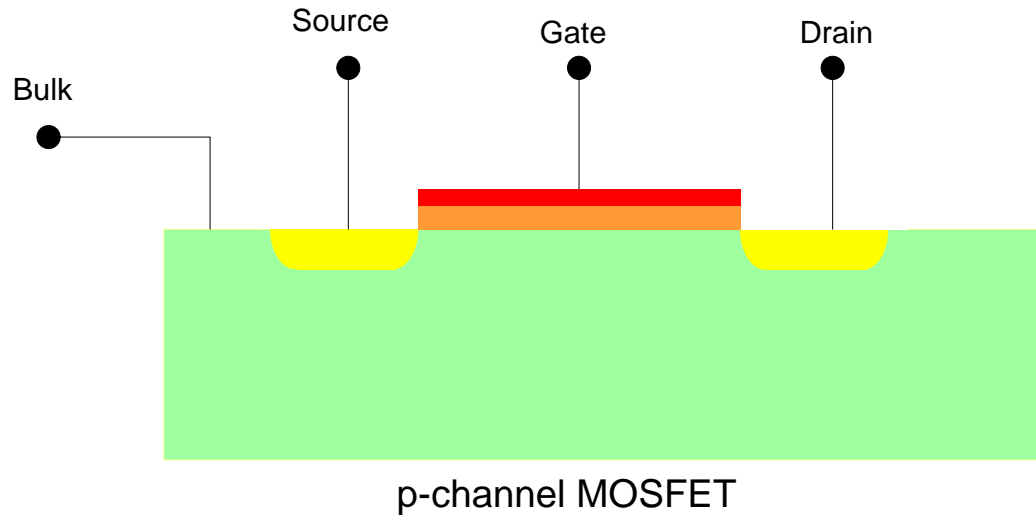
### Behavioral Description of Basic Operation

If  $V_{GS}$  is small (negative), short circuit exists between drain and source

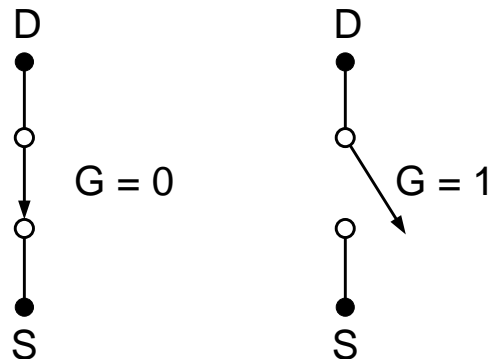
If  $V_{GS}$  is large (near 0), open circuit exists between drain and source

# MOS Transistor

## Qualitative Discussion of p-channel Operation

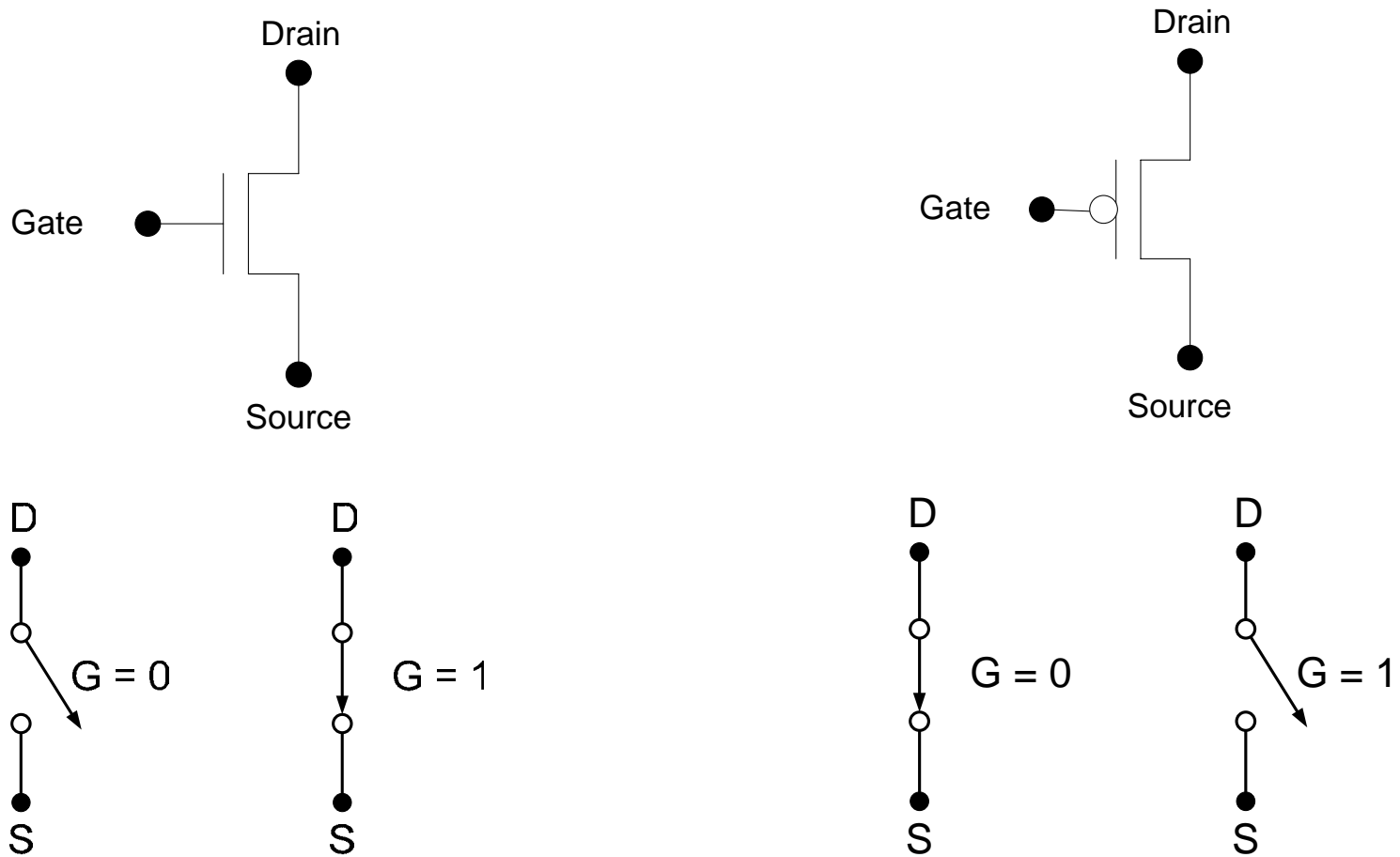


### Equivalent Circuit for p-channel MOSFET

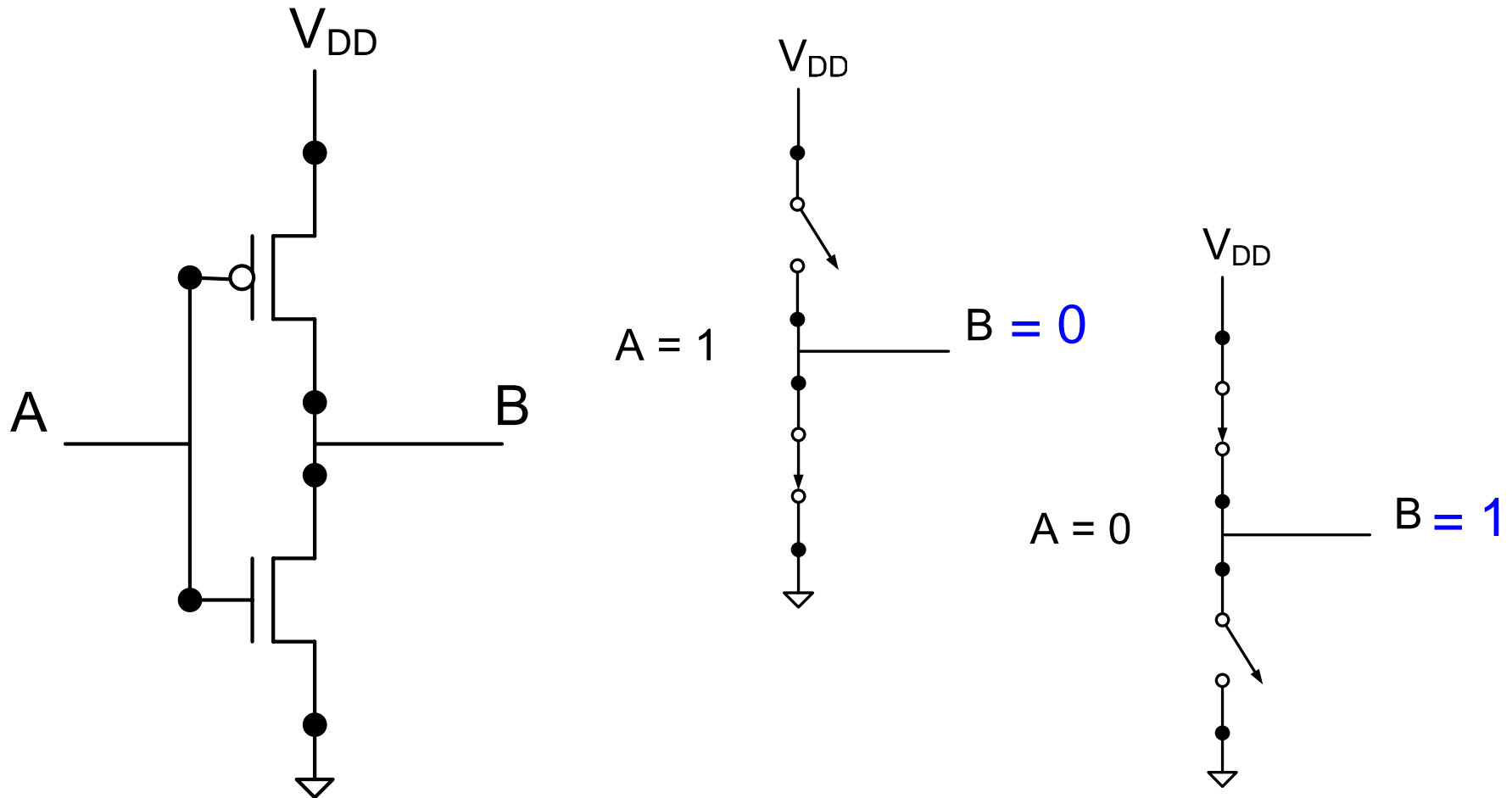


# MOS Transistor

## Comparison of Operation

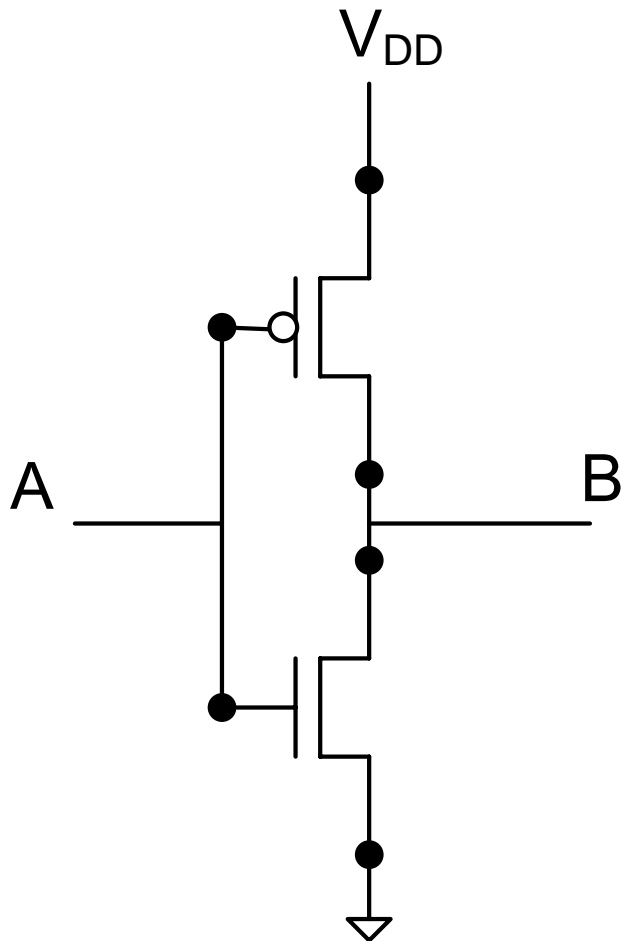


# Logic Circuits



**Circuit Behaves as a Boolean Inverter**

# Logic Circuits

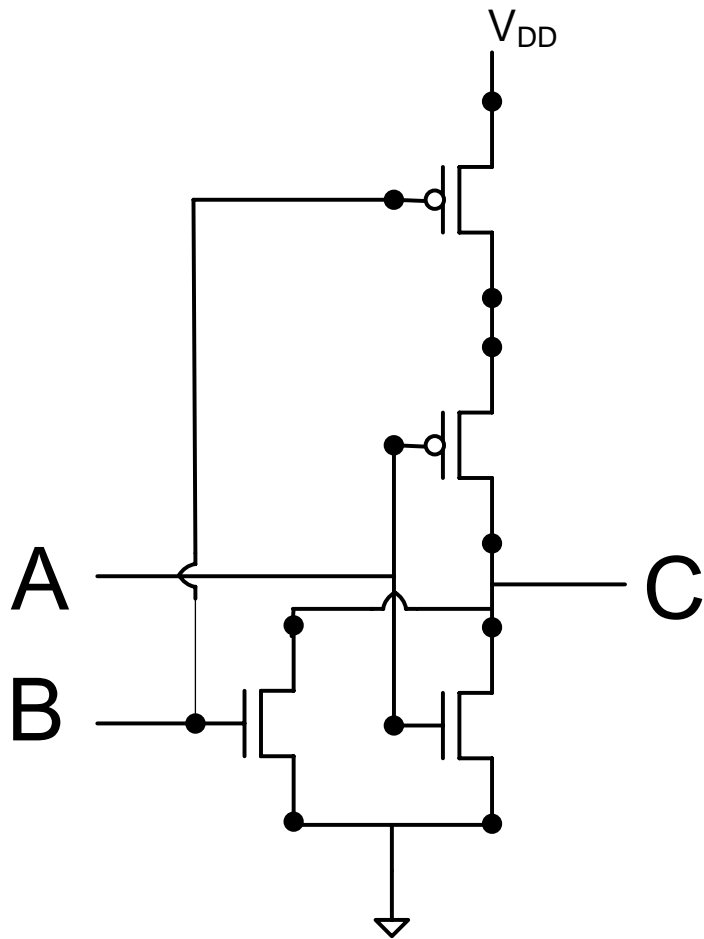


**Inverter**

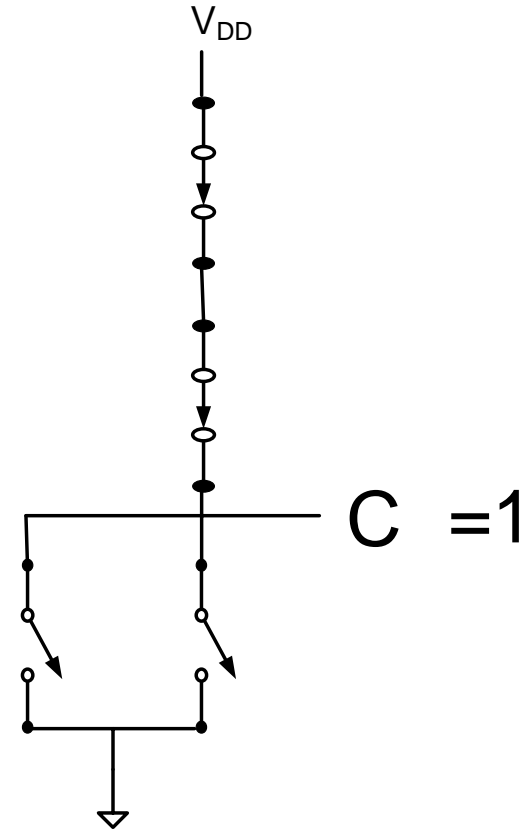
Truth Table

A	B
0	1
1	0

# Logic Circuits

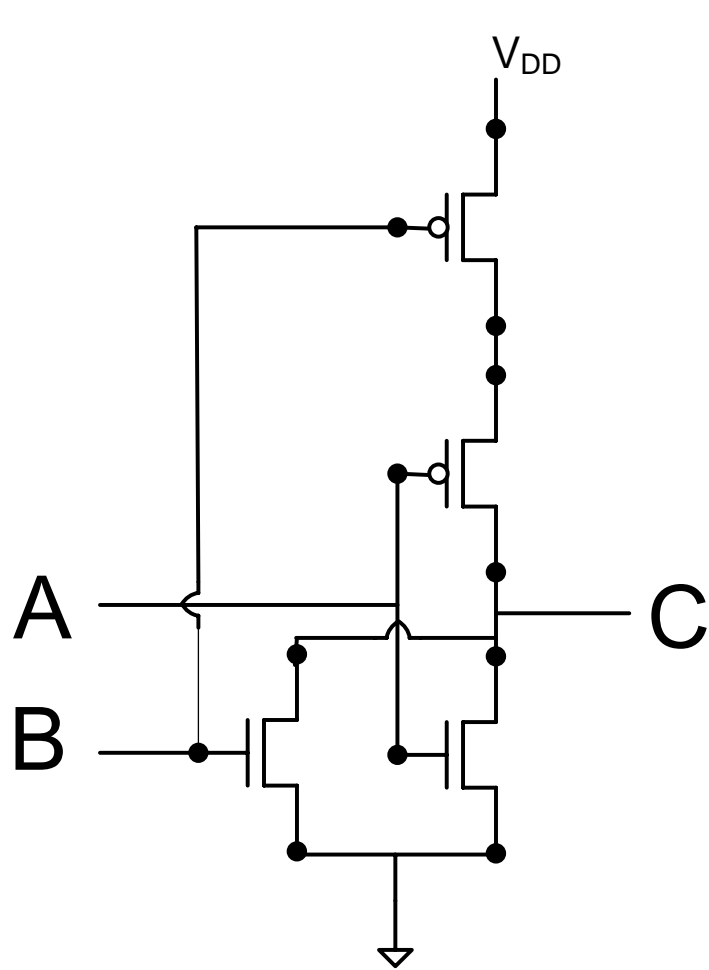


$A=0$   
 $B=0$

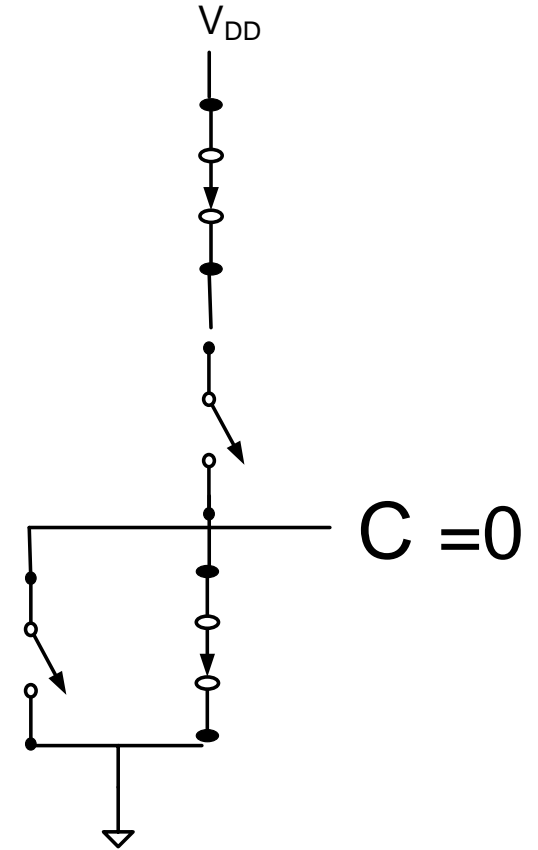




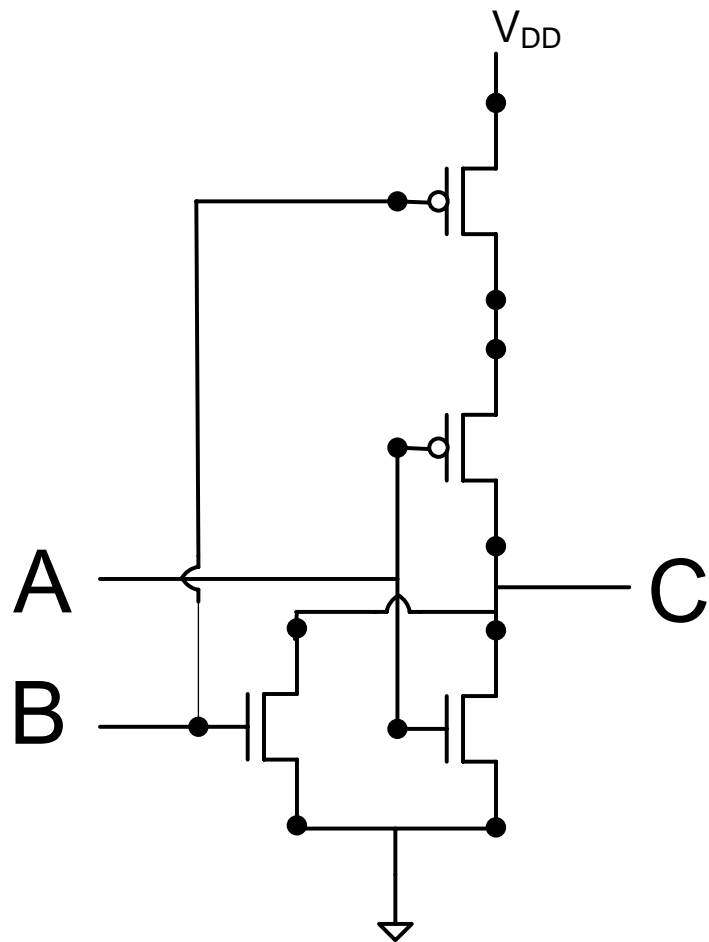
# Logic Circuits



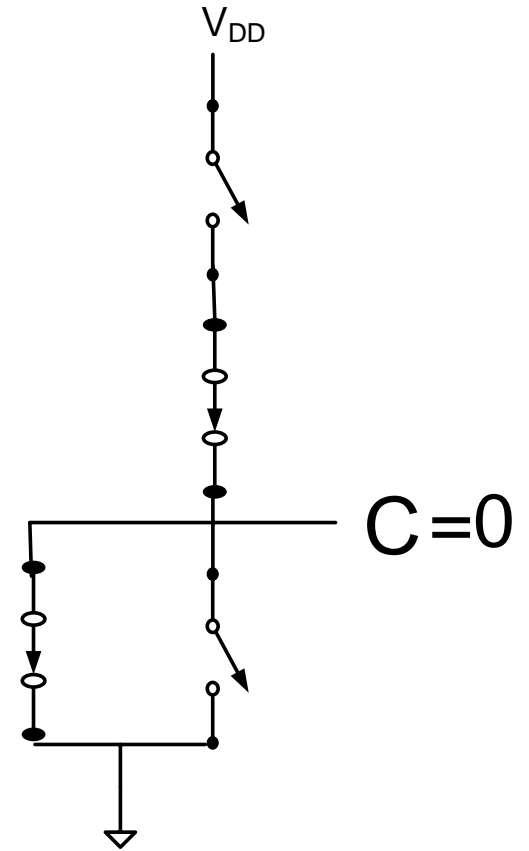
$A=1$   
 $B=0$



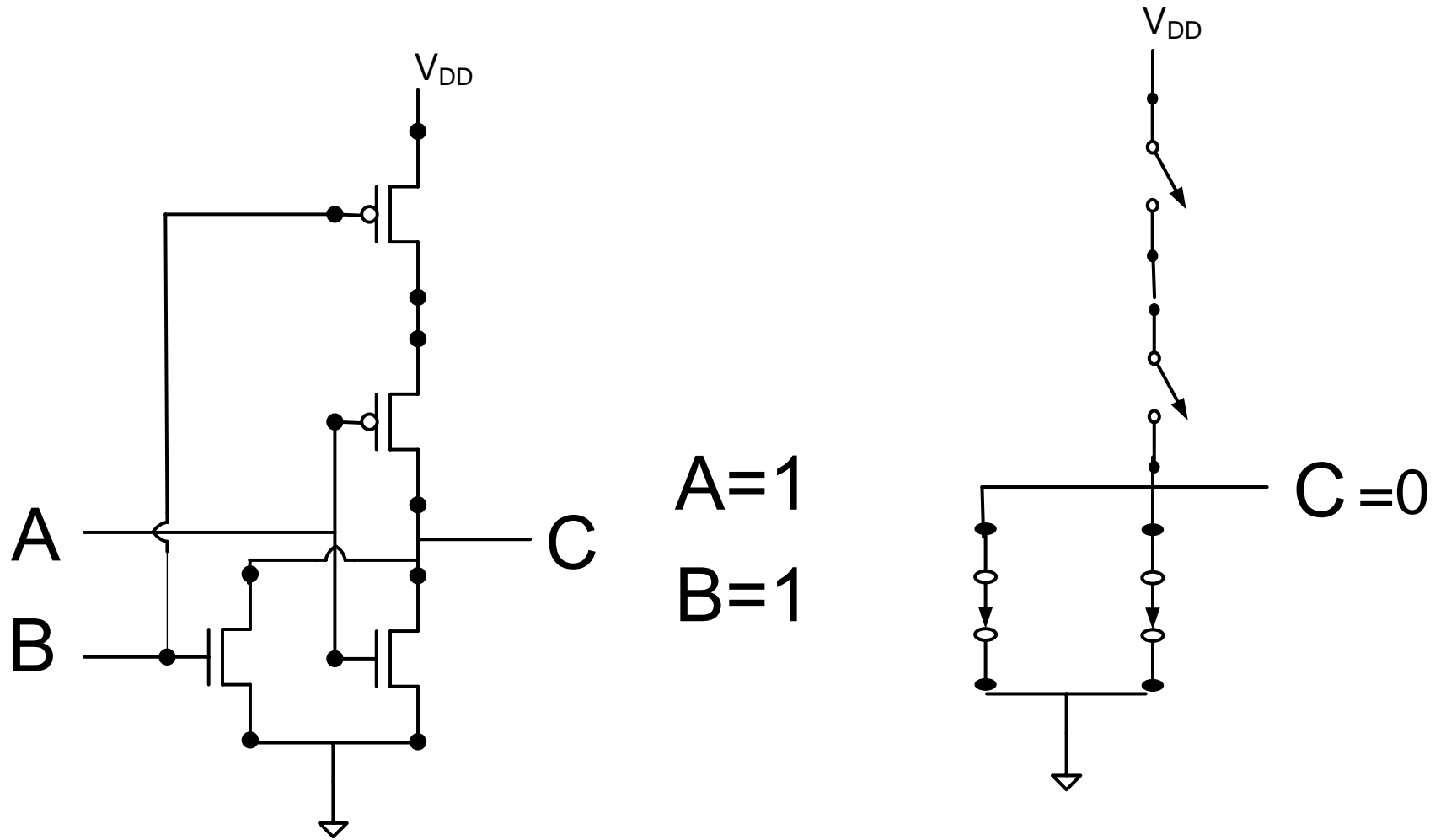
# Logic Circuits



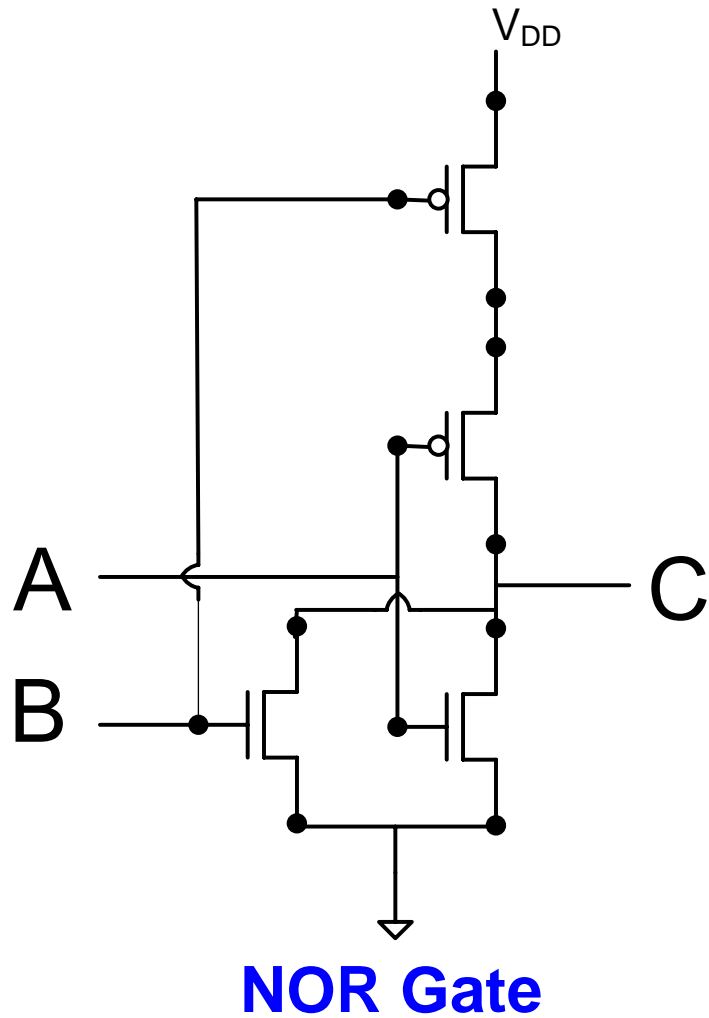
A=0  
B=1



# Logic Circuits



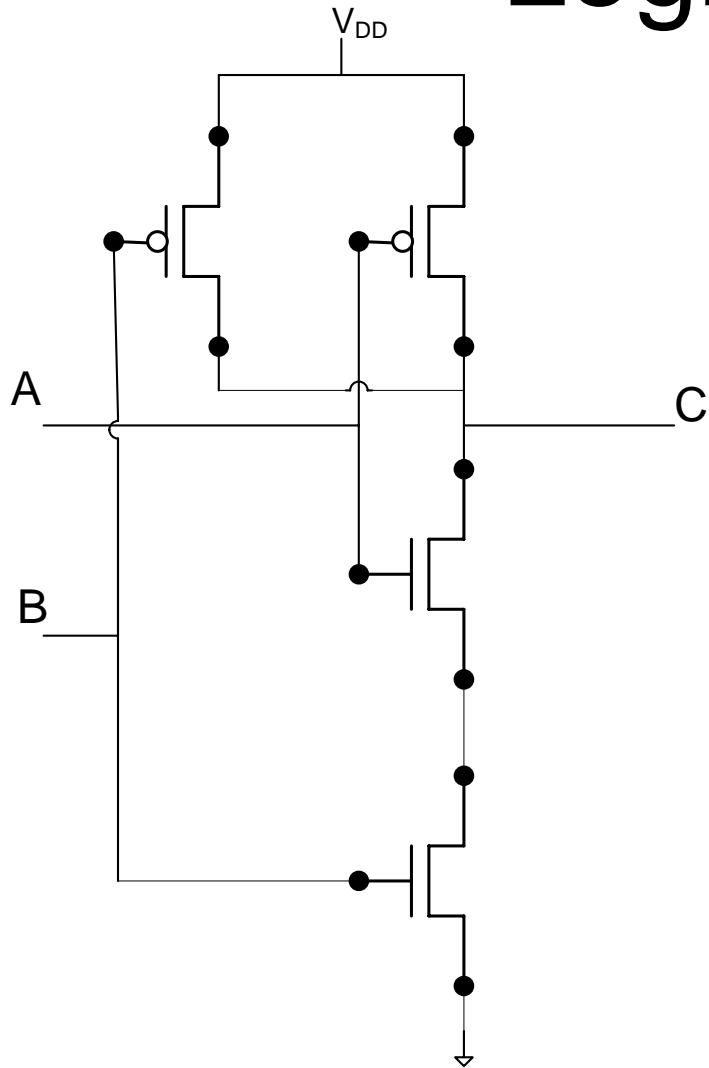
# Logic Circuits



Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

# Logic Circuits



**NAND Gate**

Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0