

# EE 434

## Lecture 5

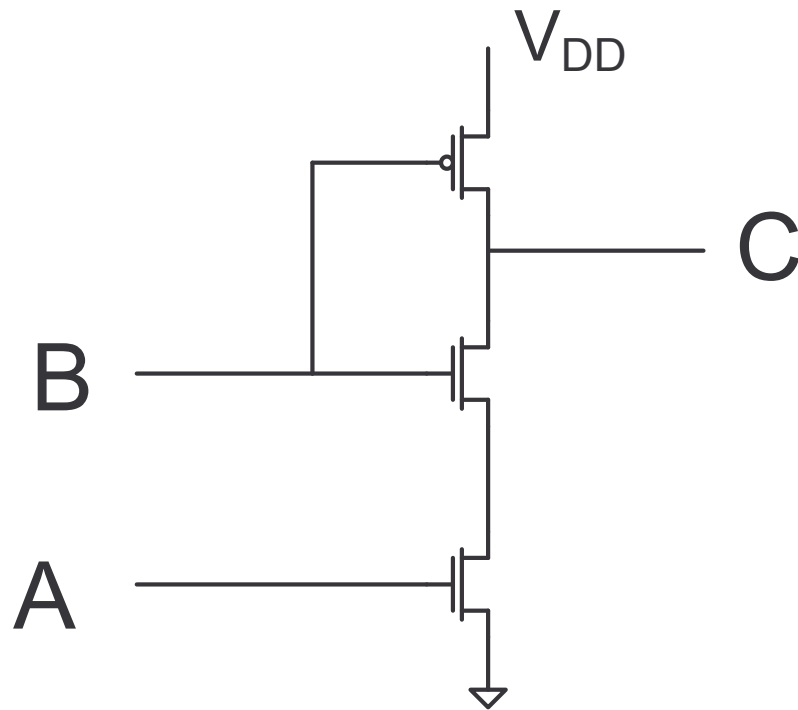
### Basic Logic Circuits

## Quiz 3

A proposed two-input Boolean Gate is shown

- Determine the Boolean output C if  $A=B=1$
- Is this a viable gate (give reasons for your answer)

Use a switch-level model for the MOS devices



And the number is ....

1            8            7            5            3  
6            9            4            2

8

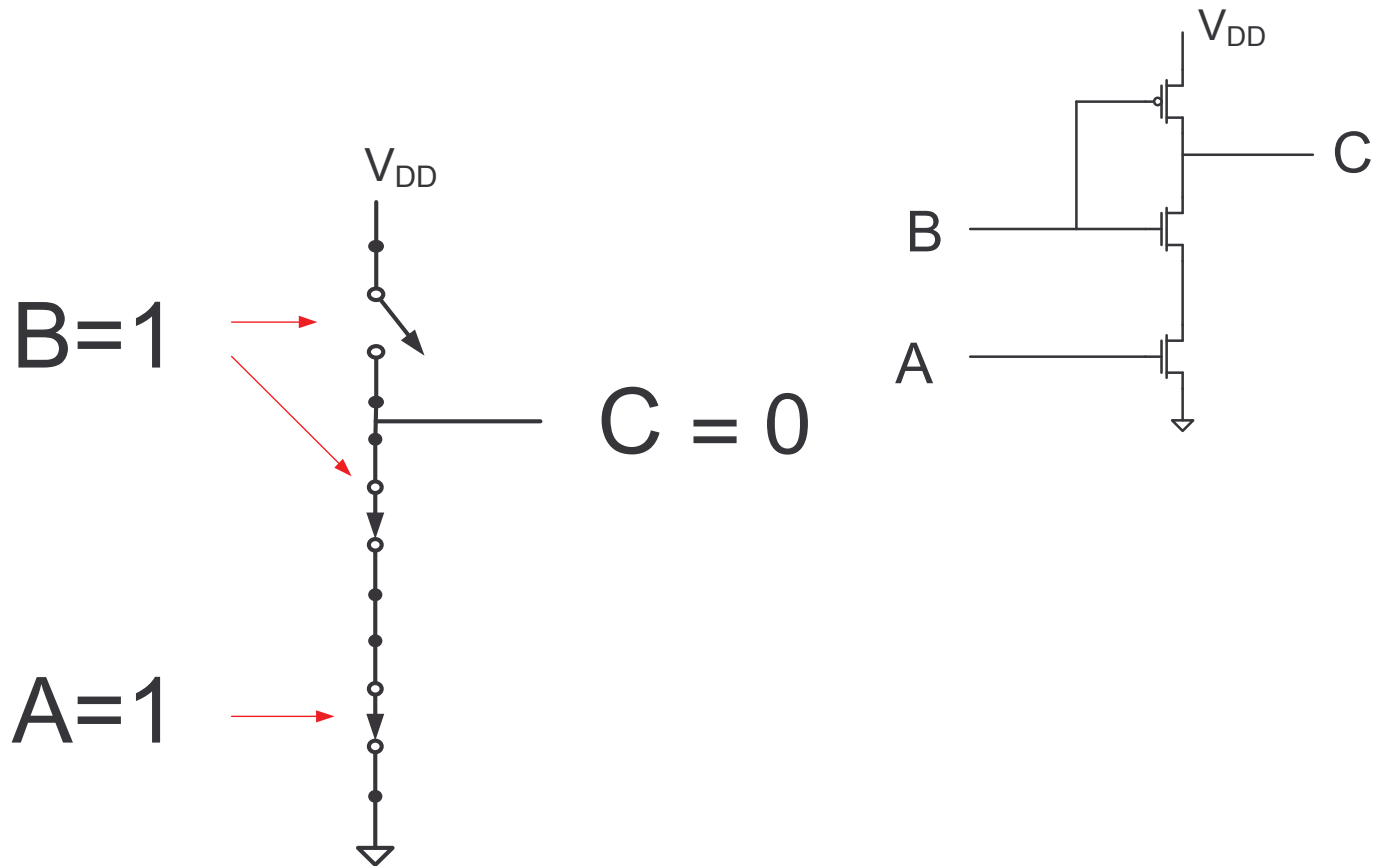
### Quiz 3

A proposed two-input Boolean Gate is shown

- Determine the Boolean output C if  $A=B=1$
- Is this a viable gate (give reasons for your answer)

Solution:

- If  $A=B=1$



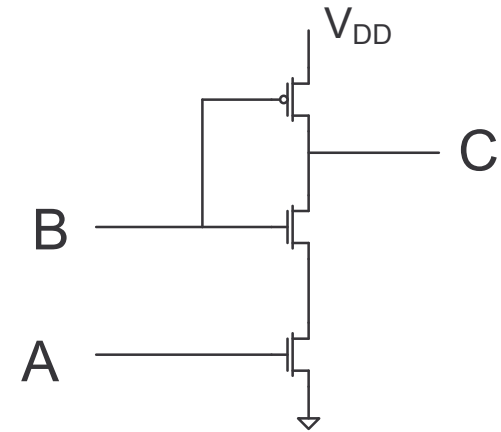
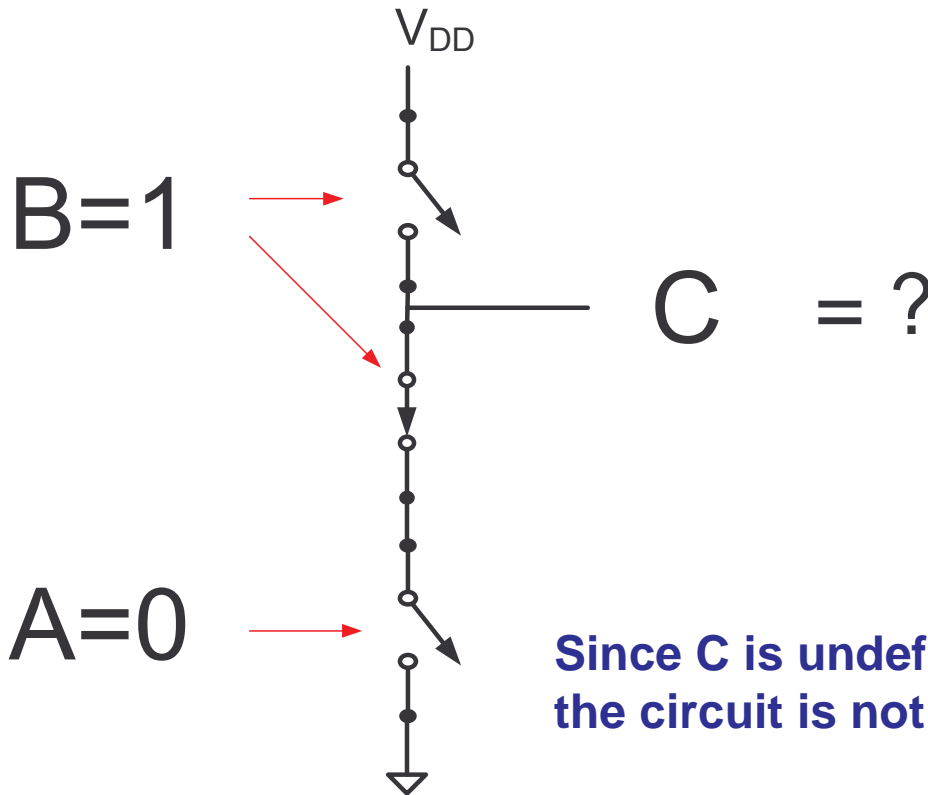
### Quiz 3

A proposed two-input Boolean Gate is shown

- Determine the Boolean output C if  $A=B=1$
- Is this a viable gate (give reasons for your answer)

Solution:

- If  $B=1$  and  $A=0$

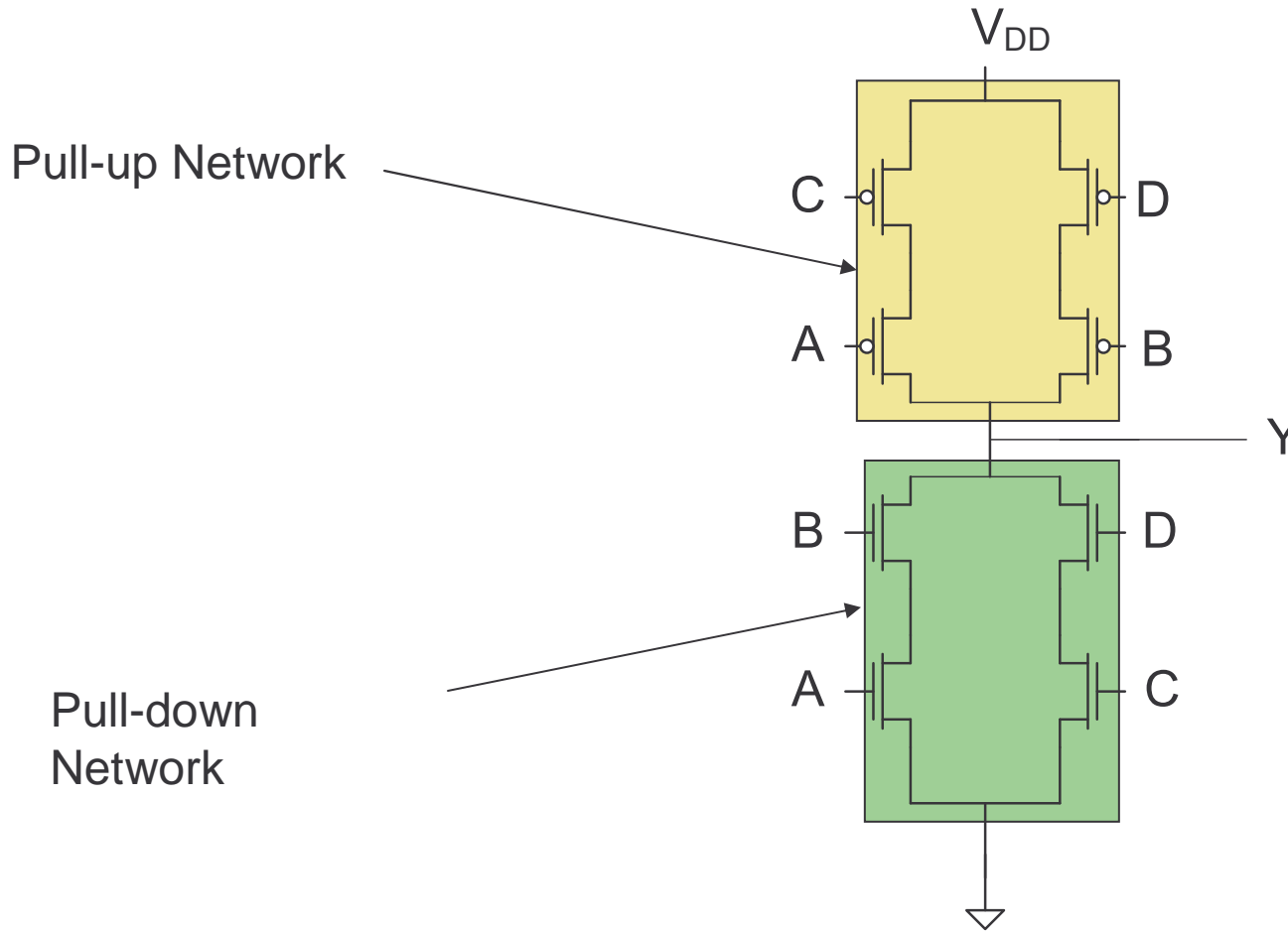


Since C is undefined for this input condition, the circuit is not a viable Boolean gate

## Review from Last Time

- Simple model of MOSFET was developed
  - hierarchical model structure will be developed
  - generally use simplest model that can be justified
- Simple CMOS gates were introduced
  - Zero power dissipation
  - Rail to Rail Swings
  - Infinitely Fast
  - Simple model may not give sufficiently accurate insight relating to these properties

# Complex Gates

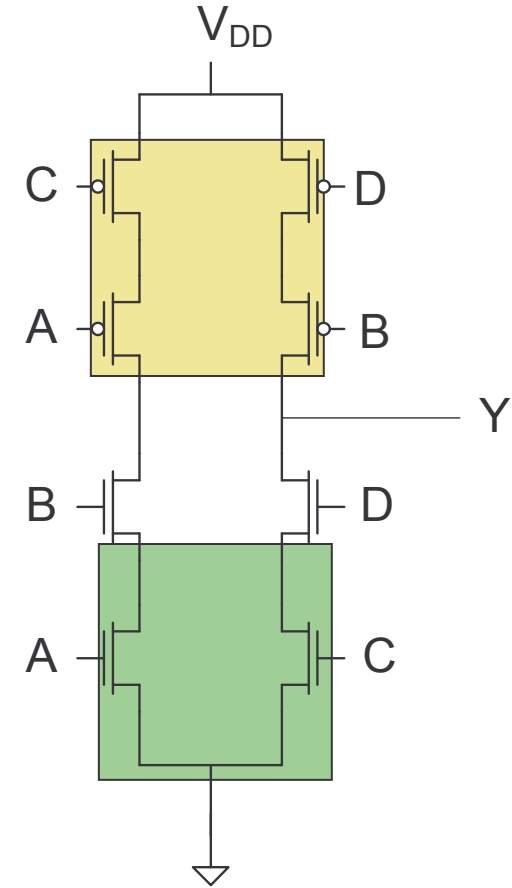


$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

# Complex Gates

Pull up and pull down network never both conducting

One of the two networks is always conducting



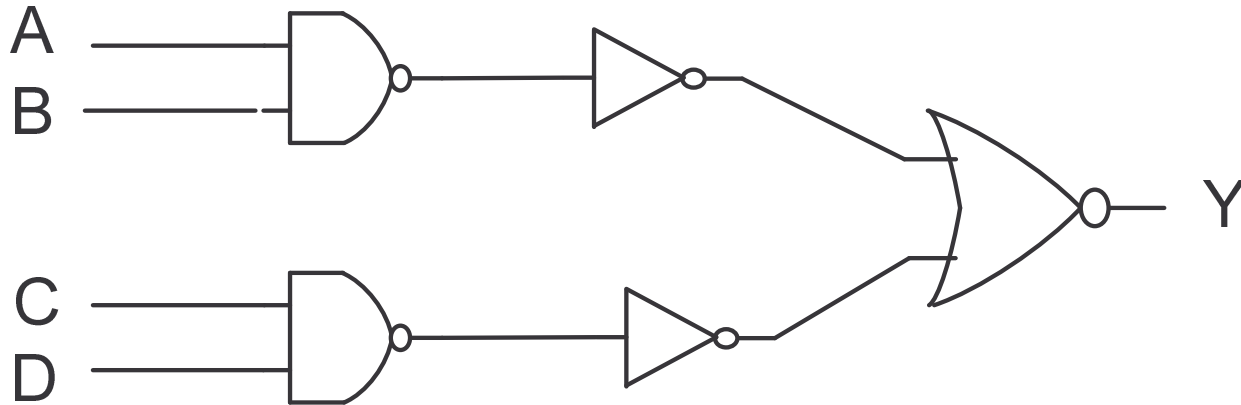
$$Y = \overline{(A \bullet B) + (C \bullet D)}$$



# Consider

$$Y = \overline{(A \cdot B) + (C \cdot D)}$$

## Alternate Implementation



**3 levels of Logic**

**16 Transistors if Basic CMOS Gates are Used**

Consider  $Y = A \cdot B$

Standard CMOS Implementation

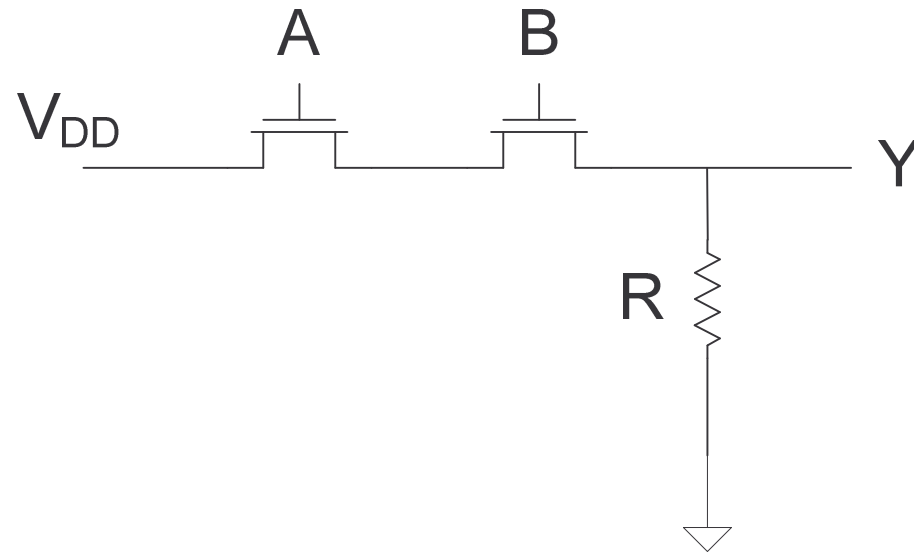


**2 levels of Logic**

**6 Transistors if Basic CMOS Gates are Used**

**Basic noninverting functions generally require more complexity if basic CMOS gates are used for implementation**

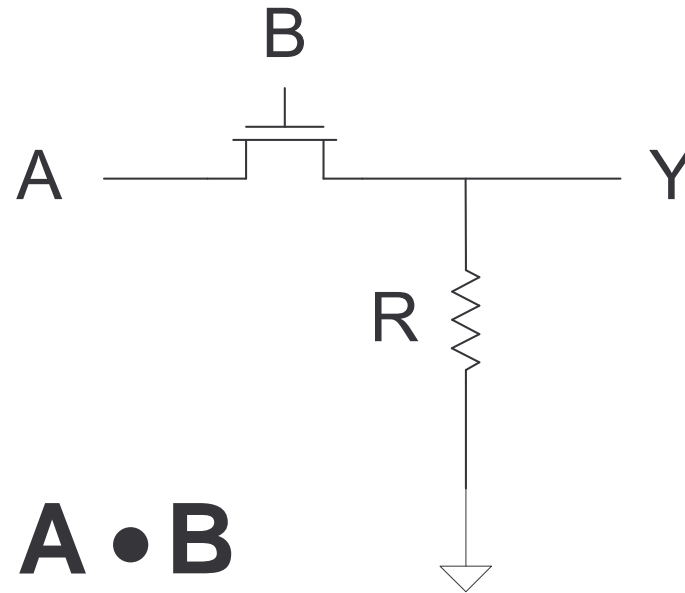
# Pass Transistor Logic



$$Y = A \cdot B$$

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor).

# Pass Transistor Logic

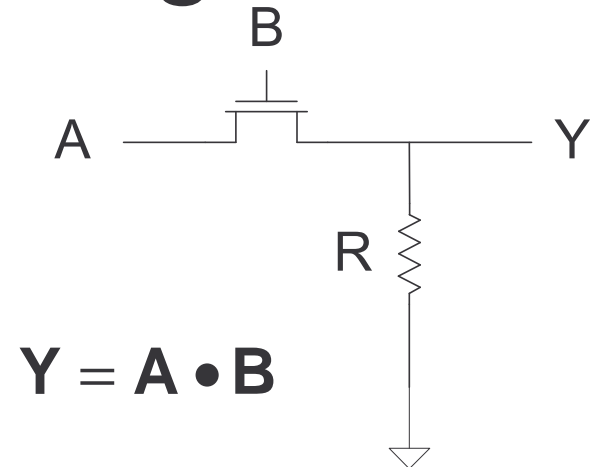


$$Y = A \cdot B$$

Even simpler pass transistor logic implementations are possible

Requires only 1 transistor (and a resistor).

# Pass Transistor Logic



Requires only 1 transistor (and a resistor)

- Resistor may require more area than several hundred or even several thousand transistors
- Signal levels may not go to  $V_{DD}$
- Static power dissipation may not be zero
- Signals may degrade unacceptably if multiple gates are cascaded
- “resistor” often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist
- Pass transistor logic is widely used

# Logic Design Styles

- Several different logic design styles are often used throughout a given design
- The designer has complete control over what is placed on silicon and governed only by cost and performance
- New logic design strategies have been proposed recently and others will likely emerge in the future
- The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements