Quiz 4

A proposed three-input Boolean Gate is shown

a. Determine the Boolean output $Y$

b. Is the static power dissipation of this gate zero?

(use the switch-level model of the MOSFET)
And the number is ....

1  8  7  6  9  4  5  2  3

4
Quiz 4

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a. Determine the Boolean output Y
b. Is the static power dissipation of this gate zero? (use the switch-level model of the MOSFET)

Solution:

a) From PDN observe

\[ Y = A \cdot (B + C) \]

In standard Sum of Products form

\[ Y = \overline{A} + \overline{B} \cdot \overline{C} \]

b) Yes – note PU and PD networks are never both conducting
Different Logic Design Styles Can Be Used

– PTL is one style that can offer significant reductions in complexity
– Signal Degradation and Static Power Dissipation are issues of concern when using PTL
– Designer is under complete control of circuits that are placed on the silicon
– Many designs will mix multiple logic design styles
– New logic design styles are still being proposed and adopted
Improved Switch-Level Model

Switch-level model including gate capacitance and drain resistance

Switch closed for \( V_G=1 \)
Improved Switch-Level Model

Switch-level model including gate capacitance and drain resistance

Switch closed for $V_G = 0$

Switch-level model including gate capacitance and drain resistance
Improved Switch-Level Model

C\textsubscript{GS} and R\textsubscript{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5μ process

C\textsubscript{GS} \approx 1.5\text{fF} \quad R\textsubscript{sw} \approx \begin{cases} 2\text{KΩ} & \text{n-channel} \\ 6\text{KΩ} & \text{p-channel} \end{cases}

Considerable emphasis will be placed upon device sizing to manage C\textsubscript{GS} and R\textsubscript{SW}
Example

With switch level model

A

Y

1 pf
Example (cont)

With improved model
Example (cont)

With improved model

\[ V_{OUT} \]

\[ C_{GS} \]

\[ R_{SW}=2K \]

\[ 5V \]

\[ 1pf \]
Example (cont)

With improved model

Recall: Step response of any first-order network with LHP pole can be written as

\[ y(t) = F + (I - F)e^{-\frac{t}{\tau}} \]

where F is the final value, I is the initial value and \( \tau \) is the time constant of the circuit

For the circuit above, F=0, I=5 and \( \tau = R_{SW}C_L \)
Example (cont)

With improved model

\[ t_{HL} \equiv R_{SW}C_L = 2K \cdot 1pF = 5E-9\sec = .5n\sec \]
Stick Diagrams

- It is often necessary to obtain information about placement, interconnect and physical-layer structure
- Stick diagrams are often used for small component-count blocks
- Approximate placement, routing, and area information can be obtained rather quickly with the use of stick diagrams
Stick Diagrams

Metal 1
poly
n-diffusion
p-diffusion
Metal 2
Contact

Additional layers can be added and color conventions are personal.
A stick diagram is not a layout but gives the basic structure that will be instantiated in the actual layout itself.

Modifications can be made much more quickly on a stick diagram than on a layout.

Iteration may be needed to come up with a good layout structure.
Stick Diagram

Alternate Representation