EE 434
Lecture 6

Logic Circuits
Process Technology

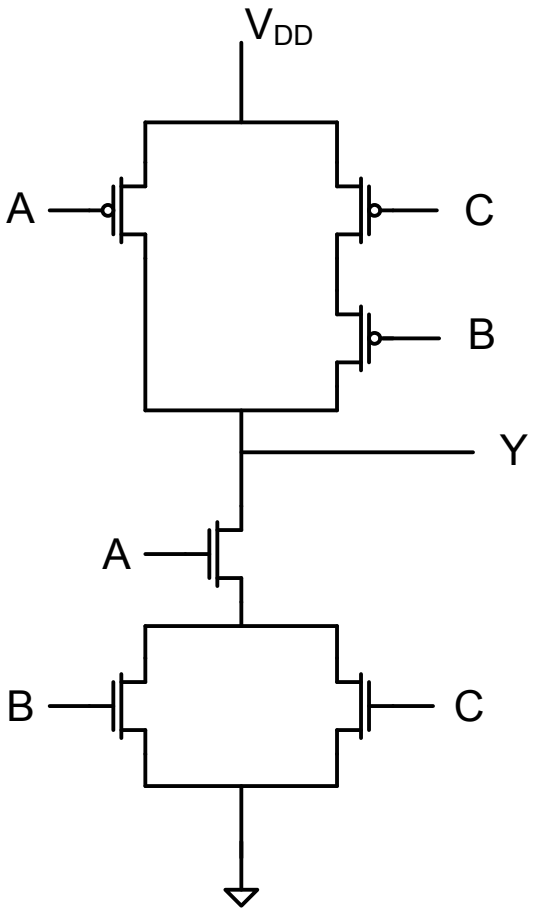
Quiz 4

A proposed three-input Boolean Gate is shown

a. Determine the Boolean output Y

b. Is the static power dissipation of this gate zero?

(use the switch-level model of the MOSFET)



And the number is ….

1 8 7 5 3

6 9 4 2

Quiz 4

A proposed three-input Boolean Gate is shown

a. Determine the Boolean output Y

b. Is the static power dissipation of this gate zero?

(use the switch-level model of the MOSFET)

Solution:

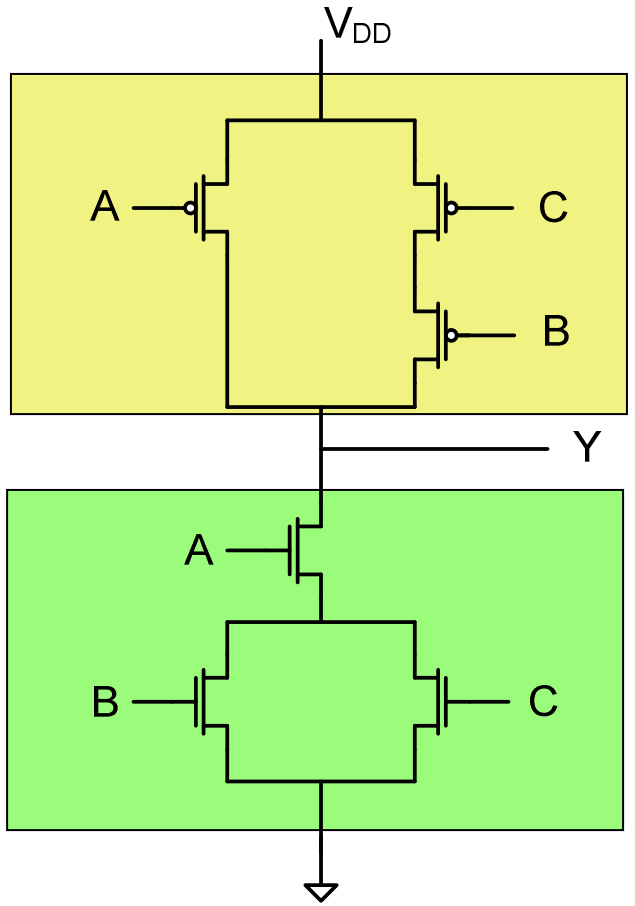
a) From PDN observe

$$\mathbf{Y} = \overline{\mathbf{A} \bullet (\mathbf{B} + \mathbf{C})}$$

In standard Sum of Products form

$$\mathbf{Y} = \overline{\mathbf{A}} + \overline{\mathbf{B}} \bullet \overline{\mathbf{C}}$$

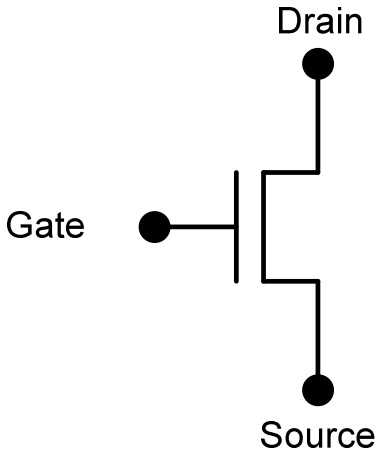
b) Yes – note PU and PD networks are never both conducting

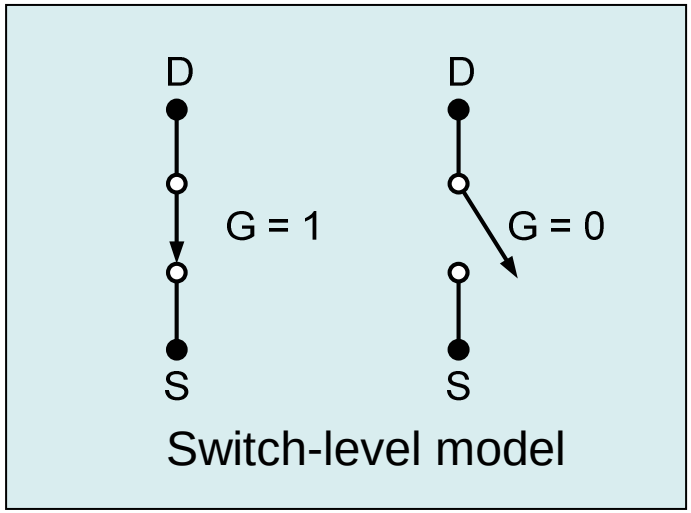


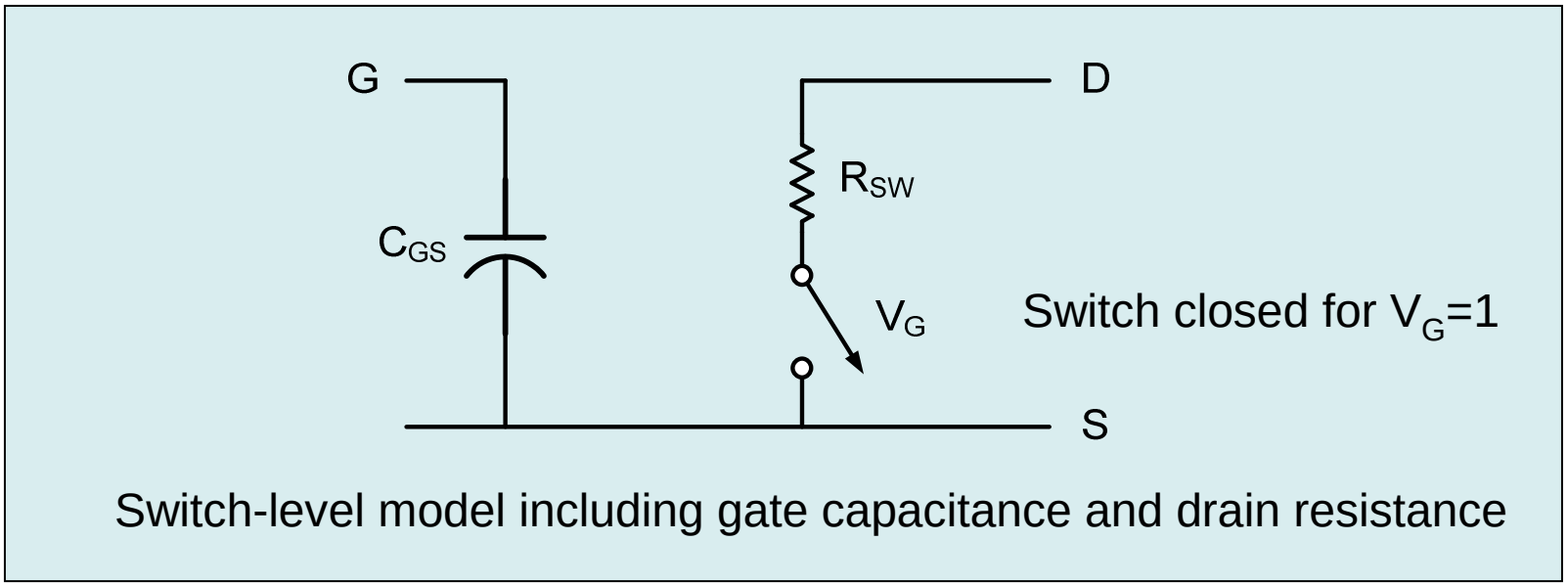
Review from Last Time

- Different Logic Design Styles Can Be Used
  - PTL is one style that can offer significant reductions in complexity
  - Signal Degradation and Static Power Dissipation are issues of concern when using PTL
  - Designer is under complete control of circuits that are placed on the silicon
  - Many designs will mix multiple logic design styles
  - New logic design styles are still being proposed and adopted

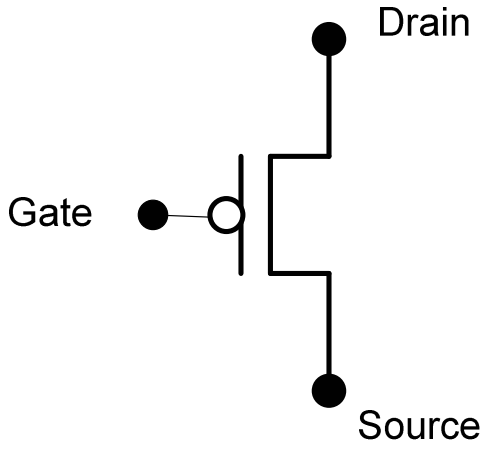
Improved Switch-Level Model

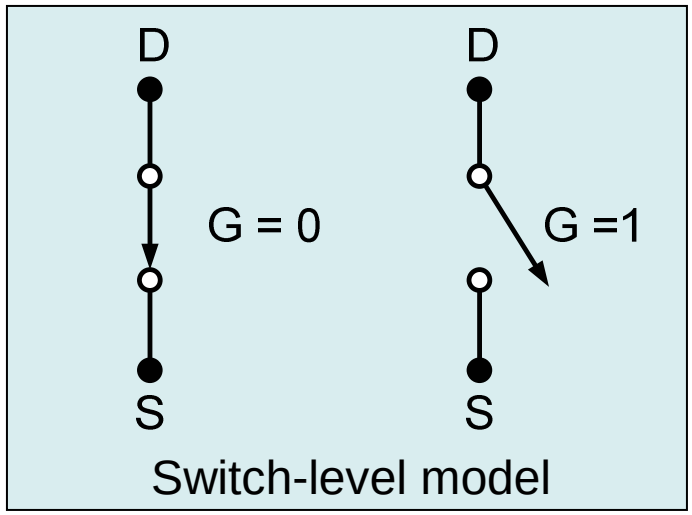


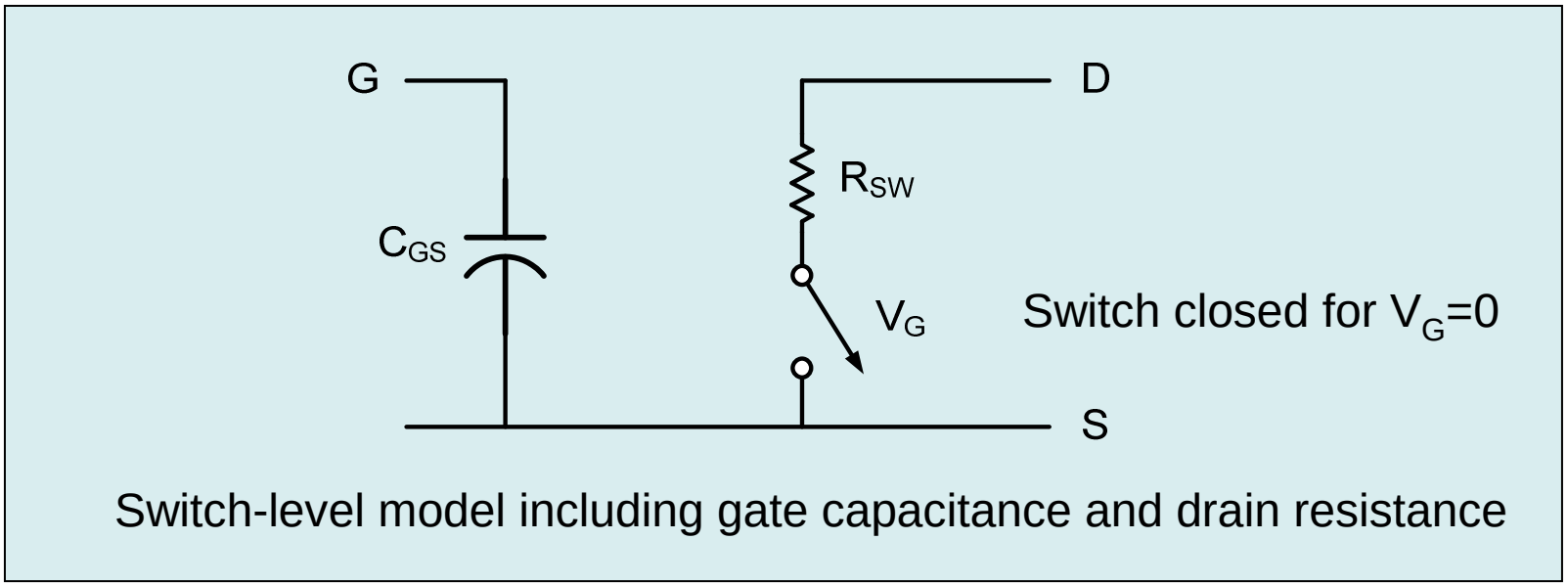




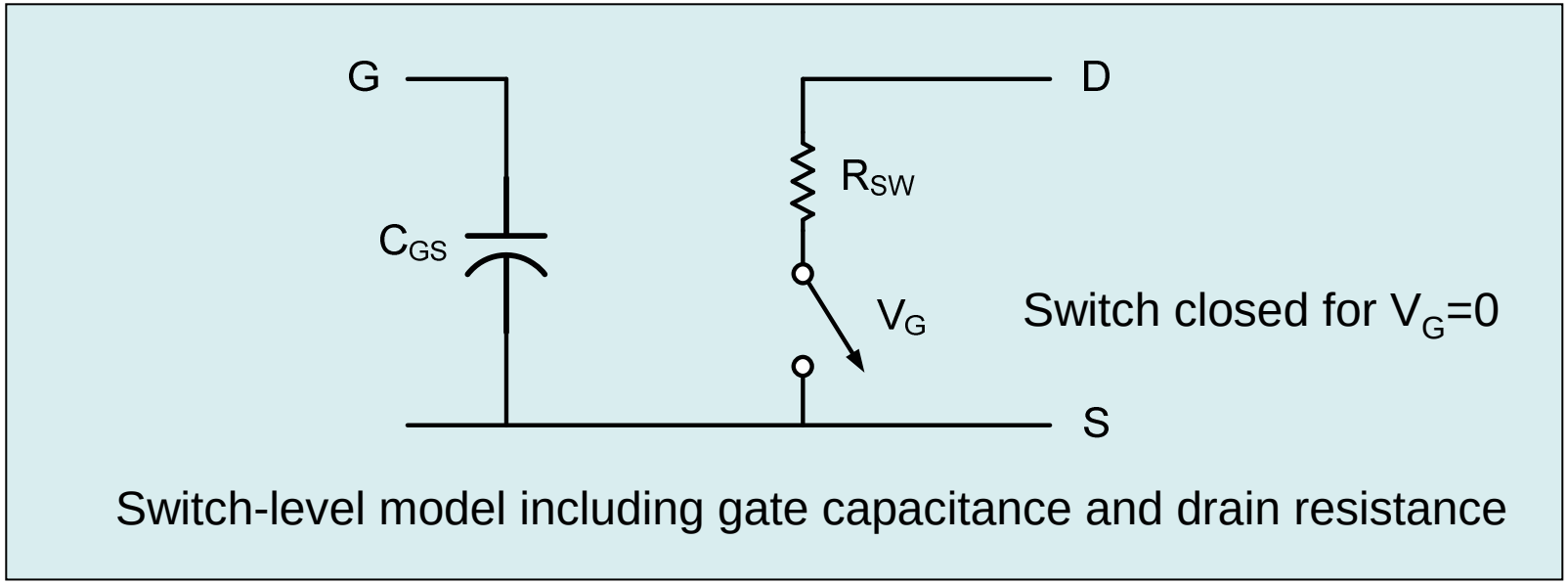
Improved Switch-Level Model







Improved Switch-Level Model



Switch-level model including gate capacitance and drain resistance

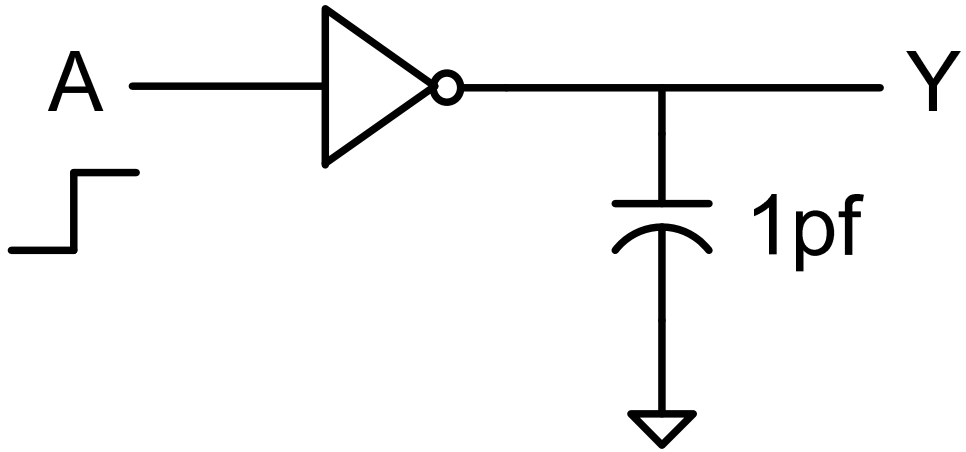
C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

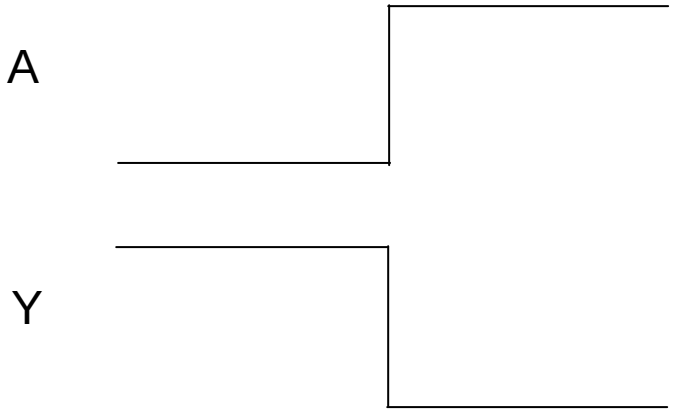
$$\mathbf{C_{GS} \cong 1.5fF} \qquad \mathbf{R_{sw}} \cong \begin{cases} \mathbf{2K\Omega \;\; n-channel} \\ \mathbf{6K\Omega \;\; p-channel} \end{cases}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

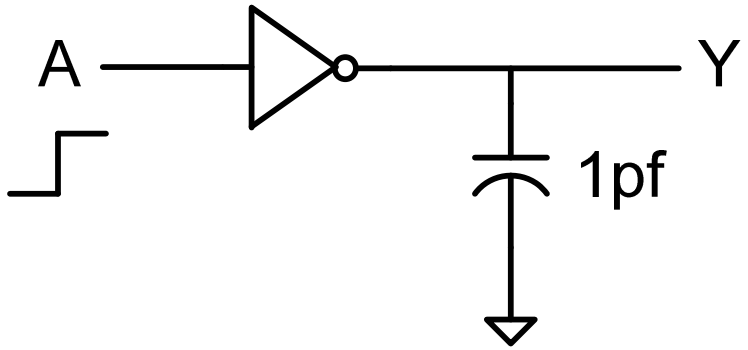
Example



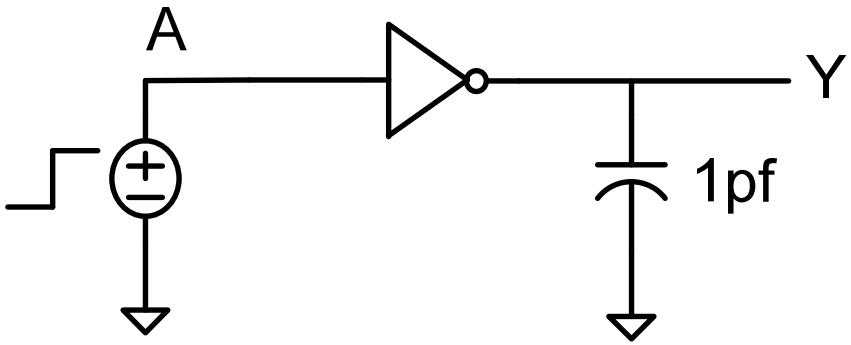
With switch level model



Example (cont)

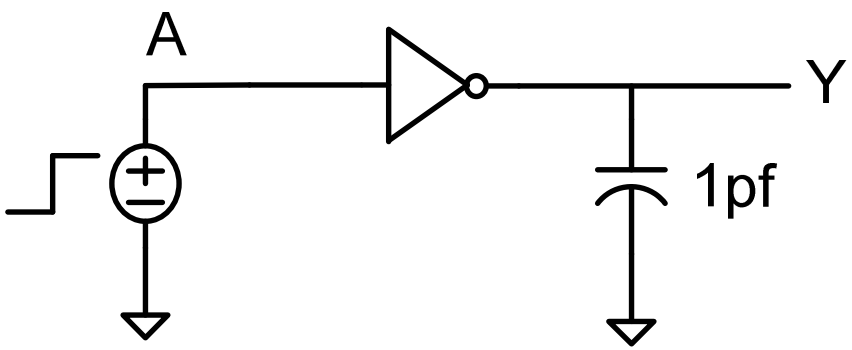


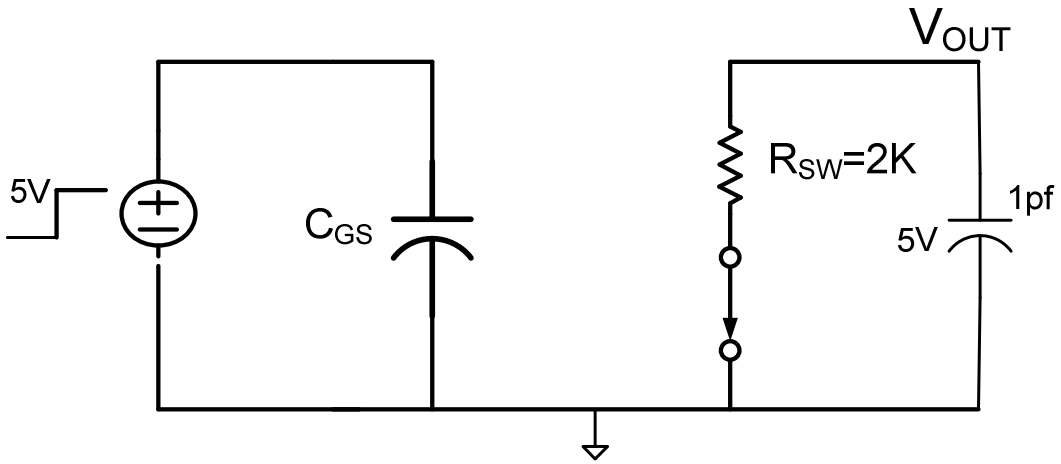
With improved model



Example (cont)

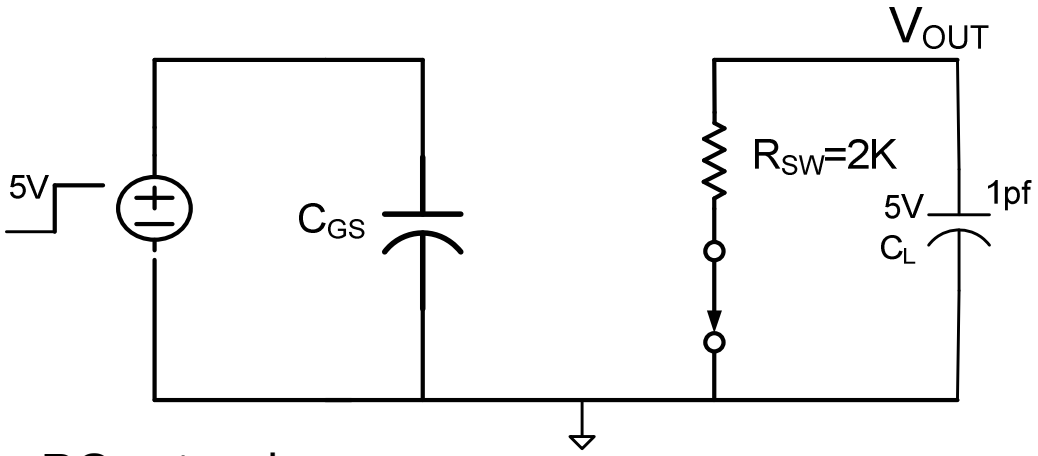
With improved model





Example (cont)

With improved model



Recognize as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

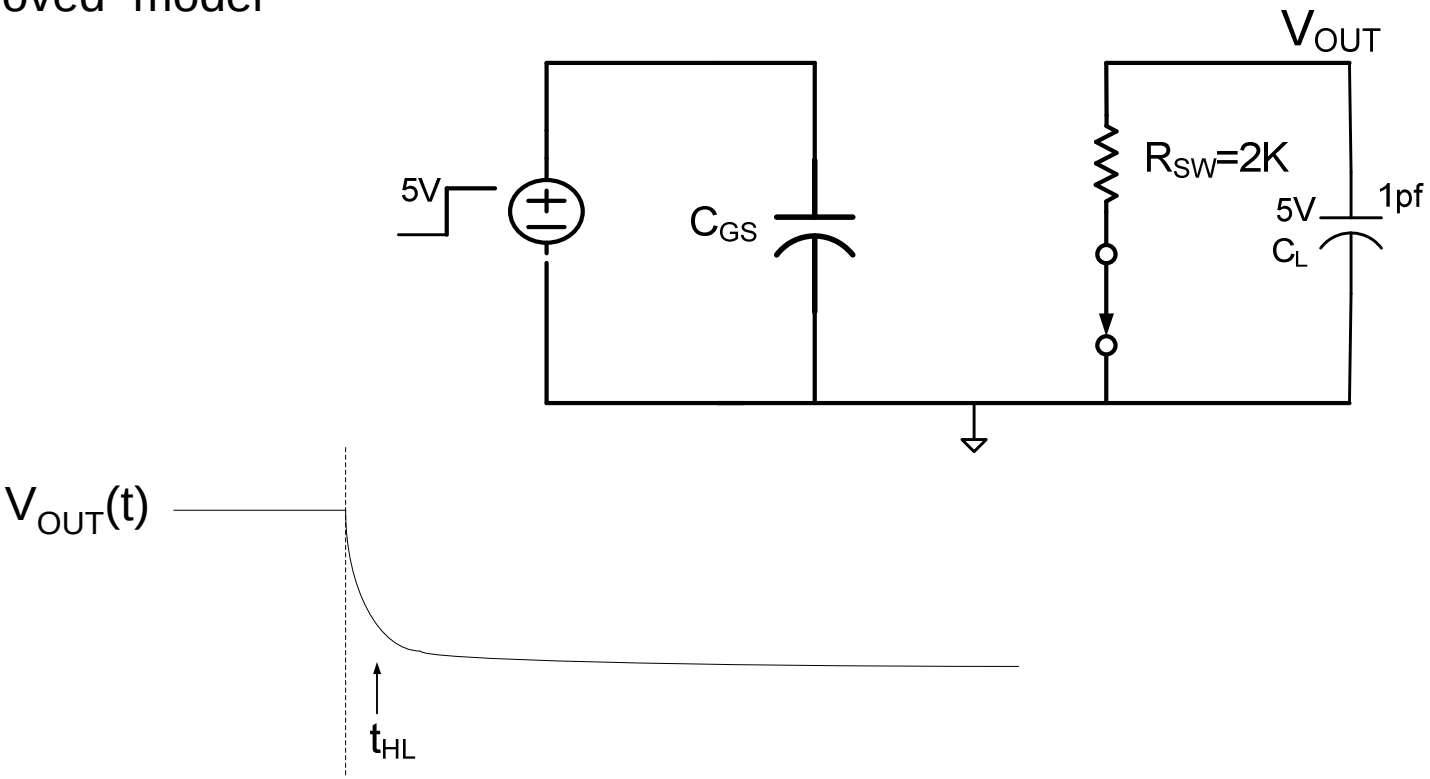
$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

where F is the final value, I is the initial value and τ is the time constant of the circuit

For the circuit above, F=0, I=5 and $\tau = R_{SW}C_L$

Example (cont)

With improved model

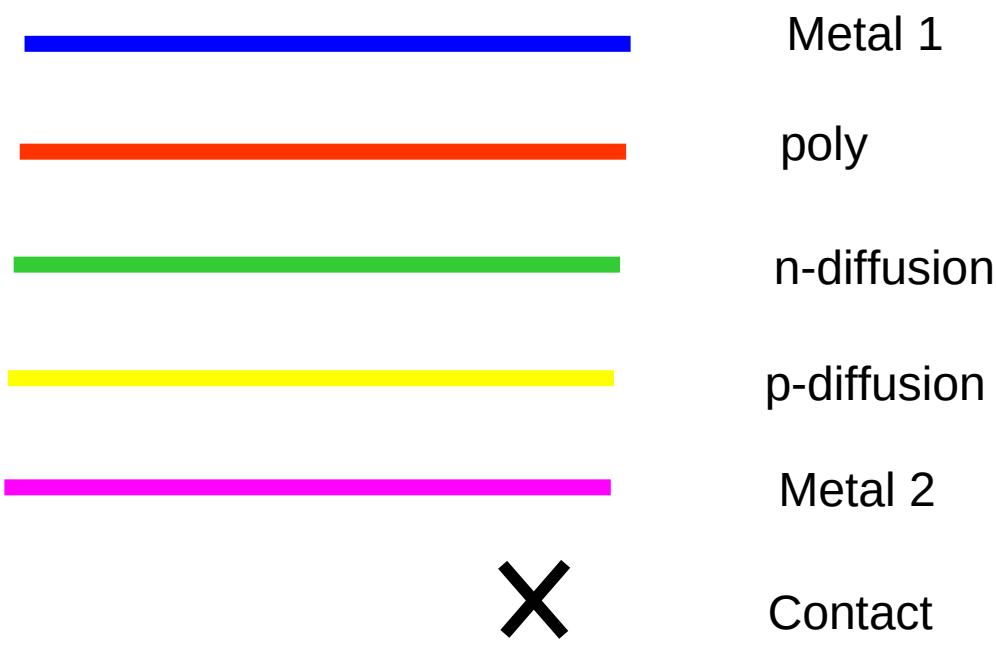


$$t_{HL} \cong R_{SW} C_L \quad = 2K \bullet 1pF = .5E-9\,\text{sec} = .5n\,\text{sec}$$

Stick Diagrams

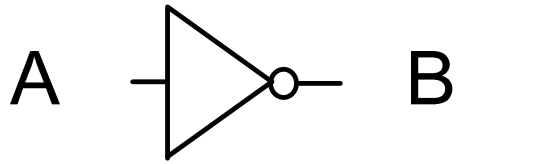
- It is often necessary to obtain information about placement, interconnect and physical-layer structure
- Stick diagrams are often used for small component-count blocks
- Approximate placement, routing, and area information can be obtained rather quickly with the use of stick diagrams

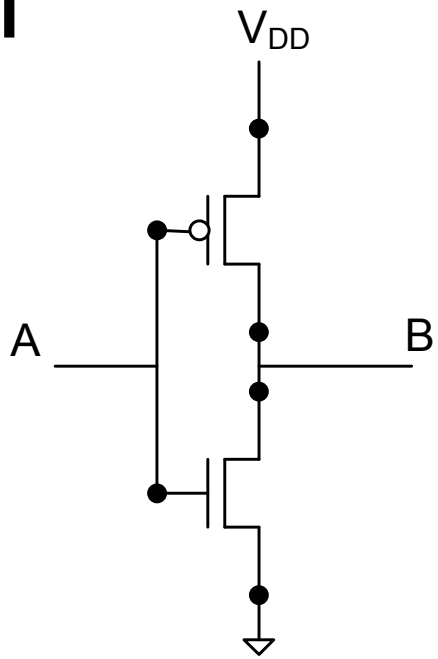
Stick Diagrams

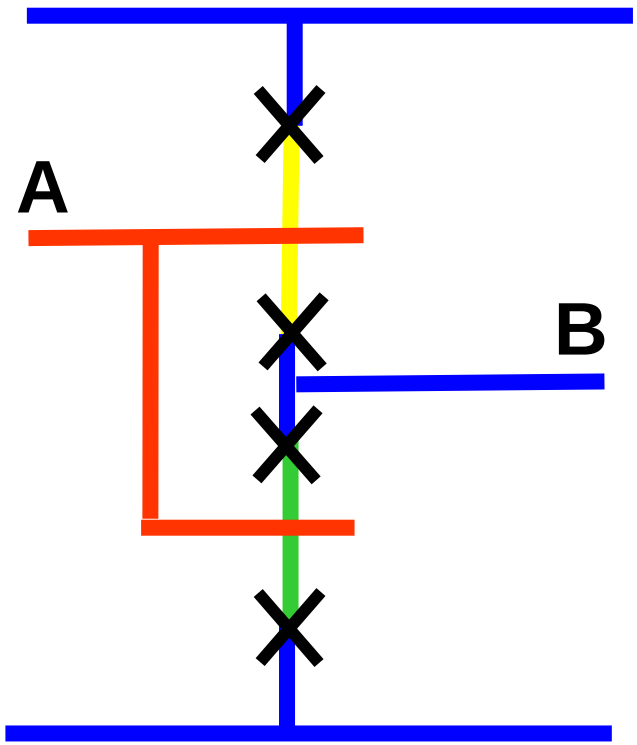


Additional layers can be added and color conventions are peronal

Stick Diagram





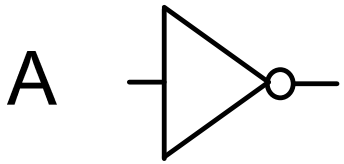


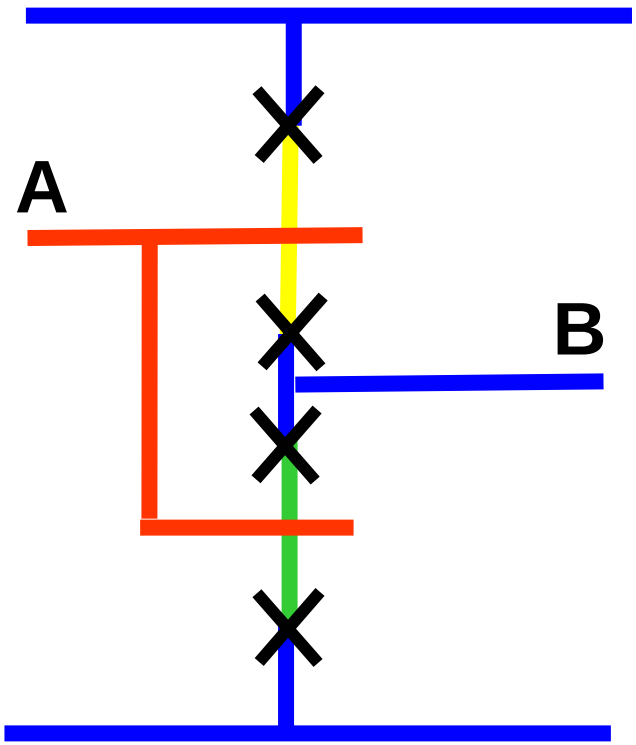
A stick diagram is not a layout but gives the basic structure that will be instantiated in the actual layout itself

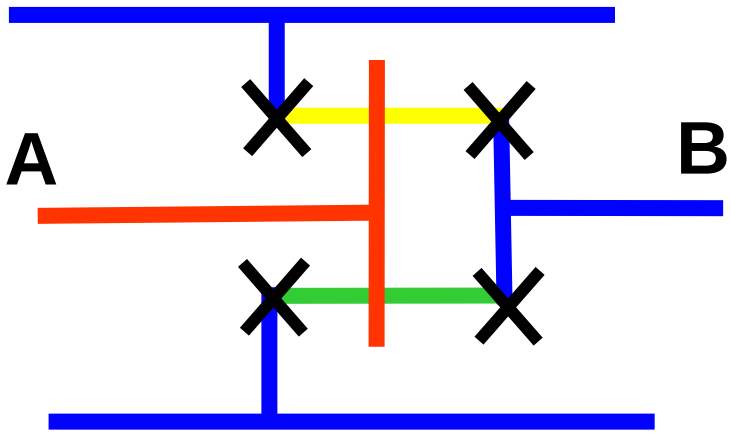
Modifications can be made much more quickly on a stick diagram than on a layout

Iteration may be needed to come up with a good layout structure

Stick Diagram







Alternate Representation