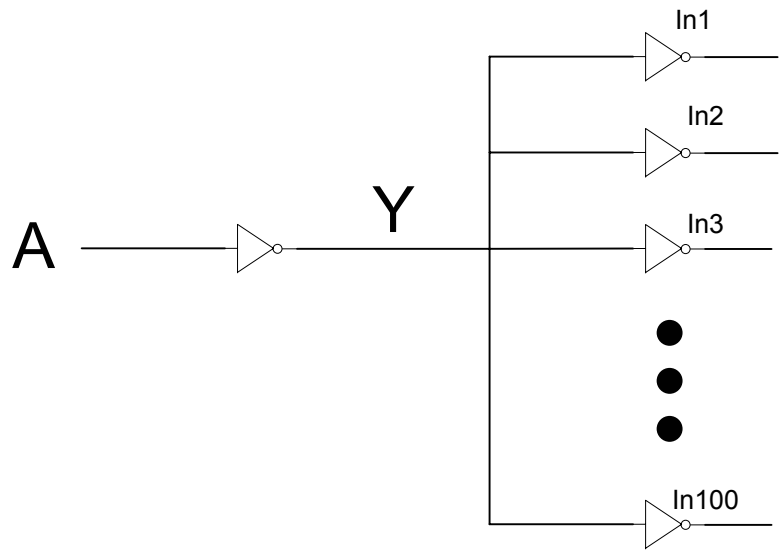
EE 434
Lecture 7

Technology Files

Quiz 5

A CMOS inverter is driving a 100 CMOS inverters. Determine the rise and fall times at the output of this inverter if the input is driven by an ideal square wave. Assume the n-channel transistors in the inverters are modeled with an improved switch-level model with input capacitance of 20fF and a channel resistance of 1KΩ and the p-channel resistors use the same model but with corresponding parameters of 50fF and 2K Ω .



And the number is ….

1 8 7 5 3

6 9 4 2

Quiz 5

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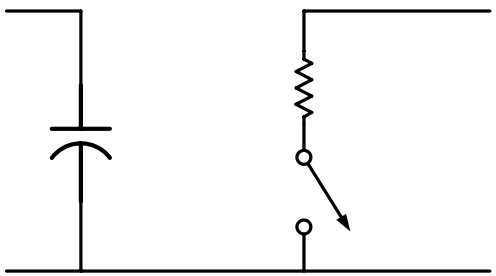
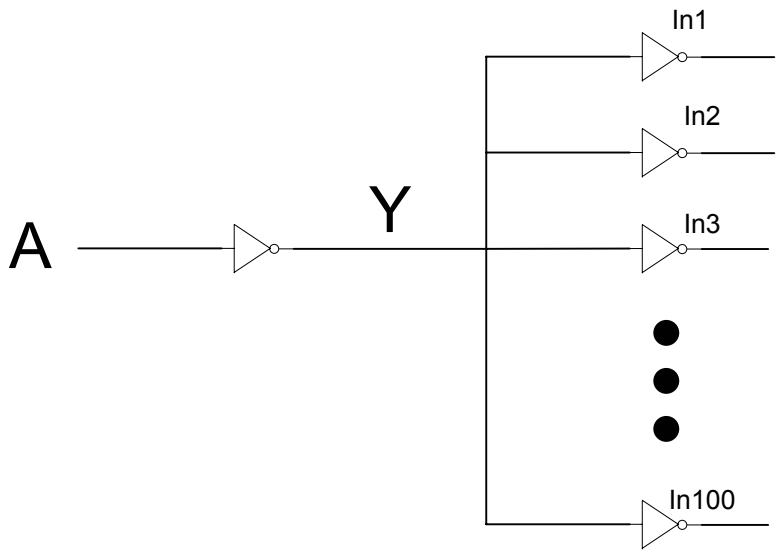
Solution:



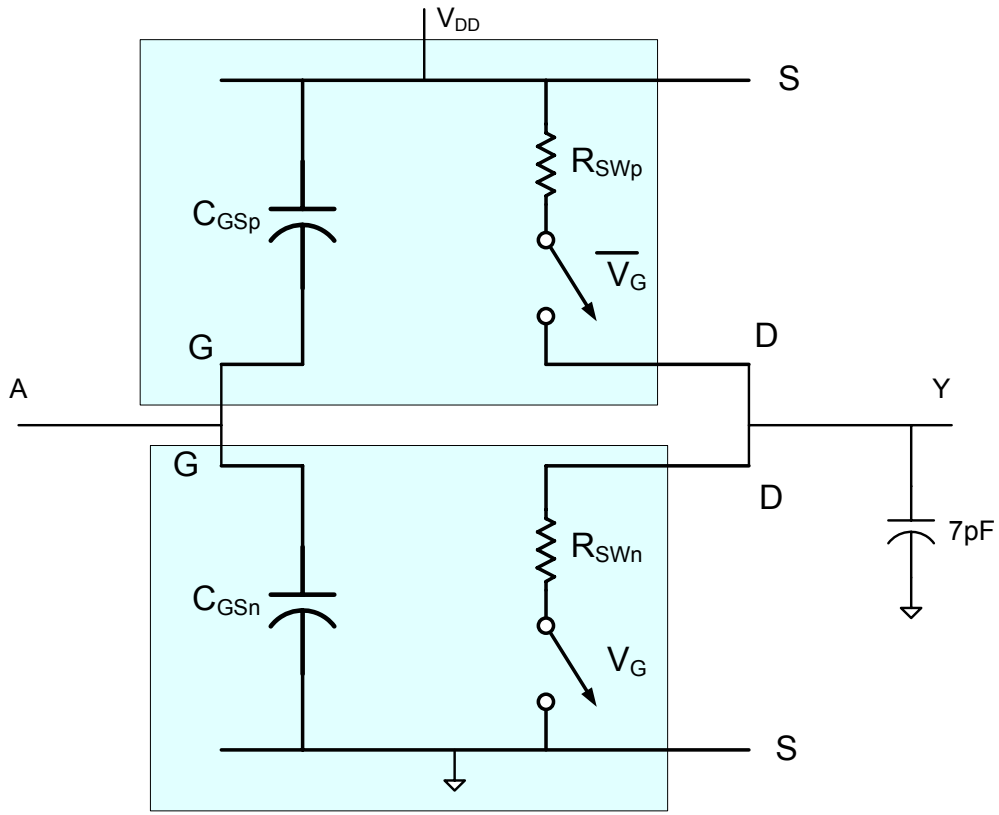
Improved switch-level model



C_L=100(20ff+50ff)=7pf

Quiz 5

Solution:



$$t_{HL} \cong R_{SWn} C_L = 1K \bullet 7pF = 7nsec$$

$$t_{LH} \cong R_{SWp} C_L = 2K \bullet 7pF = 14nsec$$

Review from Last Time

- Improved switch-level model can be used to predict rise and fall times in digital circuits
- Stick diagrams often useful for determining placement and routing strategies
  - Gives insight
  - Not included as a cell view in integrated tool flows

Technology Files

- Provide Information About Process
  - Process Flow
  - Model Parameters
  - Design Rules
- Serve as Interface Between Design Engineer and Process Engineer
- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries

Technology Files

- Process Flow (will discuss next week)
- Model Parameters (will discuss in detail after device models are introduced)
- Design Rules

Design Rules

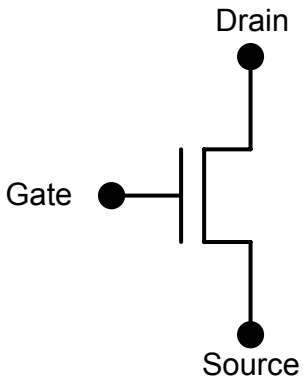
- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

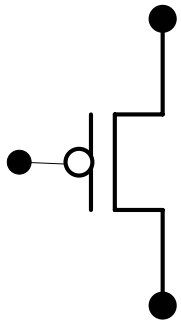
- Very large number of devices can be reliably made with the design rules of a process

- Yield and performance unpredictable and often low if rules are violated

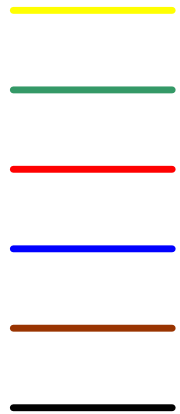
- Compatible with design rule checker in integrated toolsets

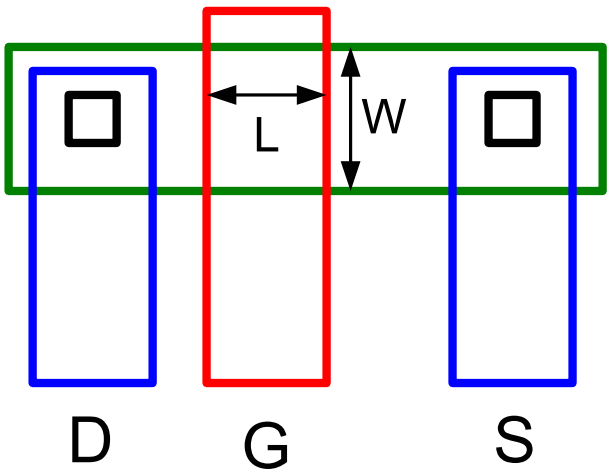
Design Rules – consider transistors



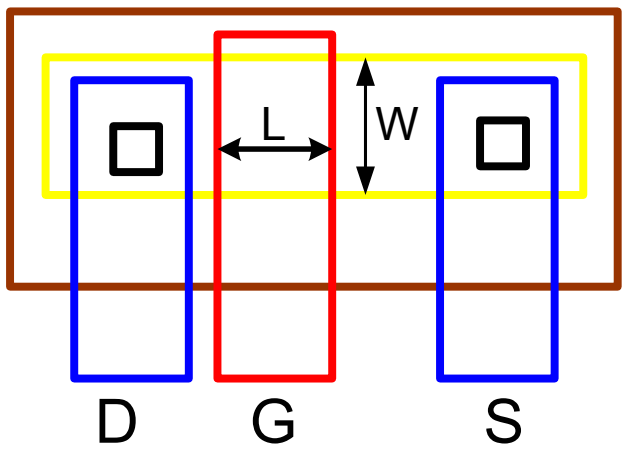


Layer Map





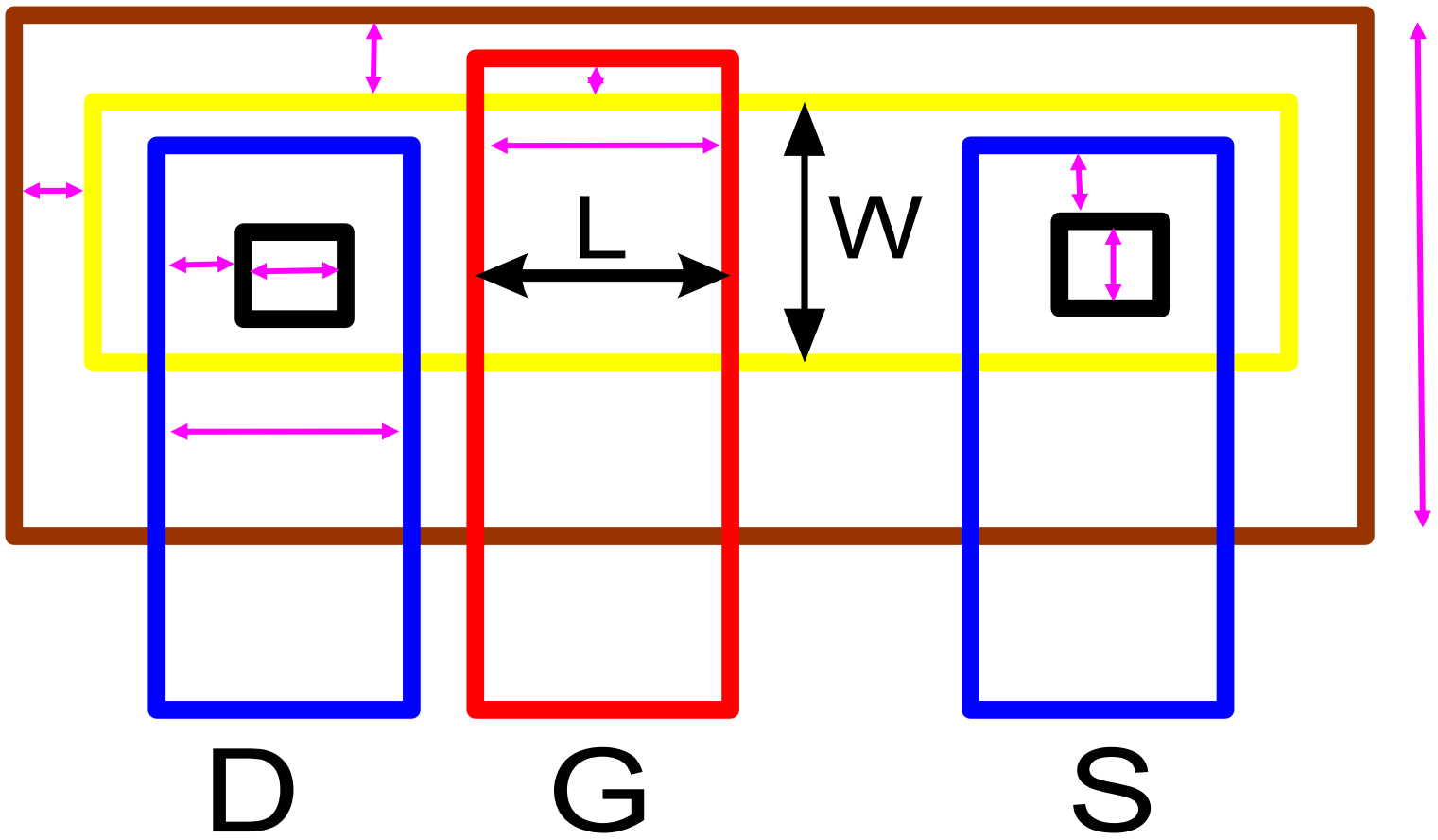
Layout



Layout

Layout always represented in a top view in two dimensions

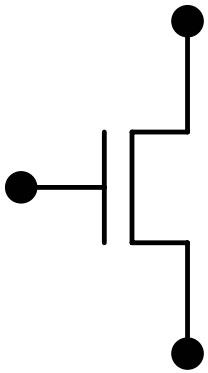
Design Rules

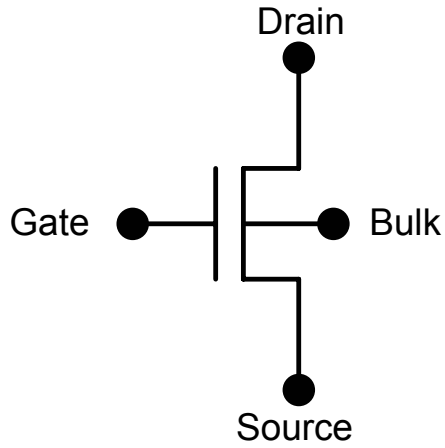


Design rules give minimum feature sizes and spacings

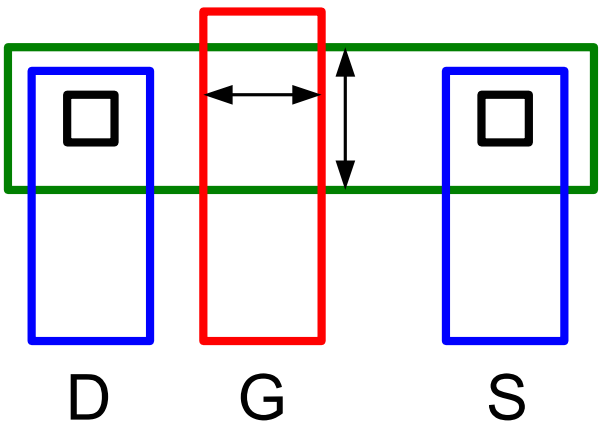
Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)

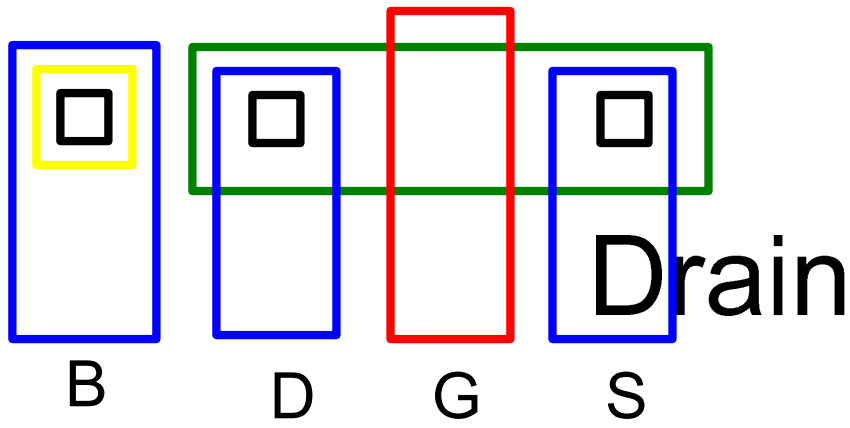
Design Rules – consider transistors





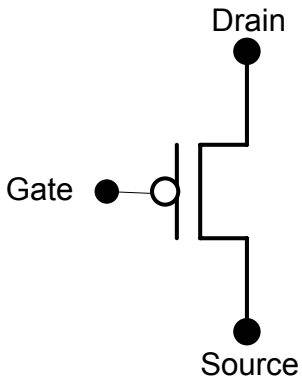
Layer Map

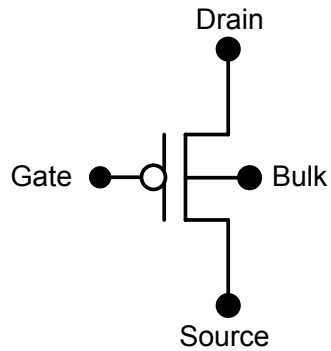




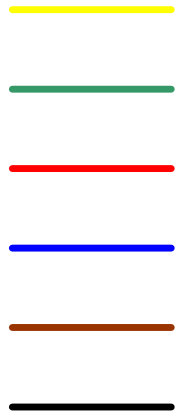
- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors**

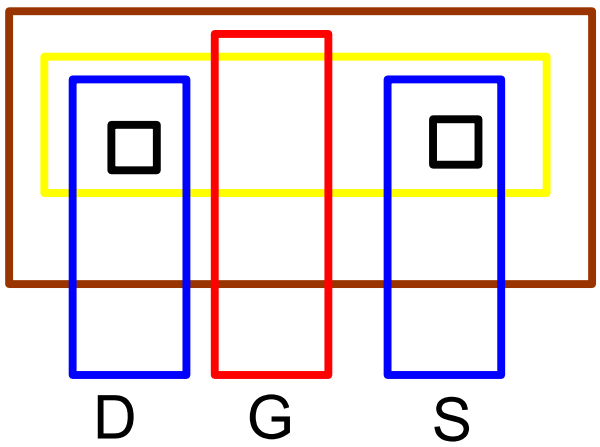
Design Rules – consider transistors

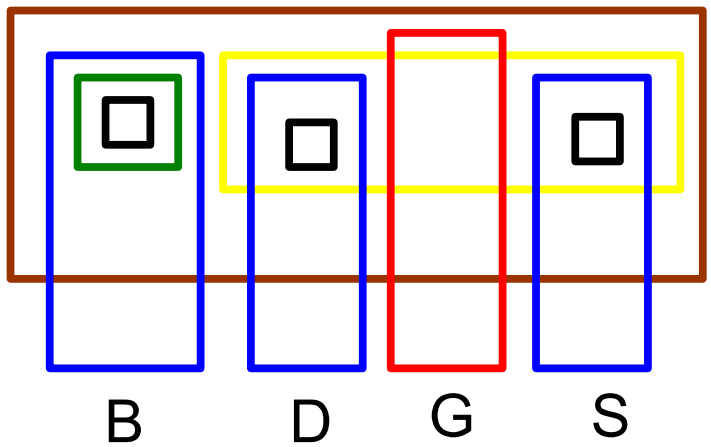




Layer Map

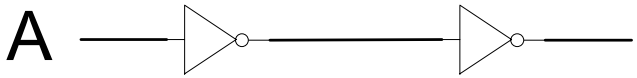




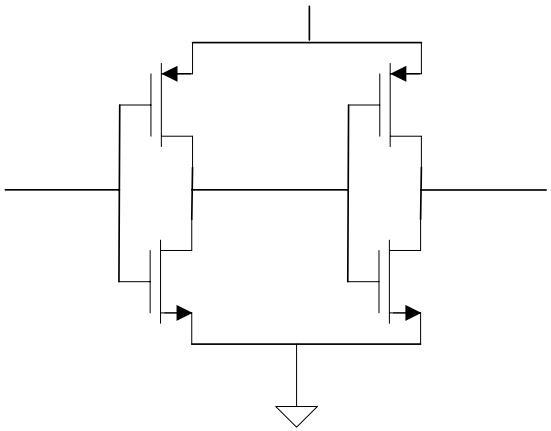


- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors is they share the same well**

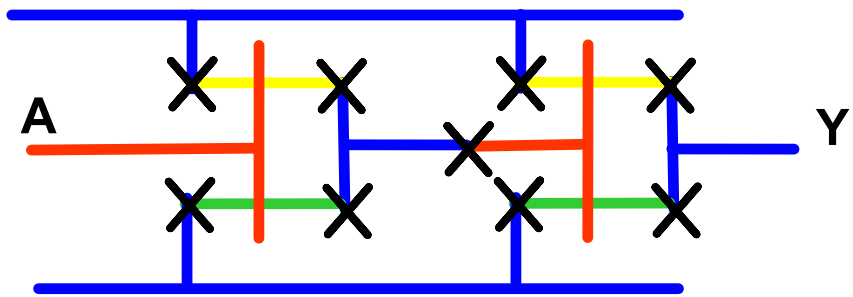
Design Rules (example)



Logic Circuit

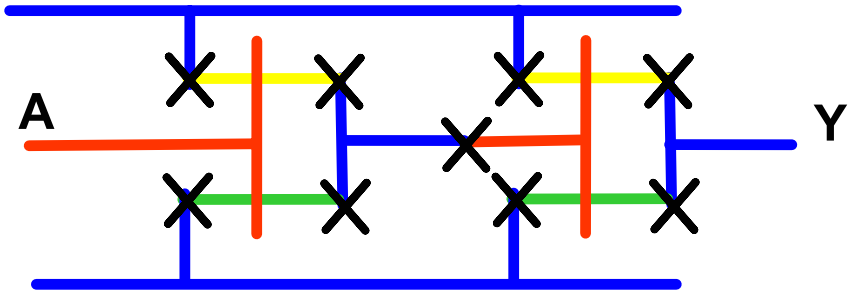


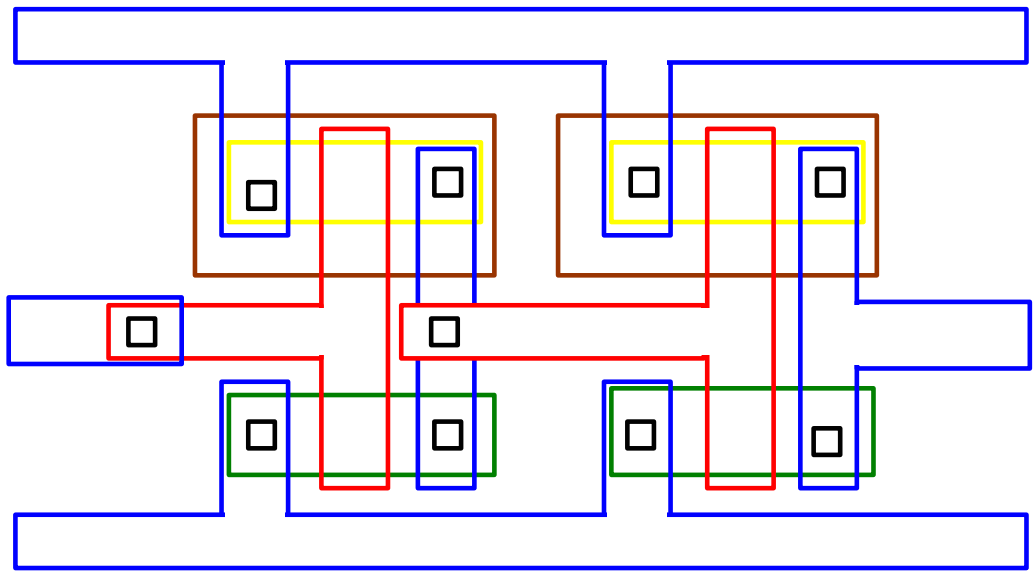
Circuit Schematic (Including Device Sizing)



Stick Diagram

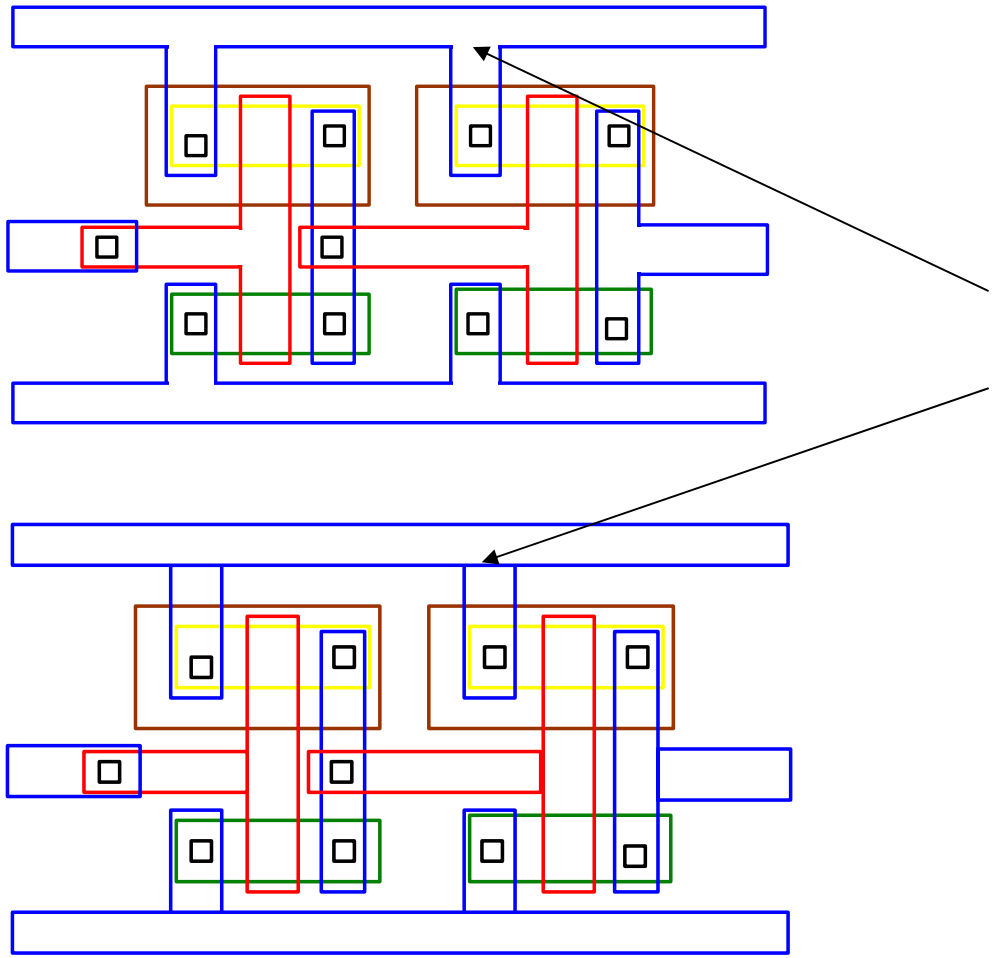
Design Rules (example)





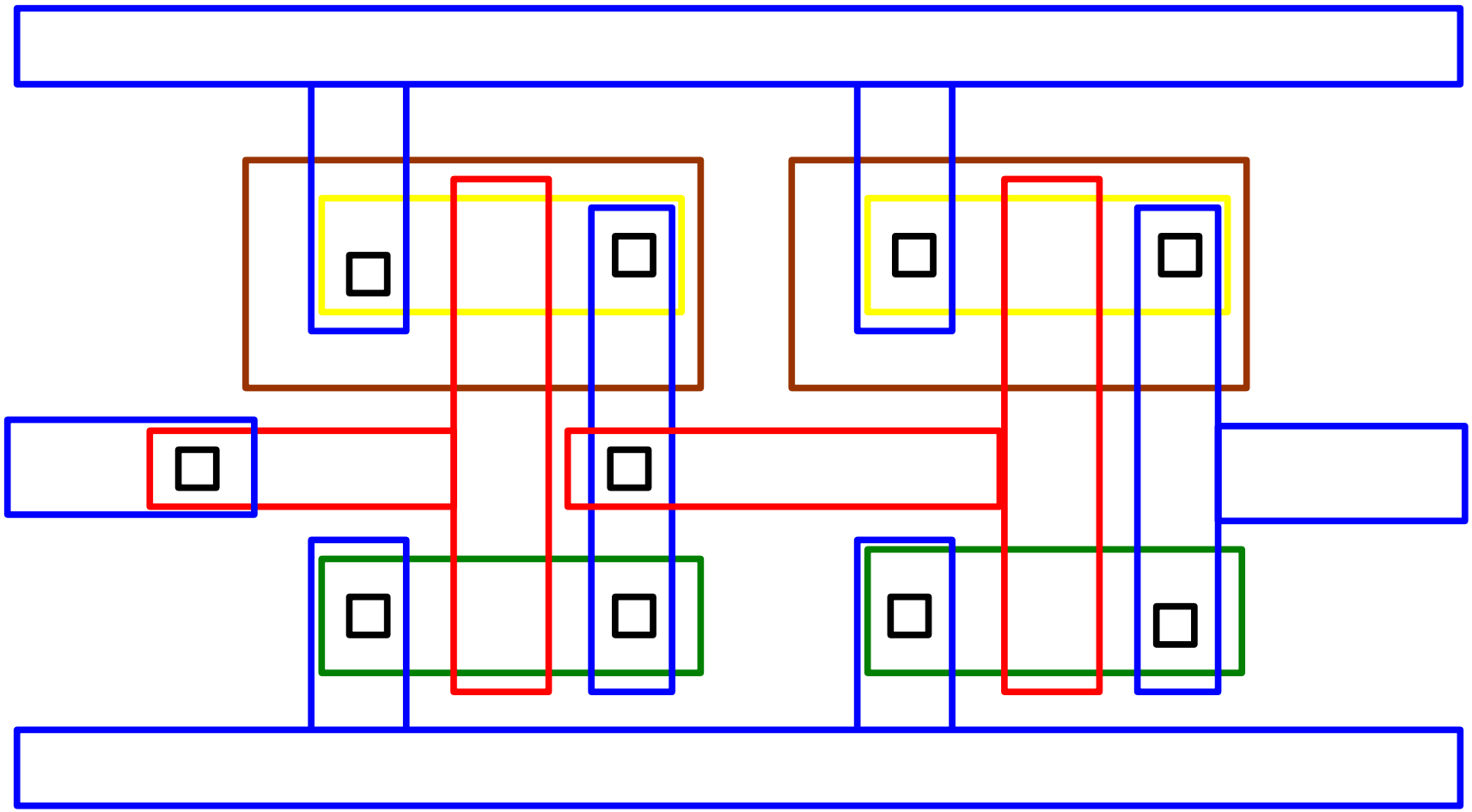
Layout

Design Rules (example)



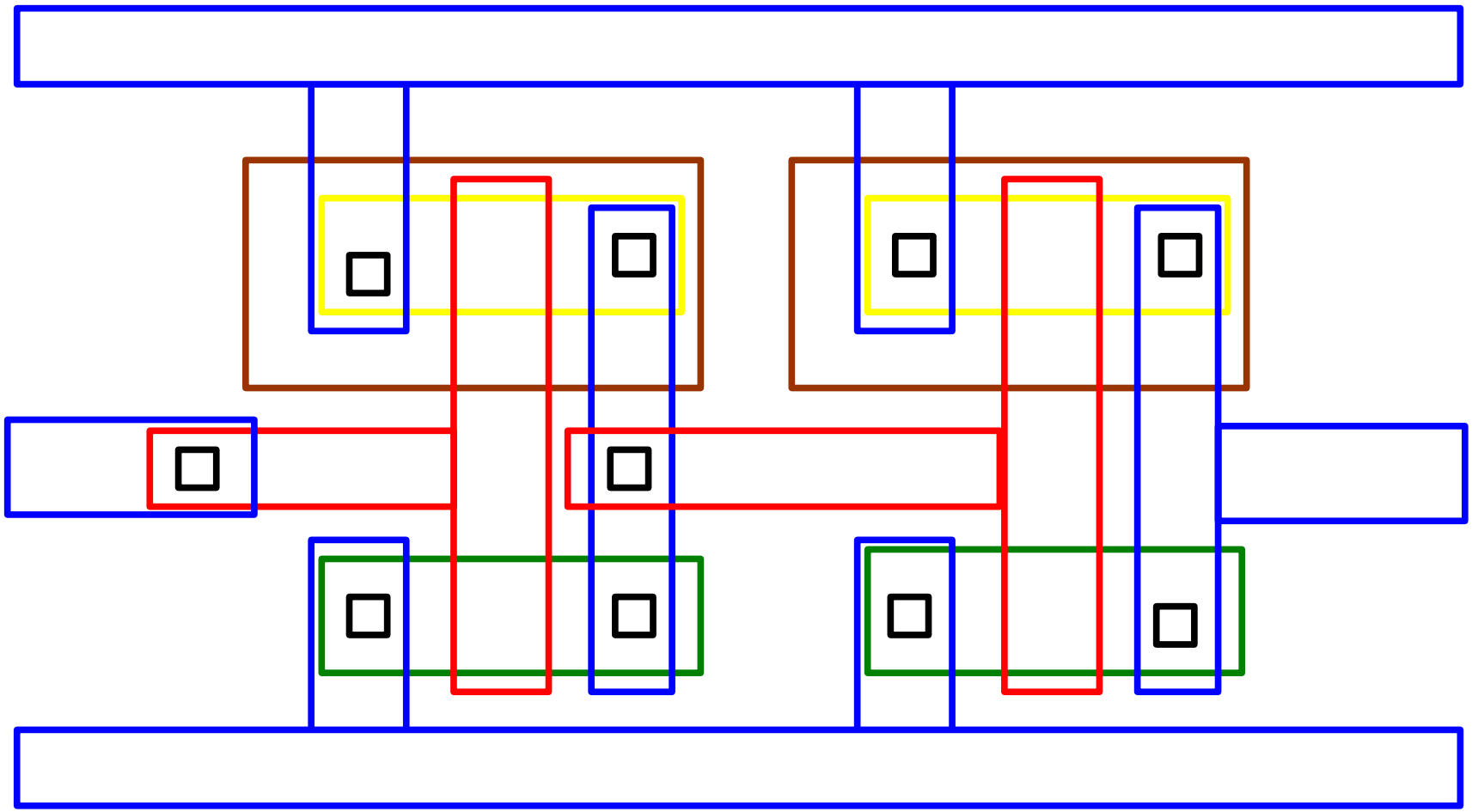
- Polygons merged in Geometric Description File (GDF)
- Separate rectangles generally more convenient to represent

Design Rules (example)



- Design rules must be satisfied throughout the design
- DRC runs incrementally during layout in most existing tools to flag most problems
- DRC can catch layout errors but not circuit design errors

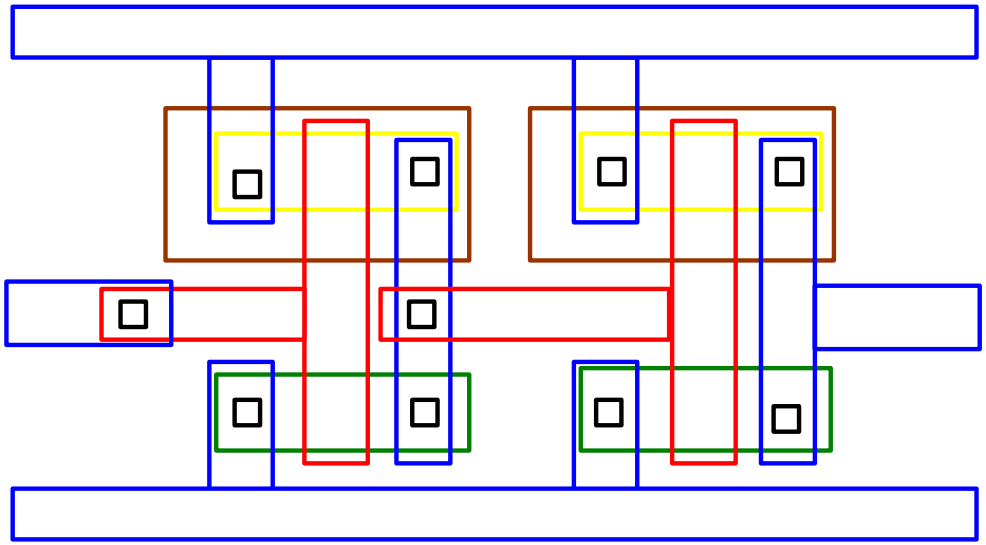
Design Rules (example)



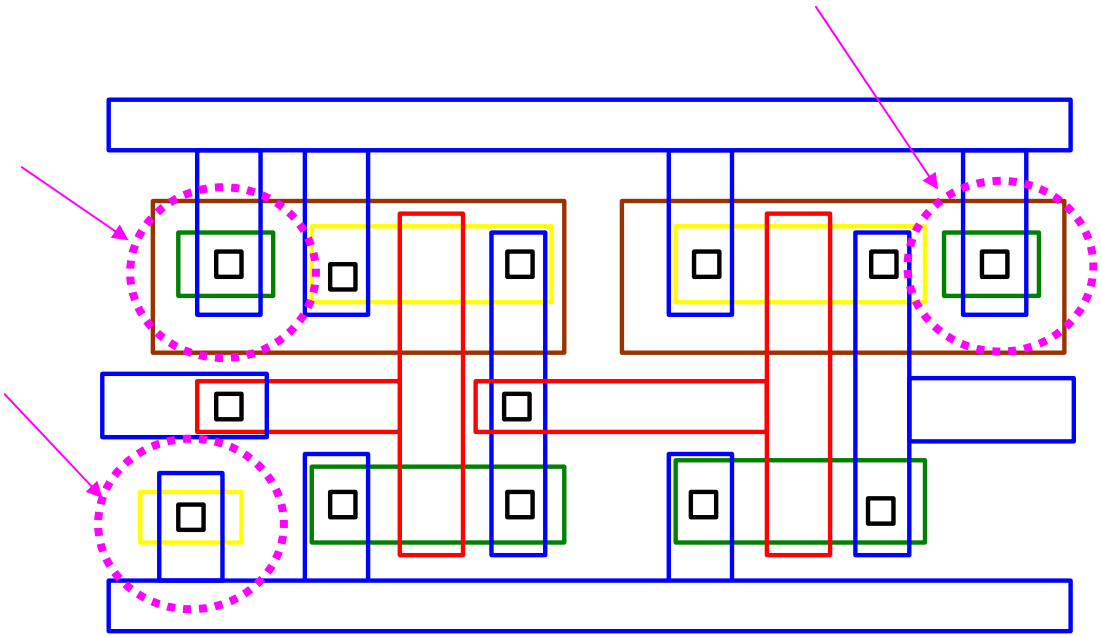
What is wrong with this layout ?

Bulk connections missing!

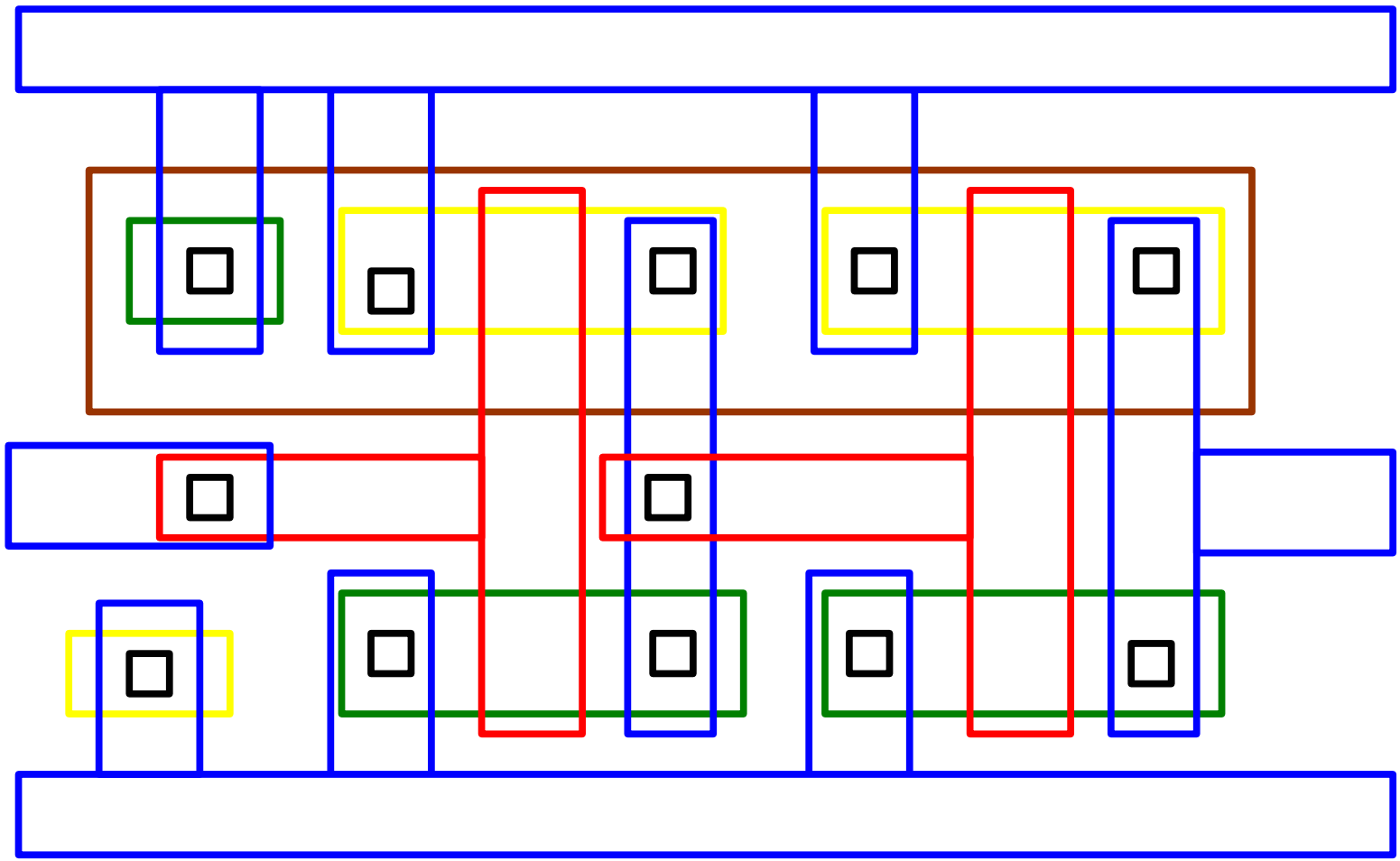
Design Rules (example)



- Note diffusions needed for bulk connections
- Note p-well connections increase area a significant amount
- Note p-wells are both connected to V_{DD} in this circuit

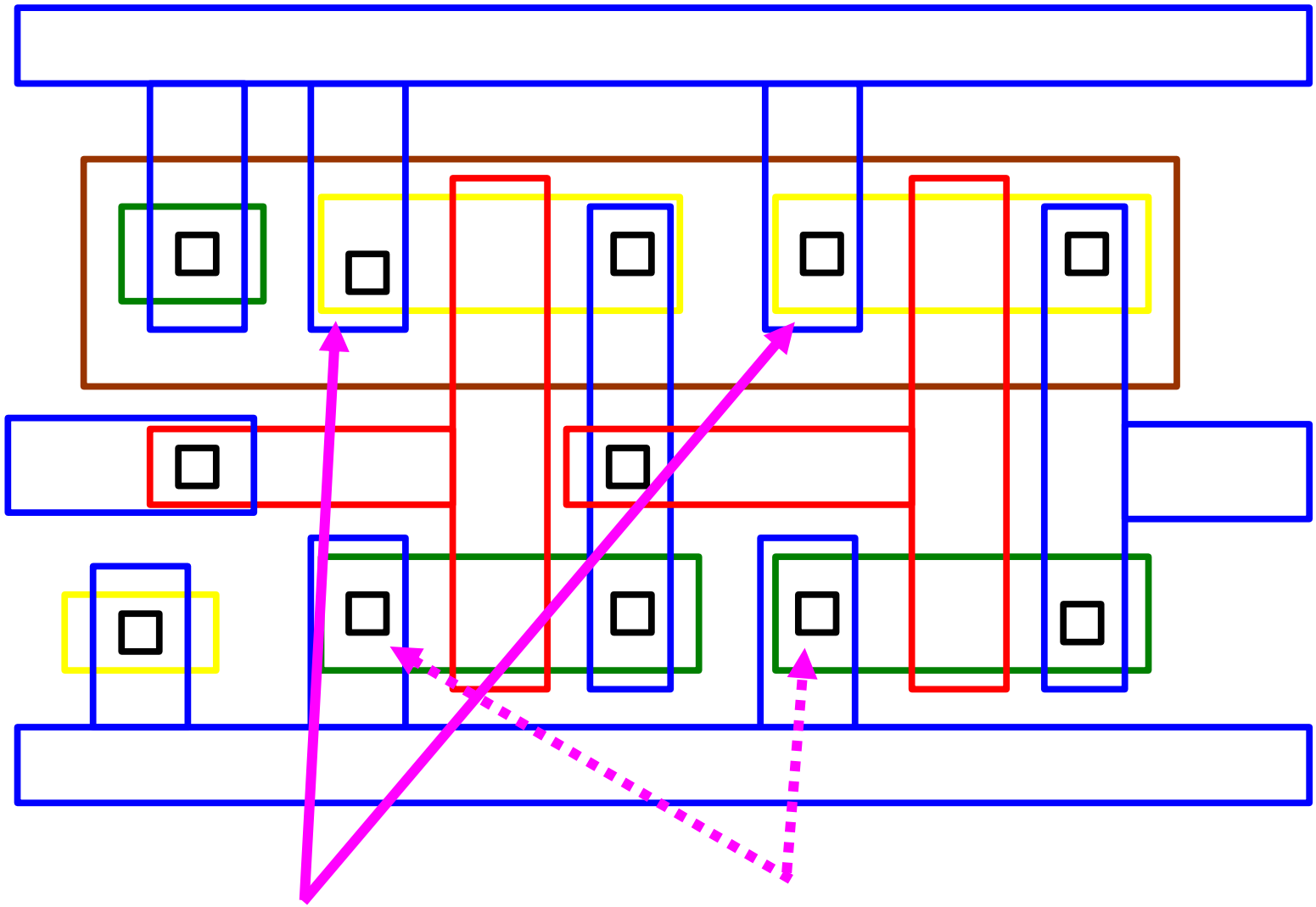


Design Rules (example)



Layout with shared p-well reduces area

Design Rules (example)



Shared p-active can be combined to reduce area

Shared n-active can be combined to reduce area

Design Rules

- Design rules can be given in absolute dimensions for every rule
- Design rules can be parameterized and given relative to a parameter
  - Makes movement from one process to another more convenient
  - Easier for designer to remember
  - Some penalty in area efficiency
  - Often termed λ-based design rules
  - Typically λ is ½ the minimum feature size in a process

Design Rules

- See www.MOSIS.org for design rules

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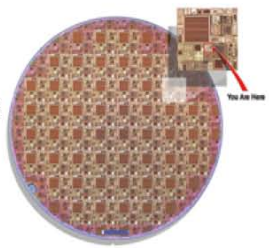

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Vendors consider their rules, process specifications, and SPICE parameters proprietary and make them available to MOSIS commercial account holders in different ways.

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- See www.MOSIS.org for design rules
- Some of these files are on class WEB site
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