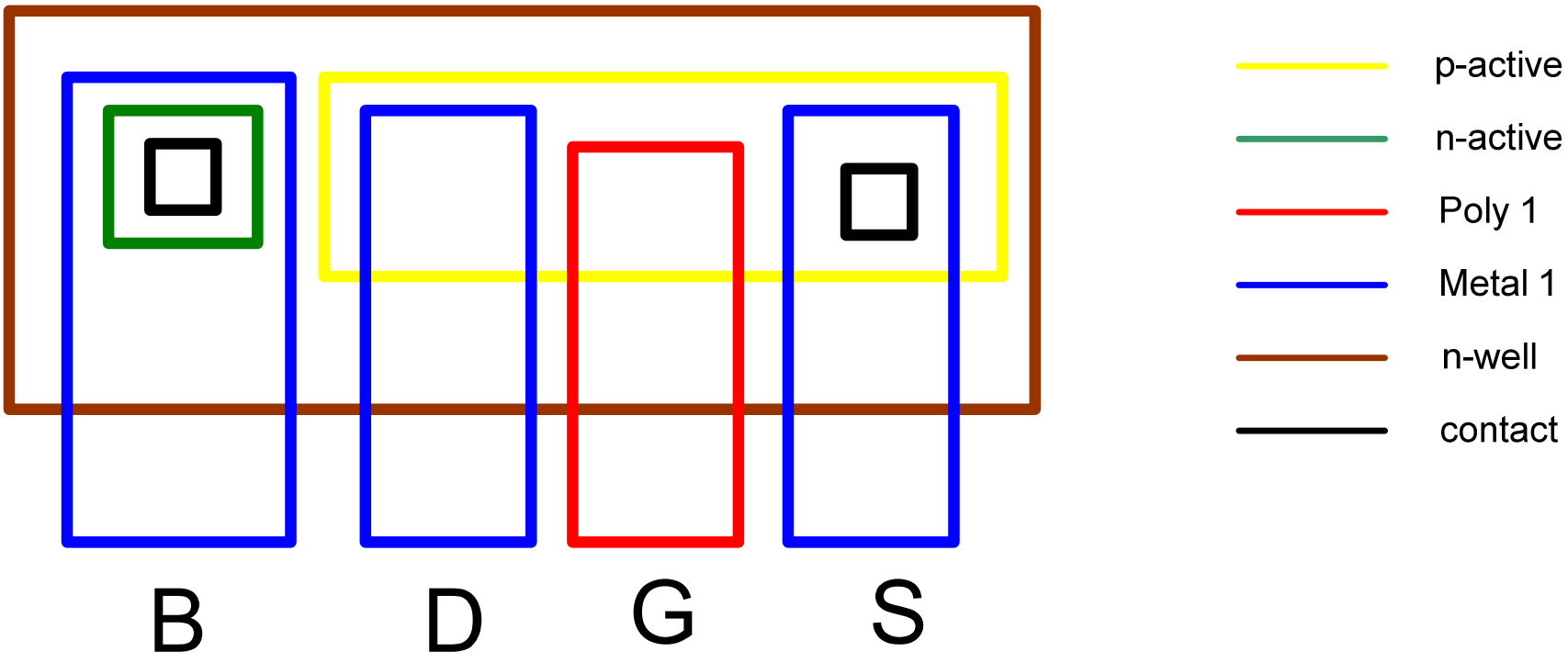
EE 434
Lecture 8

IC Fabrication Technology

Quiz 6

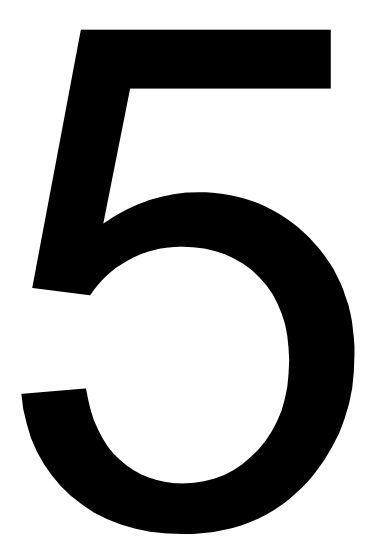
The layout of a p-channel transistor is shown. There are two fundamental errors in this layout. Identify them.



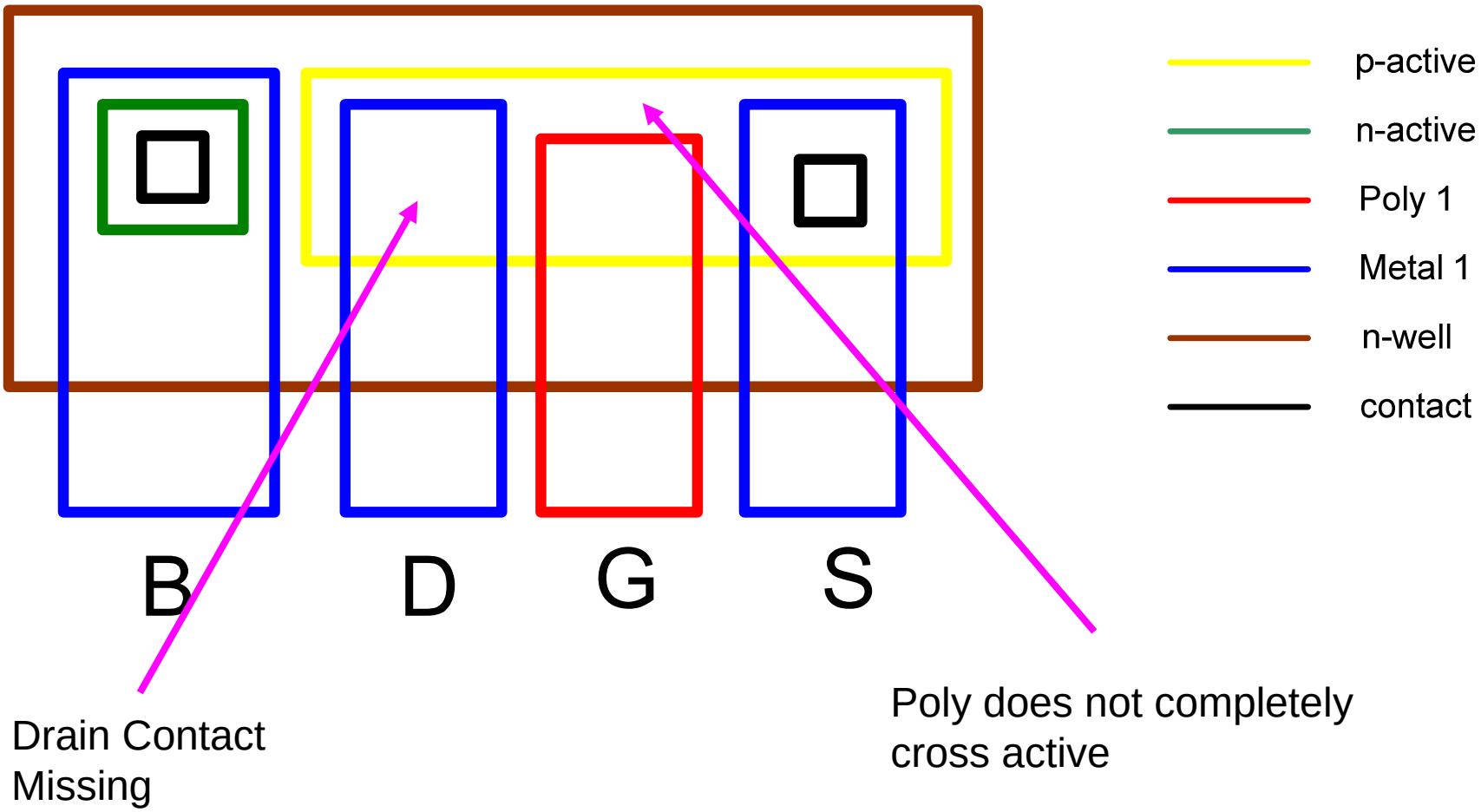
And the number is ….

1 8 7 5 3

6 9 4 2



Quiz 6 Solution



Review from Last Time

- Technology Files Characterizes a Process
  - Process Flow
  - Model Parameters
  - Design Rules
- Design Rules Provide Minimum Size and Spacing Information
  - Usually little benefit from making a design more conservative than design rules specify
  - Design rules imbedded in DRC
  - Avoid violating any design rules
- Geometric Layout Information In Geometric Description File (GDF)
  - GDF corresponds to one cell view in toolset
  - GDF ultimately sent to foundry for fabrication of IC

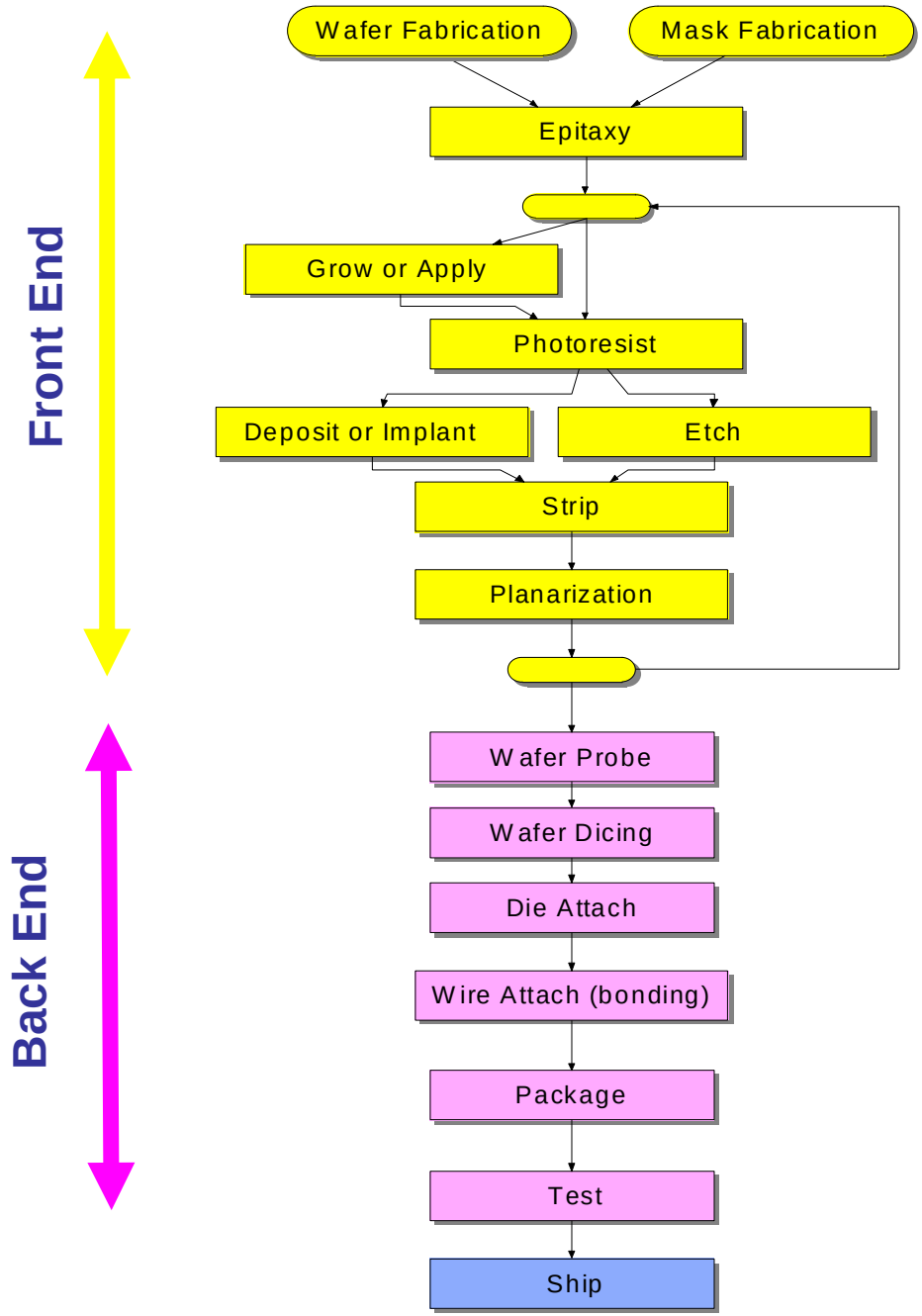
IC Fabrication Technology

See Chapter 1 and 3 of WH
or Chapter 2 GAS for details

IC Fabrication Technology

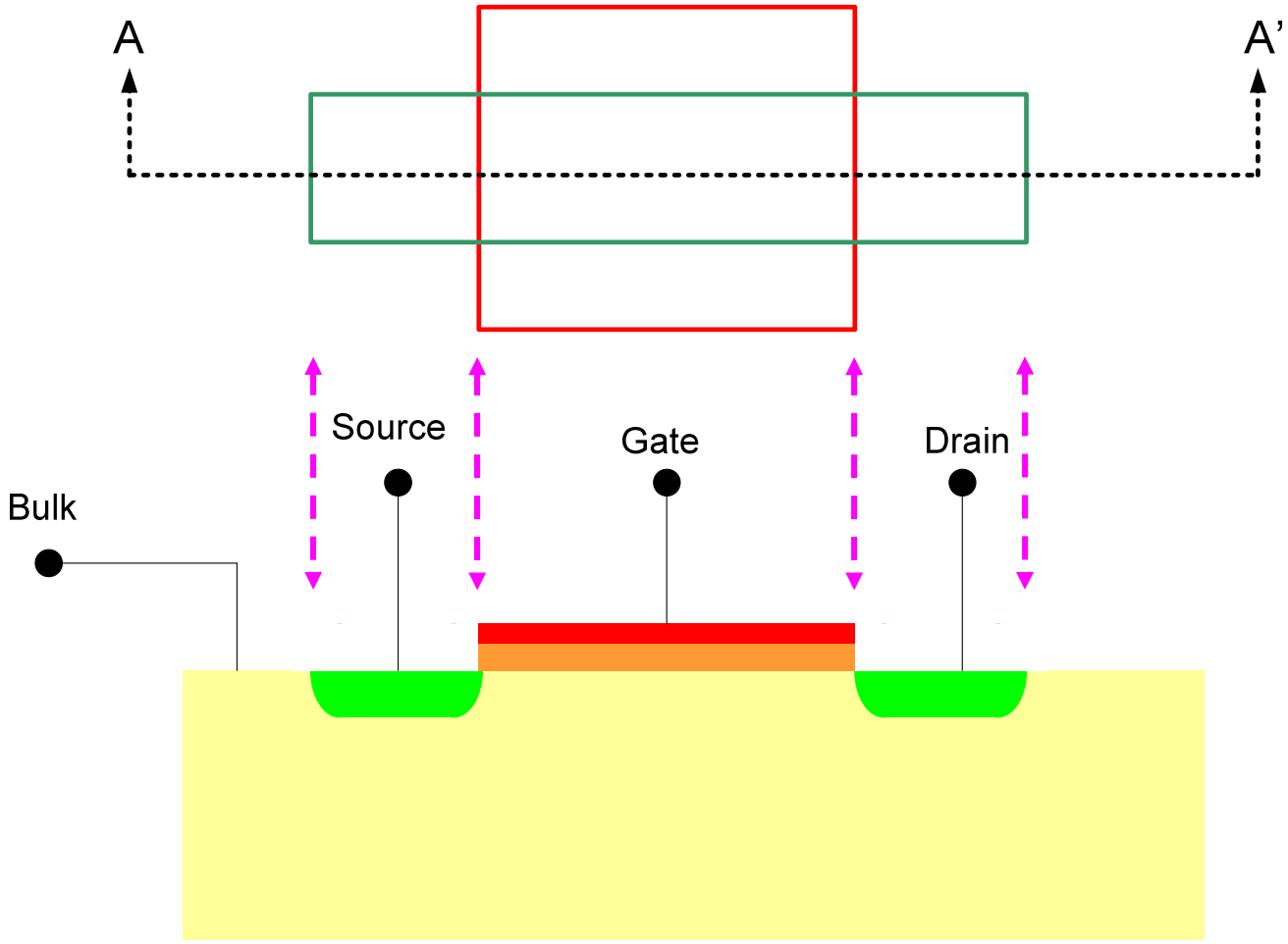
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Generic Process Flow

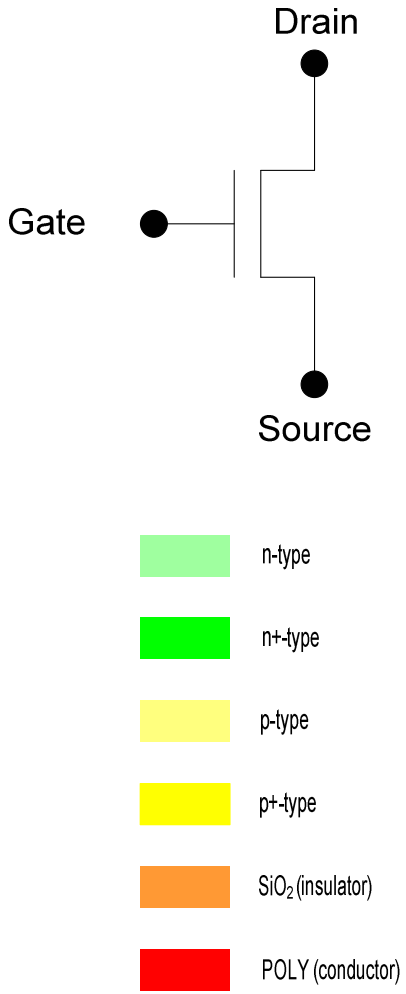


Review

MOS Transistor

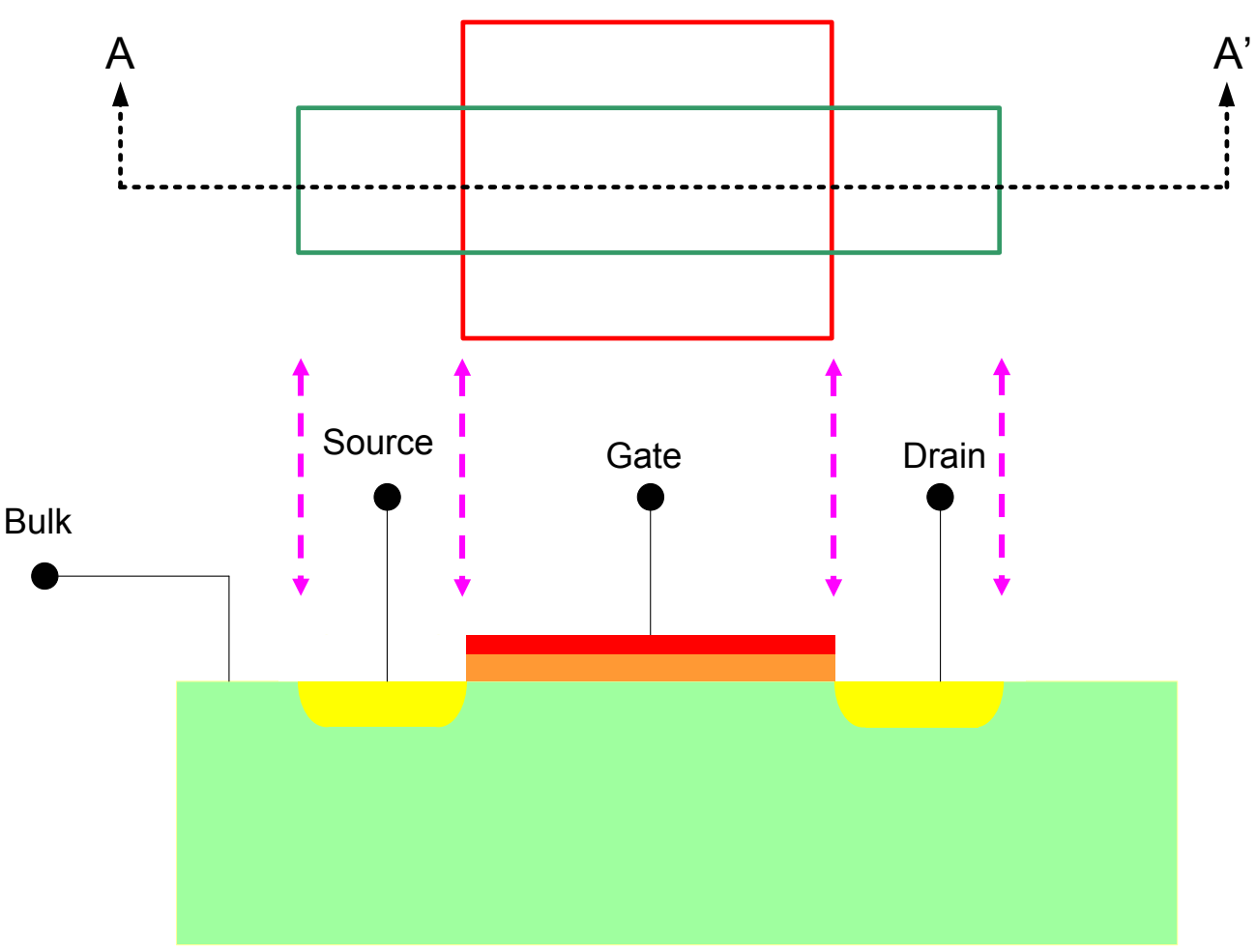


n-channel MOSFET

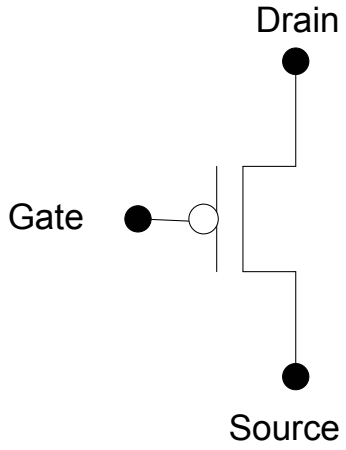


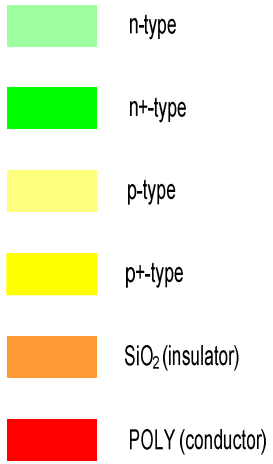
Review

MOS Transistor



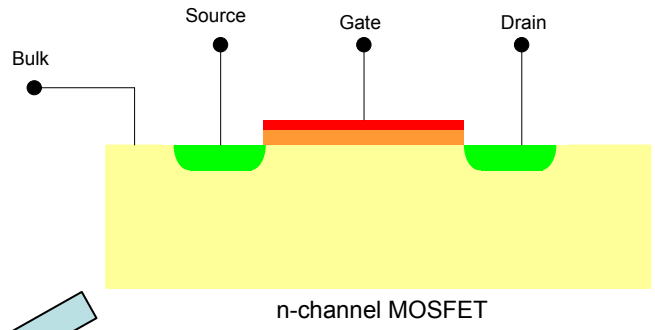
p-channel MOSFET

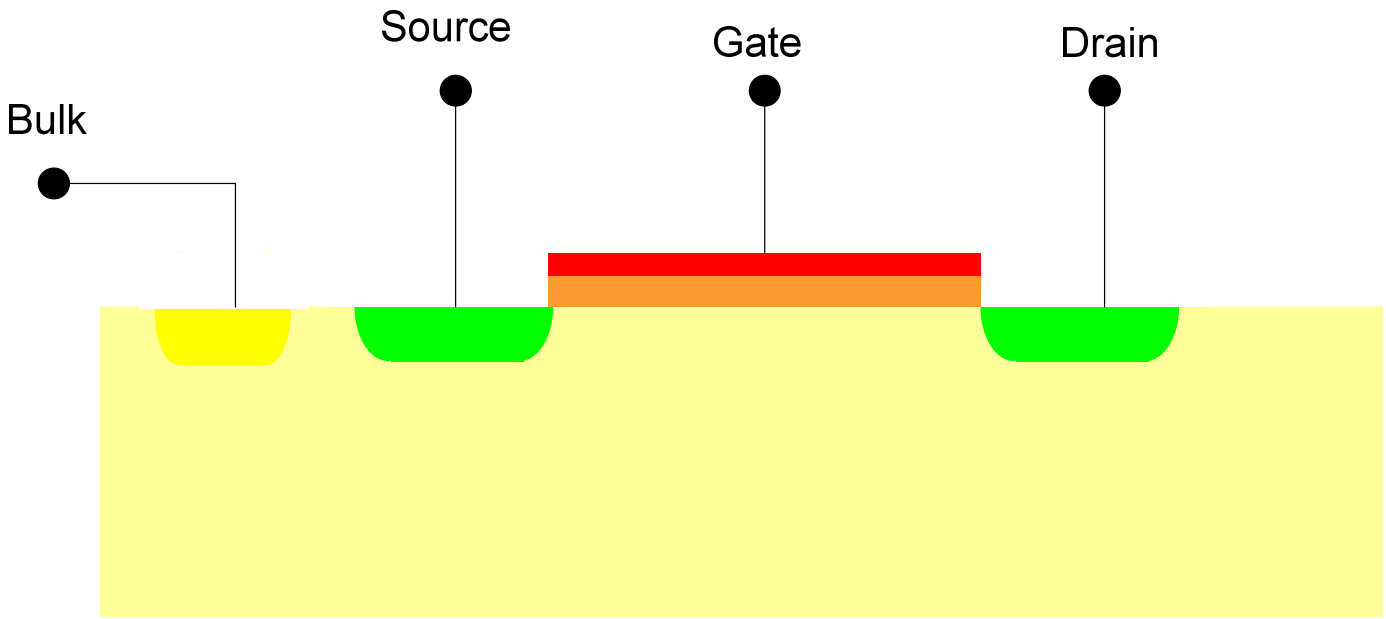




MOS Transistor

n-channel MOS transistor in Bulk CMOS n-well process with bulk contact

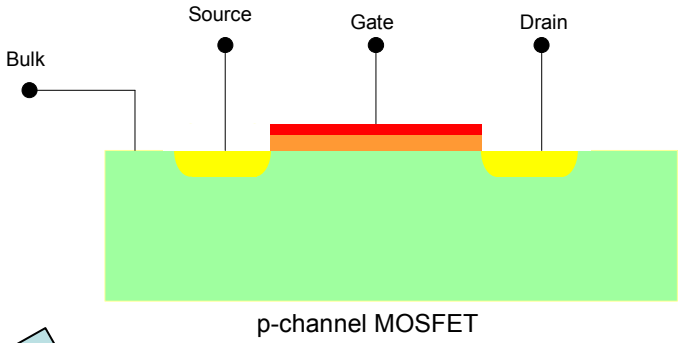


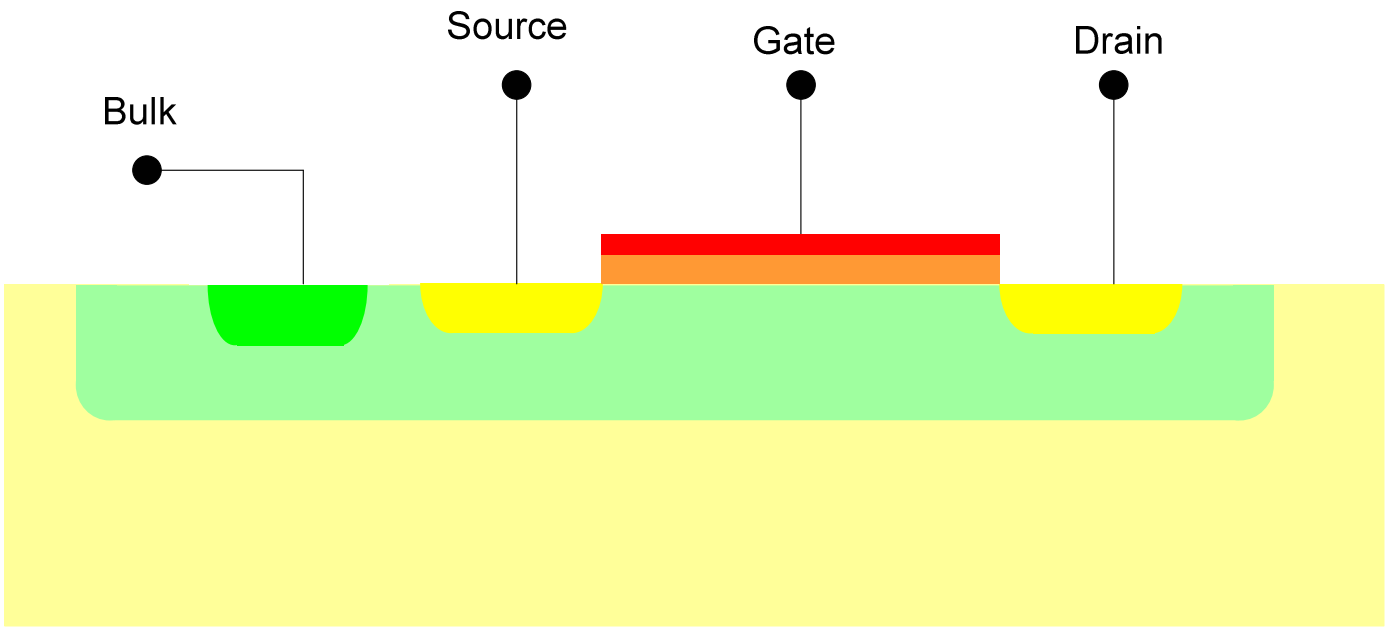


n-channel MOSFET

MOS Transistor

p-channel MOS transistor in
Bulk CMOS n-well process
with bulk contact and well (tub)



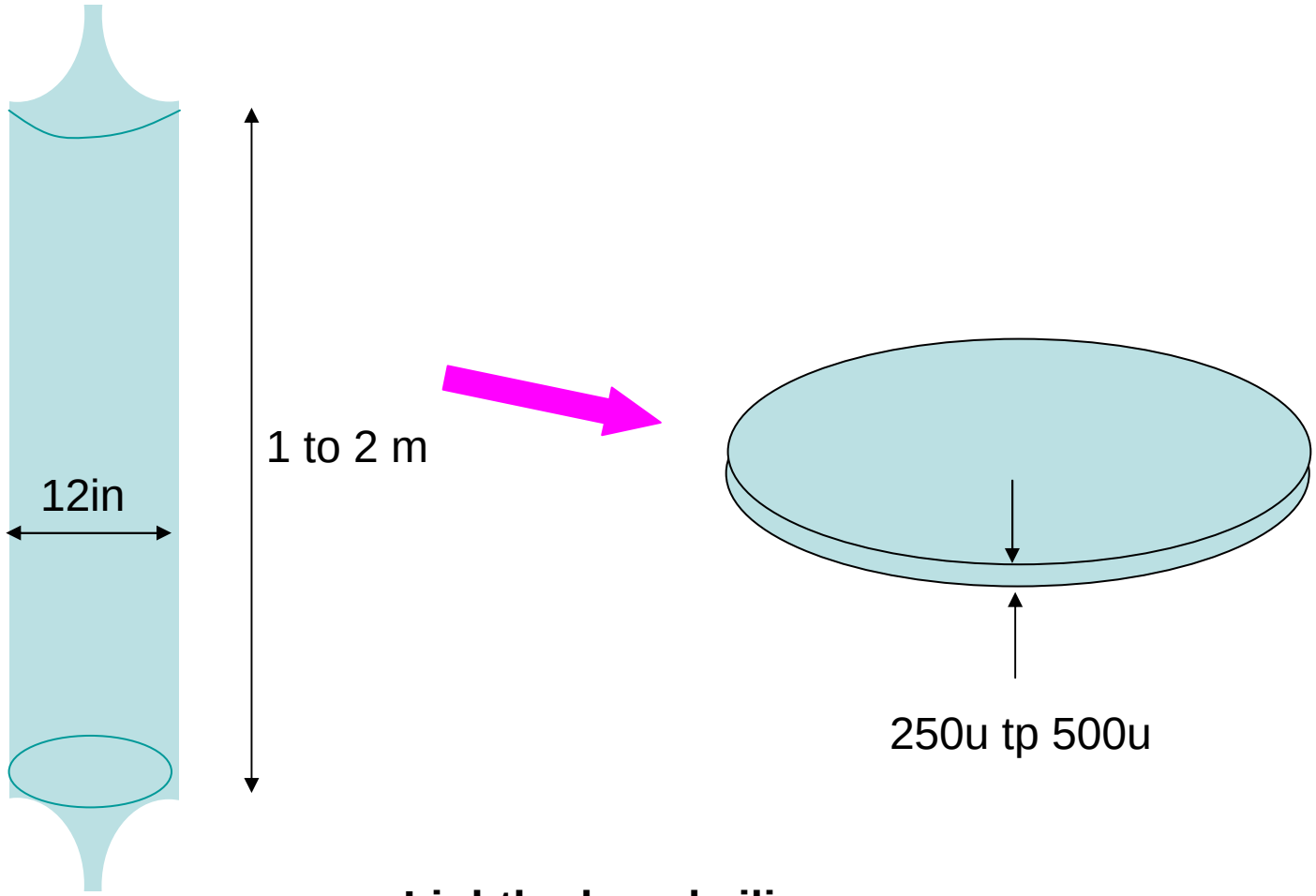


p-channel MOSFET

Crystal Preparation

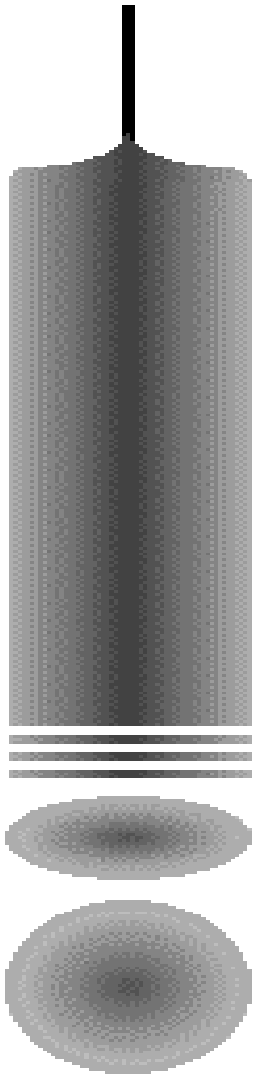
- Large crystal is grown (pulled)
  - 12 inches in diameter and 1 to 2 m long
  - Sliced to 250u to 500u thick
    - Prefer to be much thinner but thickness needed for mechanical integrity
  - 4 to 8 cm/hr pull rate
  - T=1430 ^{o}C
- Crystal is sliced to form wafers
- Cost for 12” wafer around $200
- 5 companies provide 90% of worlds wafers
- Somewhere around 400,000 12in wafers/month

Crystal Preparation



Lightly-doped silicon
Excellent crystalline structure

Crystal Preparation

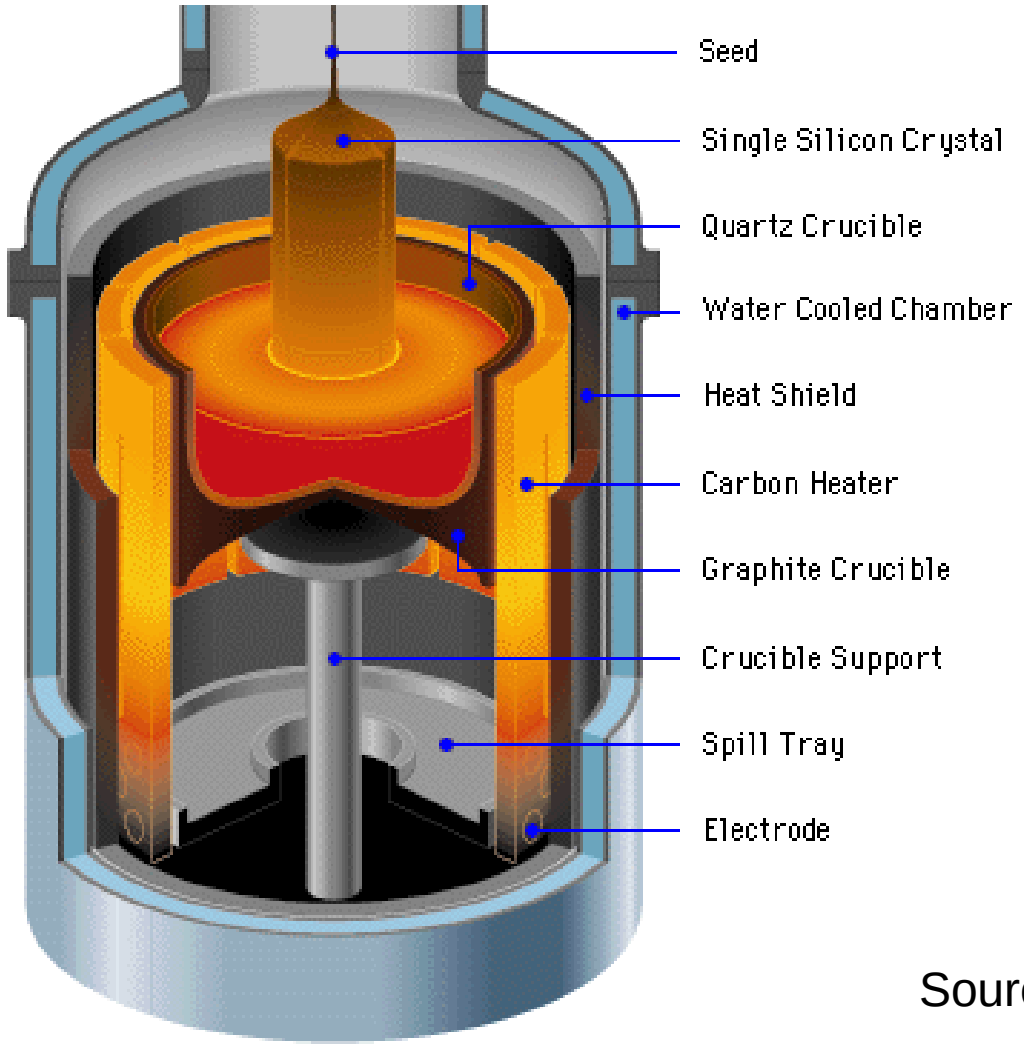


From www.infras.com

Crystal Preparation

Source: WEB

Crystal Preparation



Source: WEB

Crystal Preparation

Source: WEB

Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB

Crystal Preparation

Source: WEB

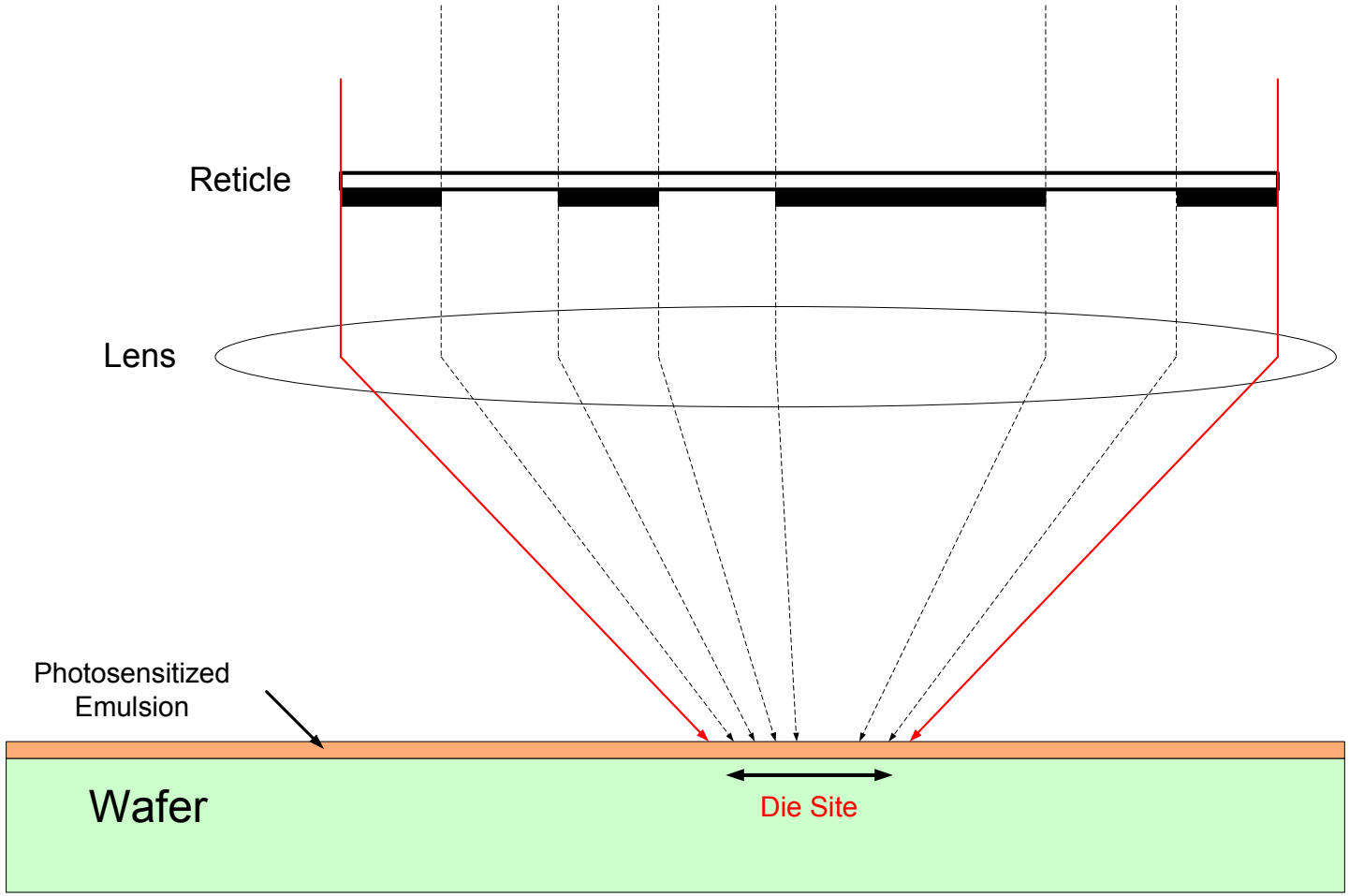
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Masking

- Use masks or reticles to define features on a wafer
  - Masks same size as wafer
  - Reticles used for projection
  - Reticle much smaller (but often termed mask)
  - Reticles often of quartz with chrome
  - Quality of reticle throughout life of use is critical
  - Single IC may require 20 or more reticles
  - Cost of “mask set” now exceeds $1million for state of the art processes
  - Average usage 500 to 1500 times
  - Mask costs exceeding 50% of total fabrication costs in sub 100nm processes
  - Serve same purpose as a negative (or positive) in a photographic process

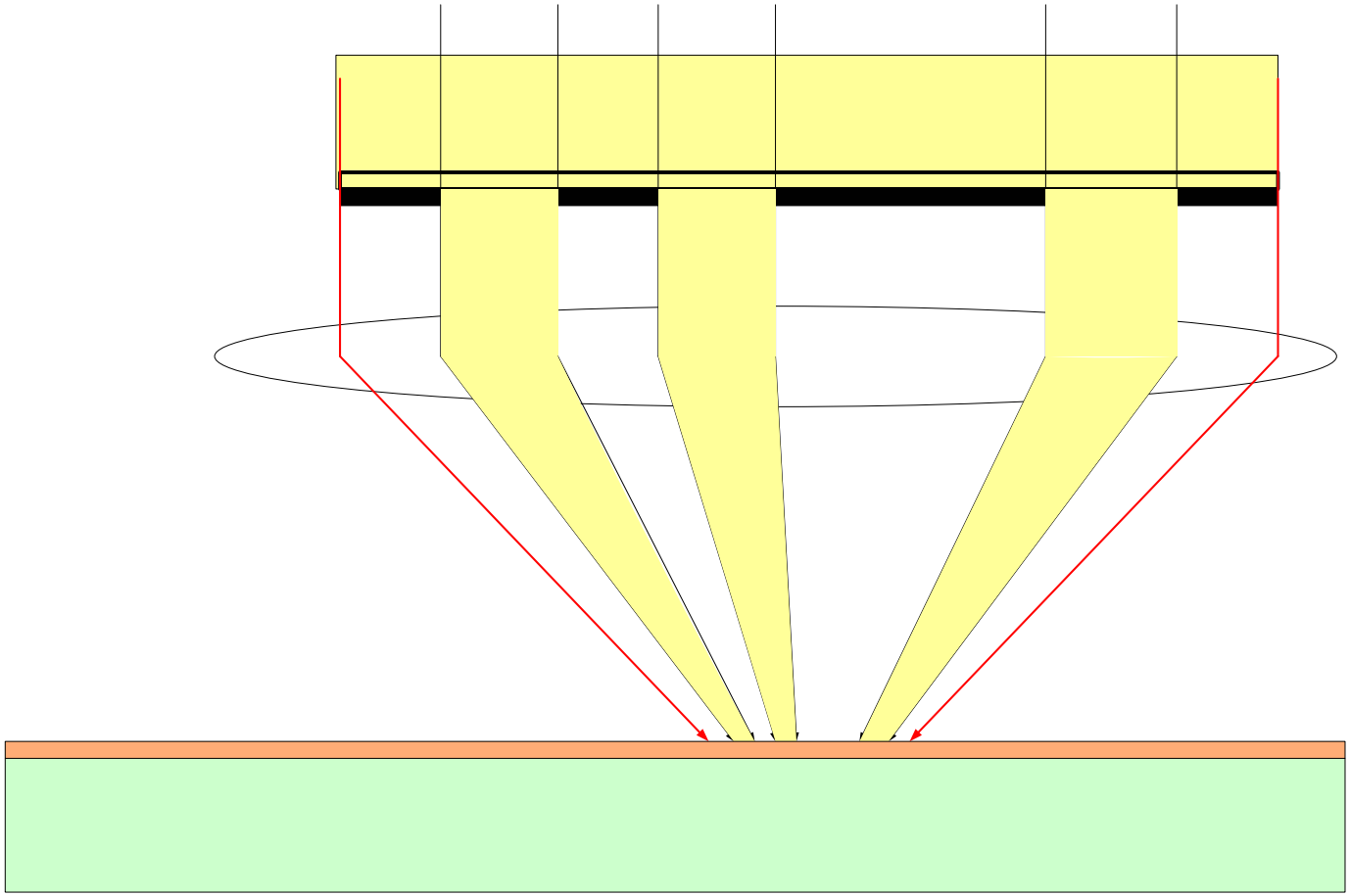
Masking



Step and Repeat (stepper) used to image across wafer

Masking

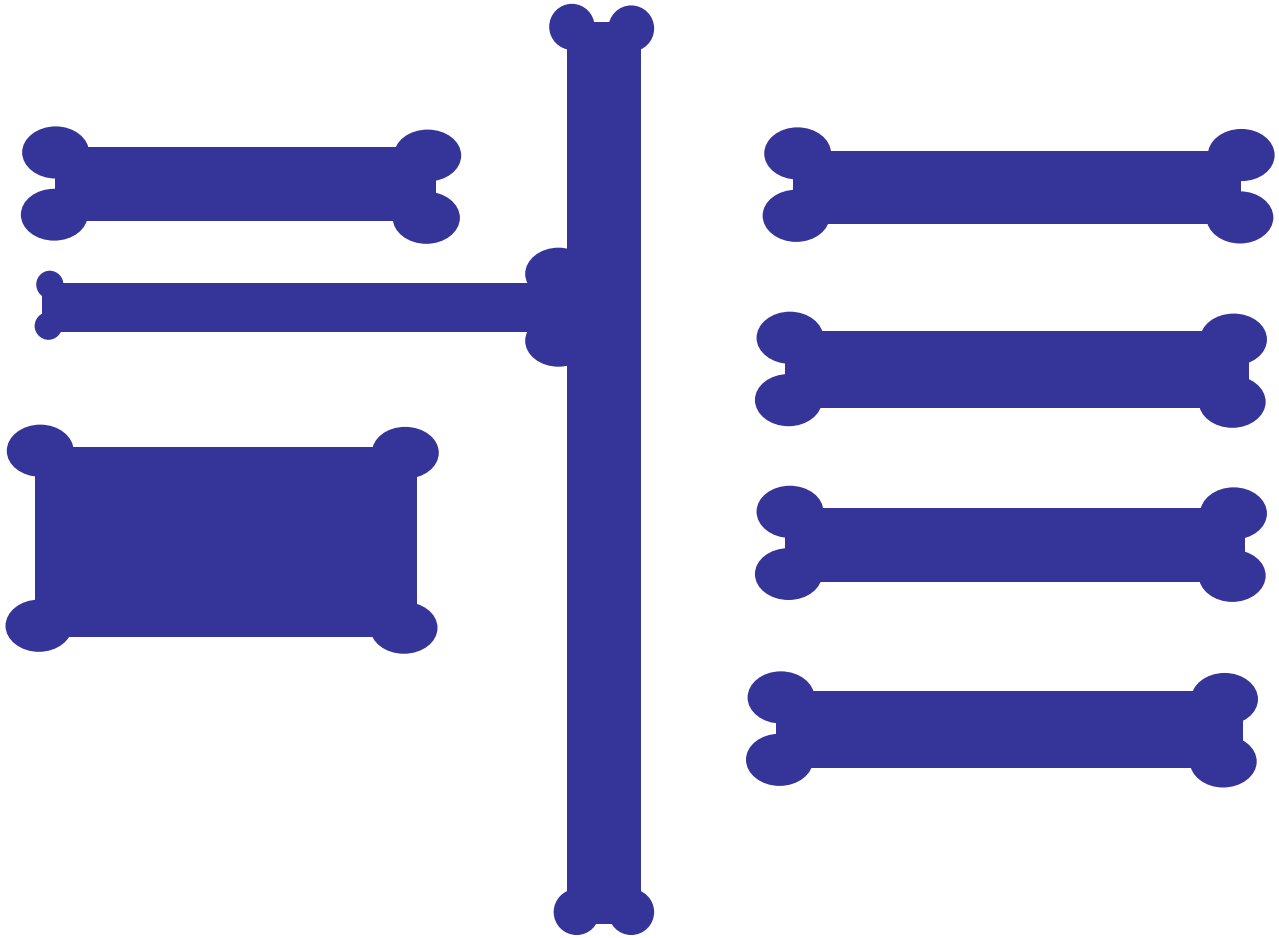
Exposure through reticle



Masking

Mask Features

Masking



Mask Features Intentionally Distorted to Compensated For Wavelength Limitations in Small Features

IC Fabrication Technology

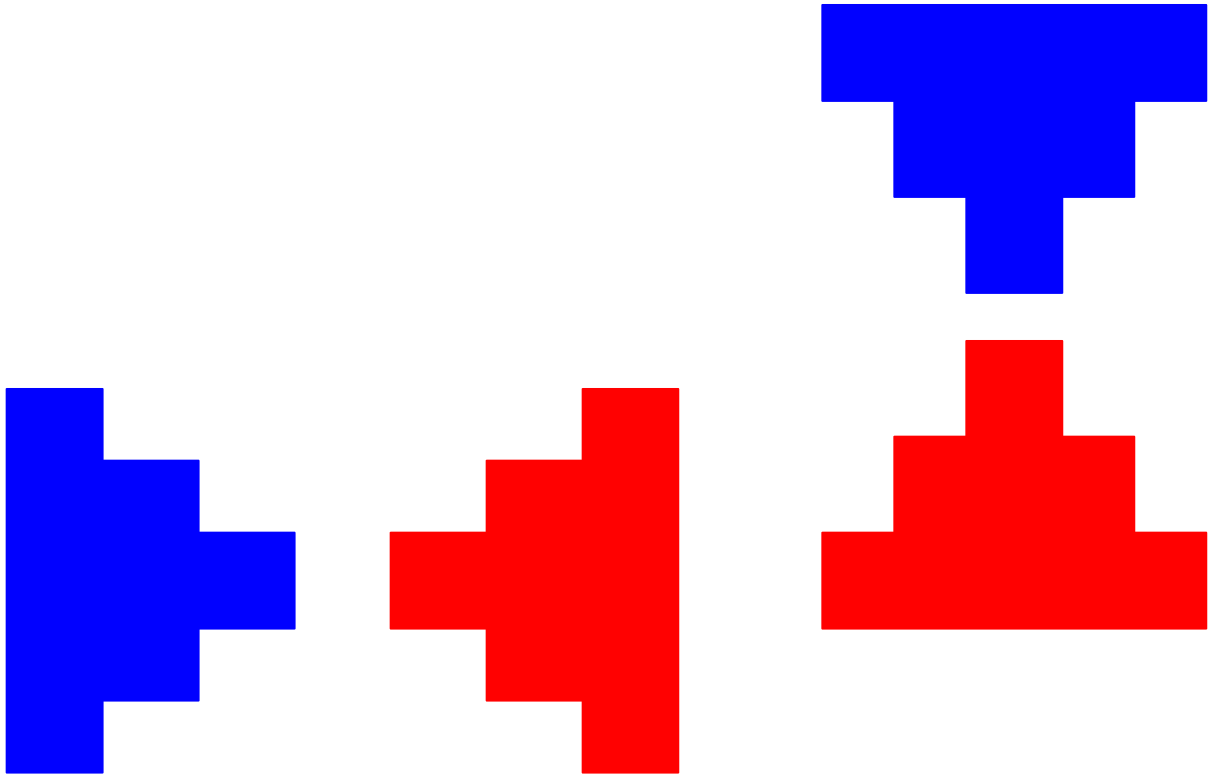
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
- Exposure
  - Projection through reticle with stepper
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

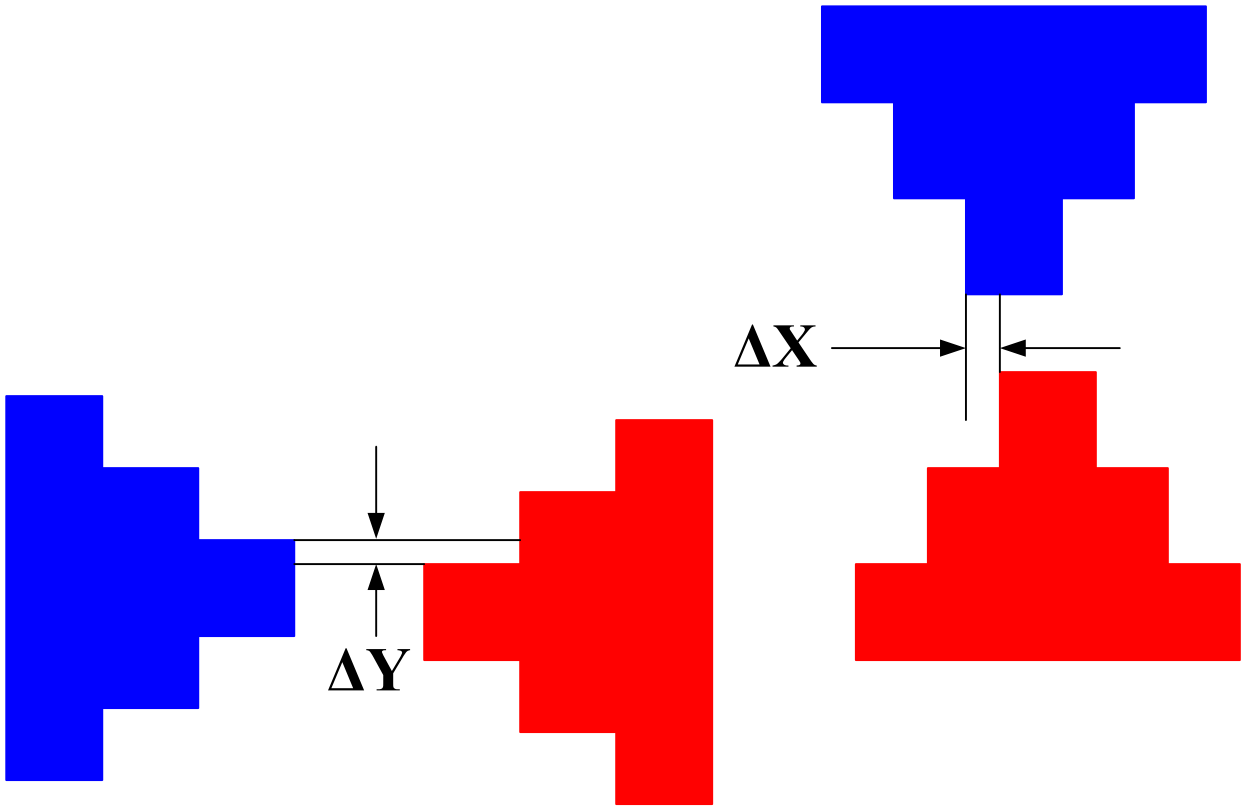
Mask Alignment

Correctly Aligned



Mask Alignment

Alignment Errors



IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Deposition

- Application of something to the surface of the silicon wafer or substrate
  - Layers 15A to 20u thick
- Methods
  - Physical Vapor Deposition (nonselective)
    - Evaporation/Condensation
    - Sputtering (better host integrity)
  - Chemical Vapor Deposition (nonselective)
    - Reaction of 2 or more gases with solid precipitate
    - Reduction by heating creates solid precipitate (pyrolytic)
  - Screening (selective)
    - For thick films
    - Low Tech, not widely used today

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Etching

Selective Removal of Unwanted Materials

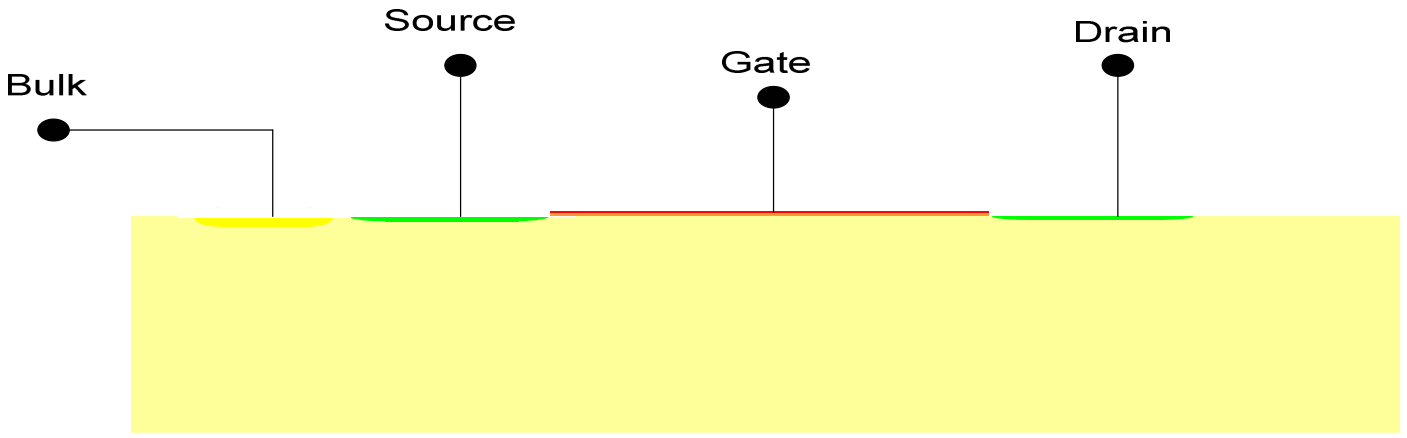
- Wet Etch
  - Inexpensive but under-cutting a problem
- Dry Etch
  - Often termed ion etch or plasma etch

Etching

Desired Physical Features

Note: Vertical Dimensions Generally Orders of Magnitude Smaller Than Lateral Dimensions so Different Vertical and Lateral Scales Will be Used In This Discussion

Lateral Relative to Vertical Dimensions

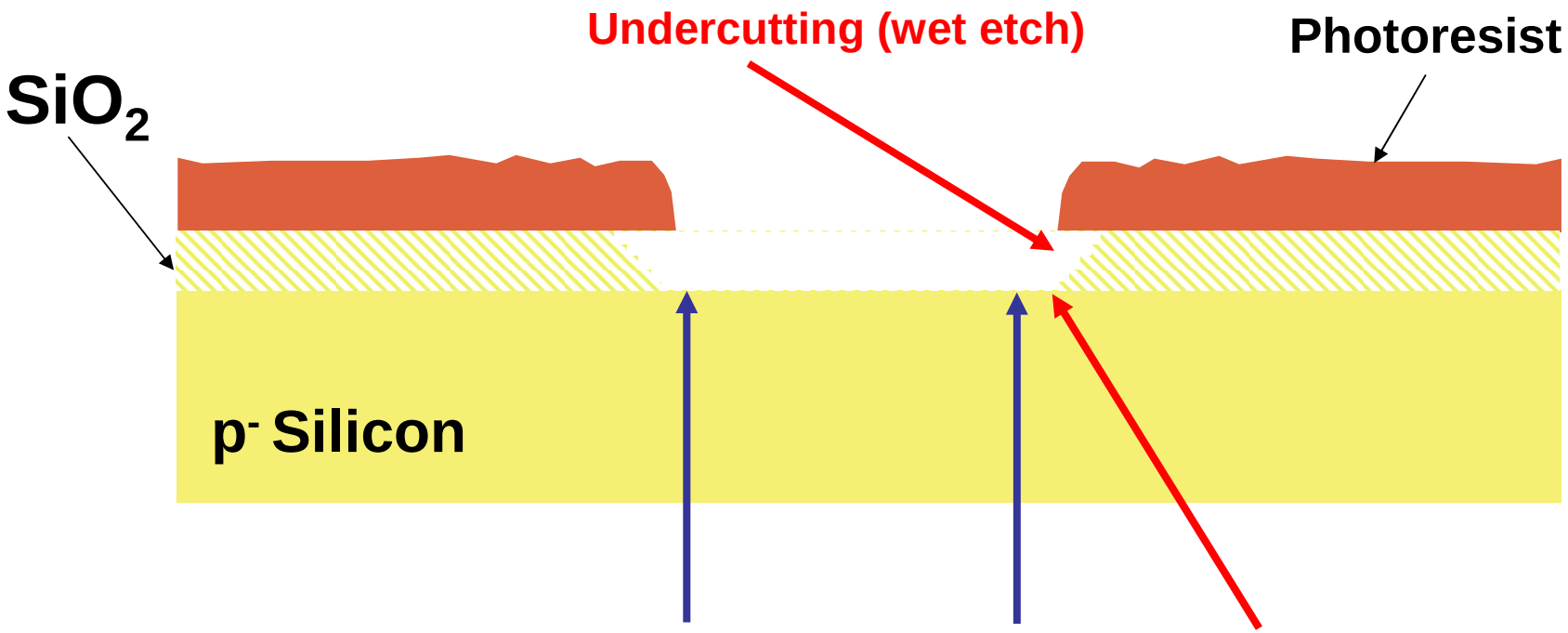


n-channel MOSFET

Still Not to Scale

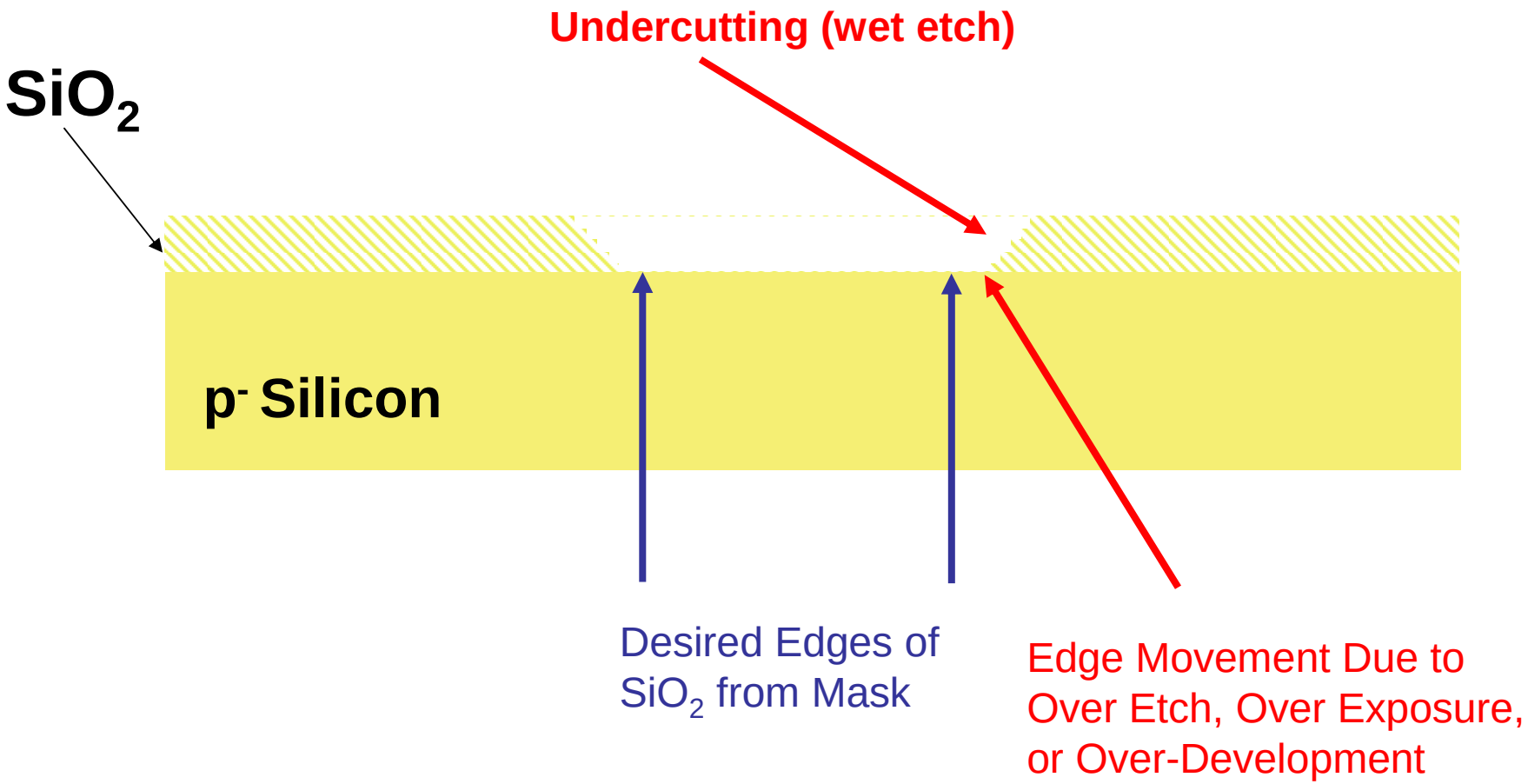
For Example, the wafer thickness is around 250u and the gate oxide is around 50A (5E-3u) and diffusion depths are around λ/5

Etching



Feature Degradation

Etching



SiO_2 after photoresist removal

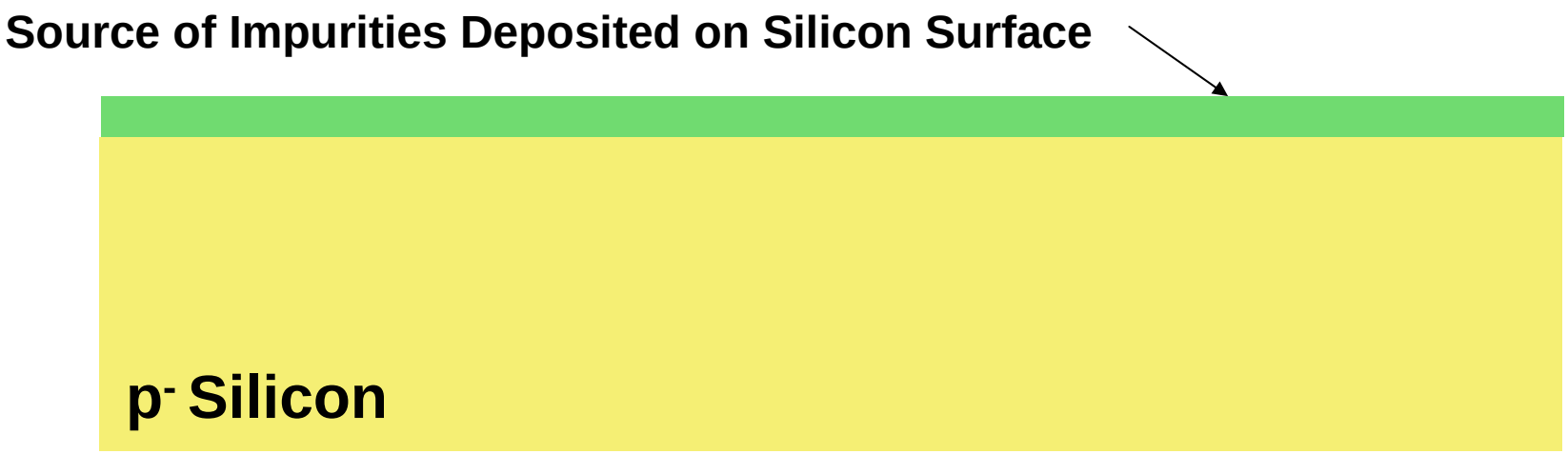
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800^{o}C to 1200^{o}C
- Source of Impurities
  - Deposition
  - Ion Implantation
    - Only a few A^{o} deep
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion

Diffusion



Before Diffusion

After Diffusion

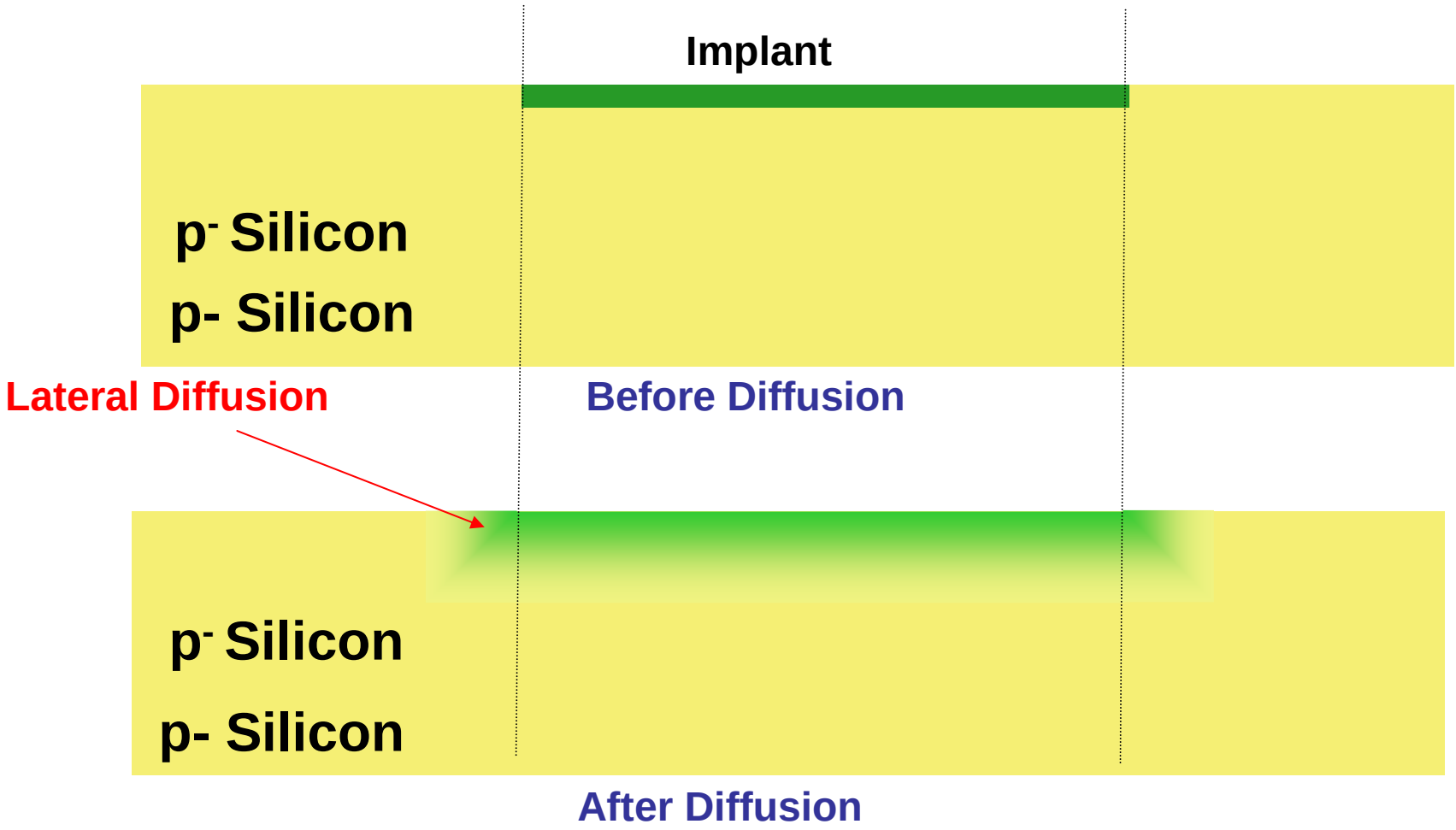
Diffusion

Source of Impurities Implanted in Silicon Surface

Before Diffusion

After Diffusion

Diffusion


Implant
p- Silicon
p- Silicon
Lateral Diffusion
Before Diffusion
p- Silicon
p- Silicon
After Diffusion

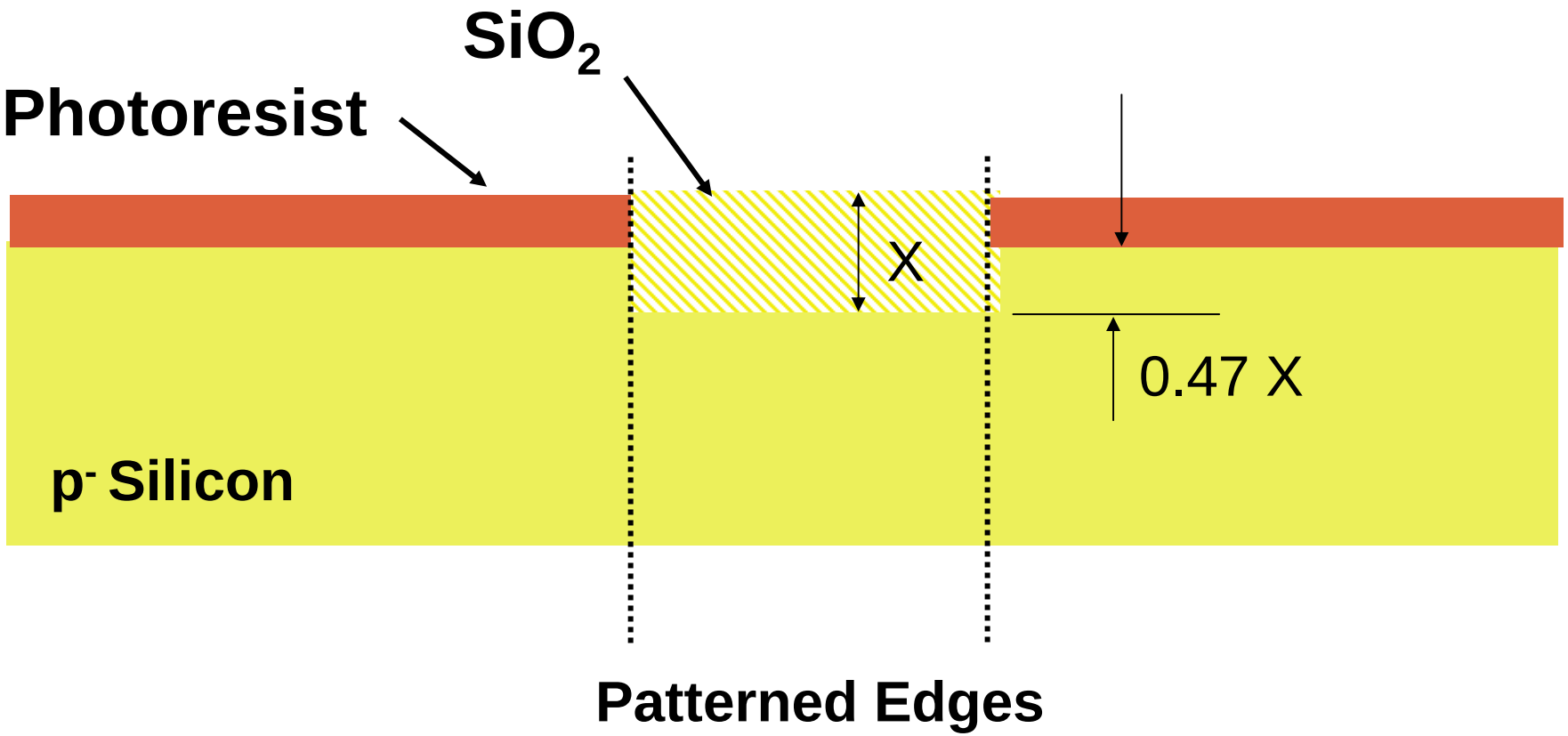
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Oxidation

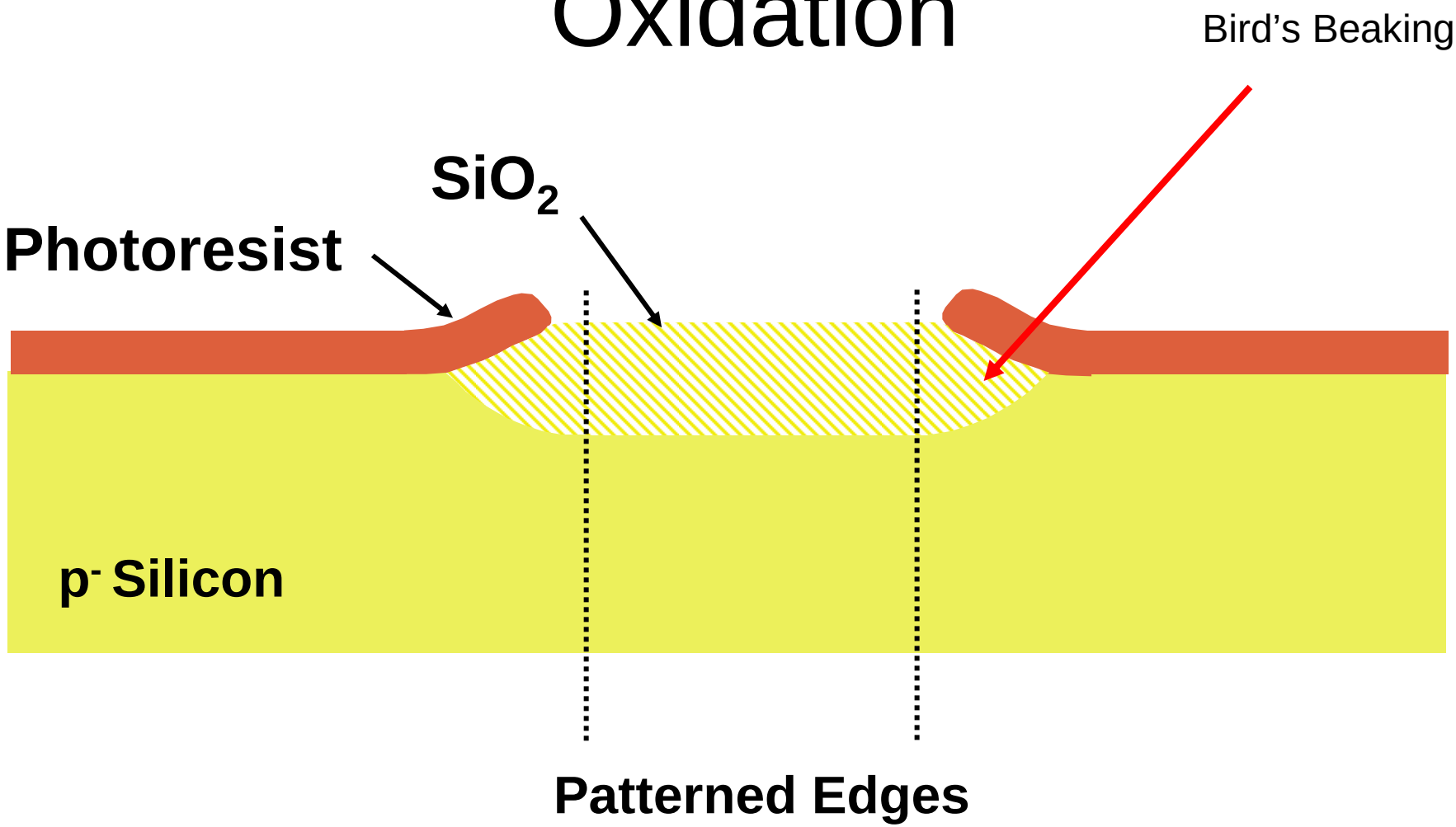
- SiO_2 is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO_2 consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO_2 on materials other than Si

Oxidation



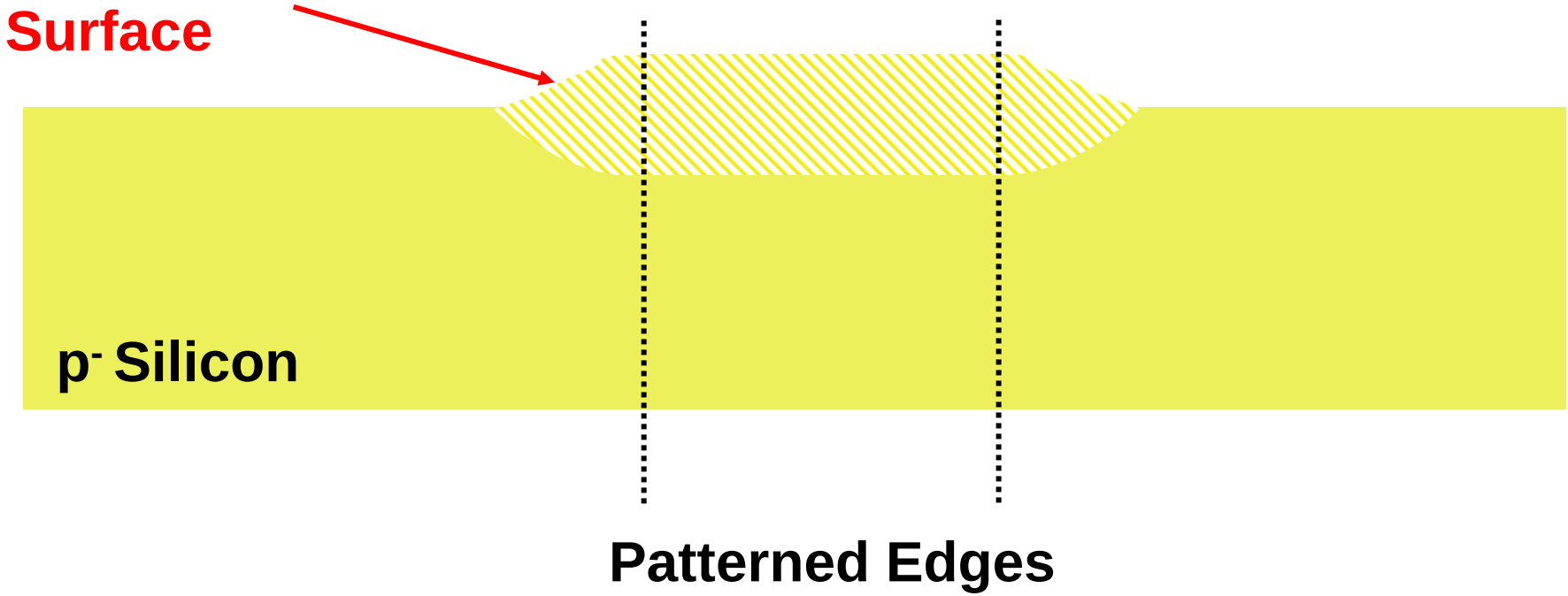
Thermally Grown SiO_2 - desired growth

Oxidation



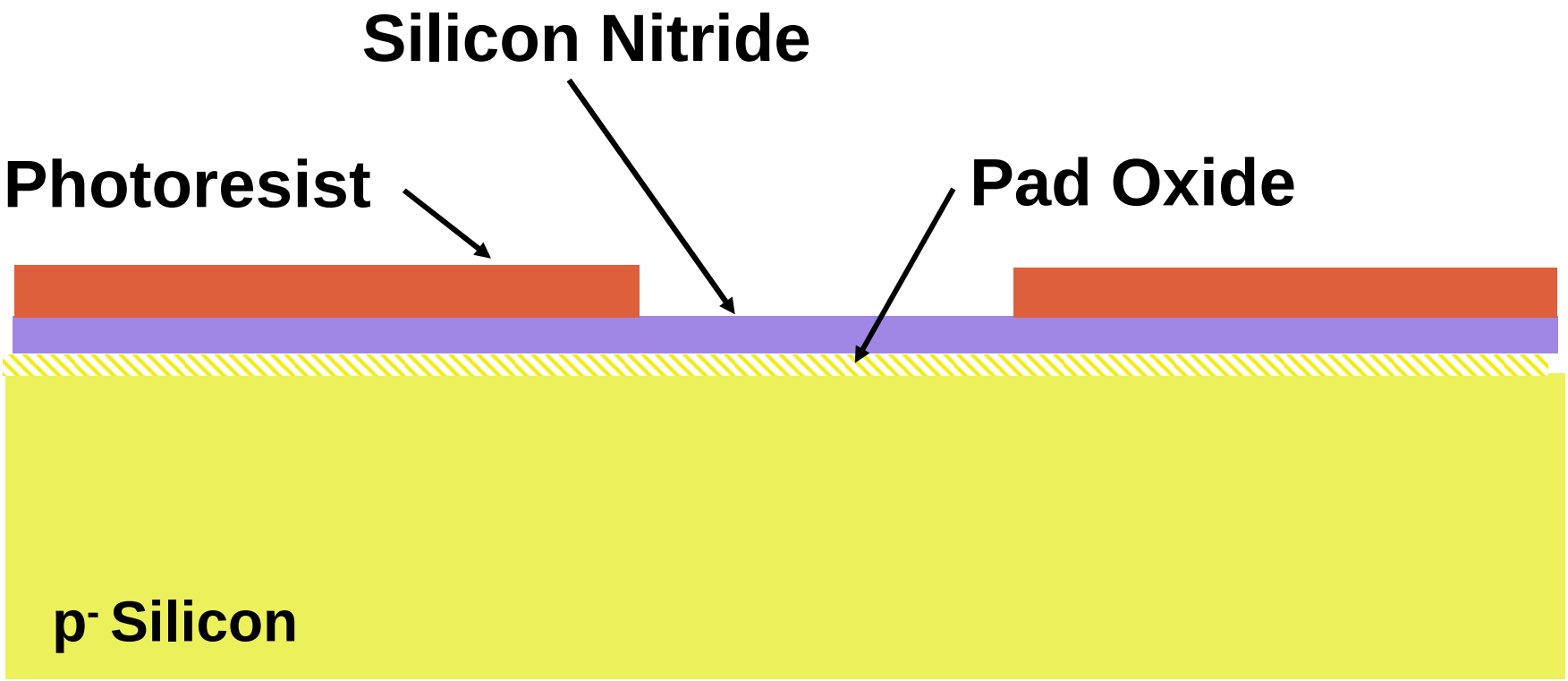
Thermally Grown SiO_2 - actual growth

Oxidation



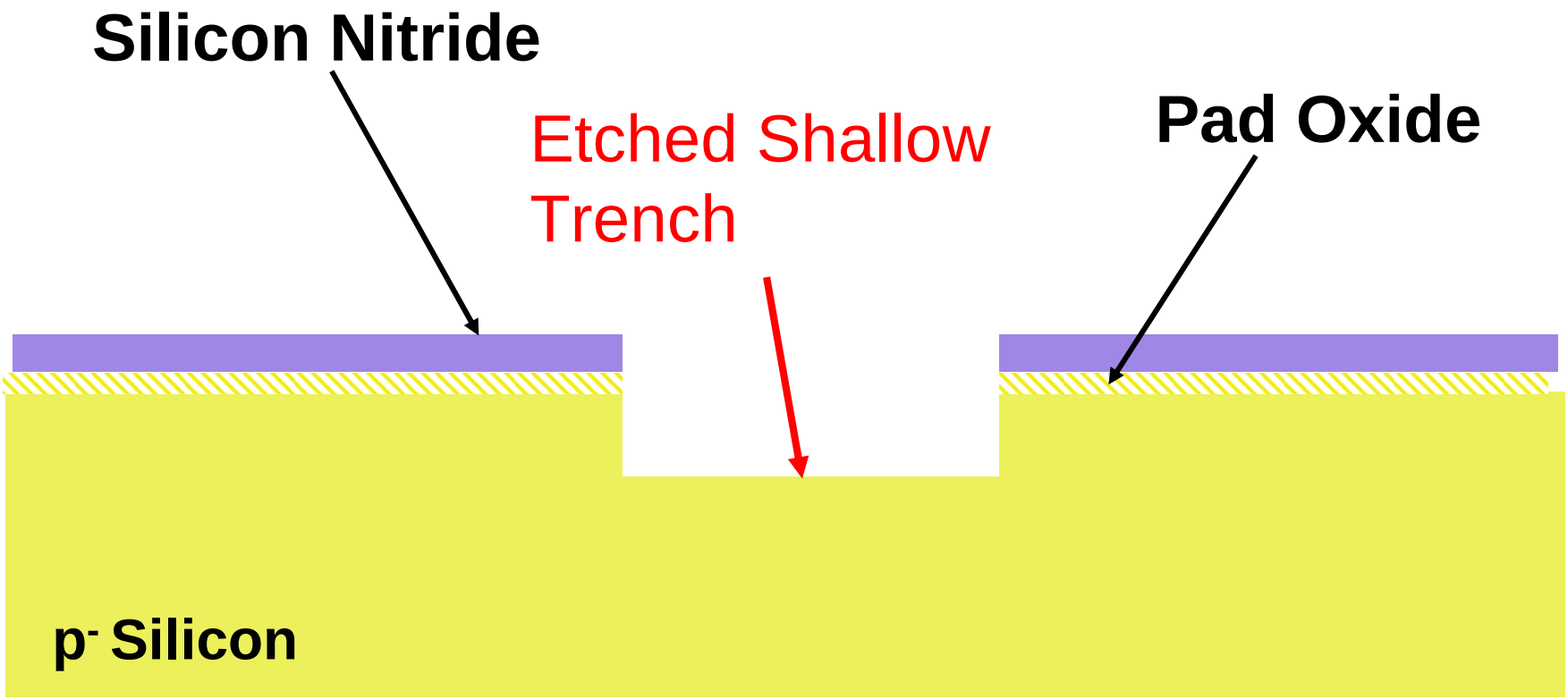
Thermally Grown SiO_2 - actual growth

Oxidation



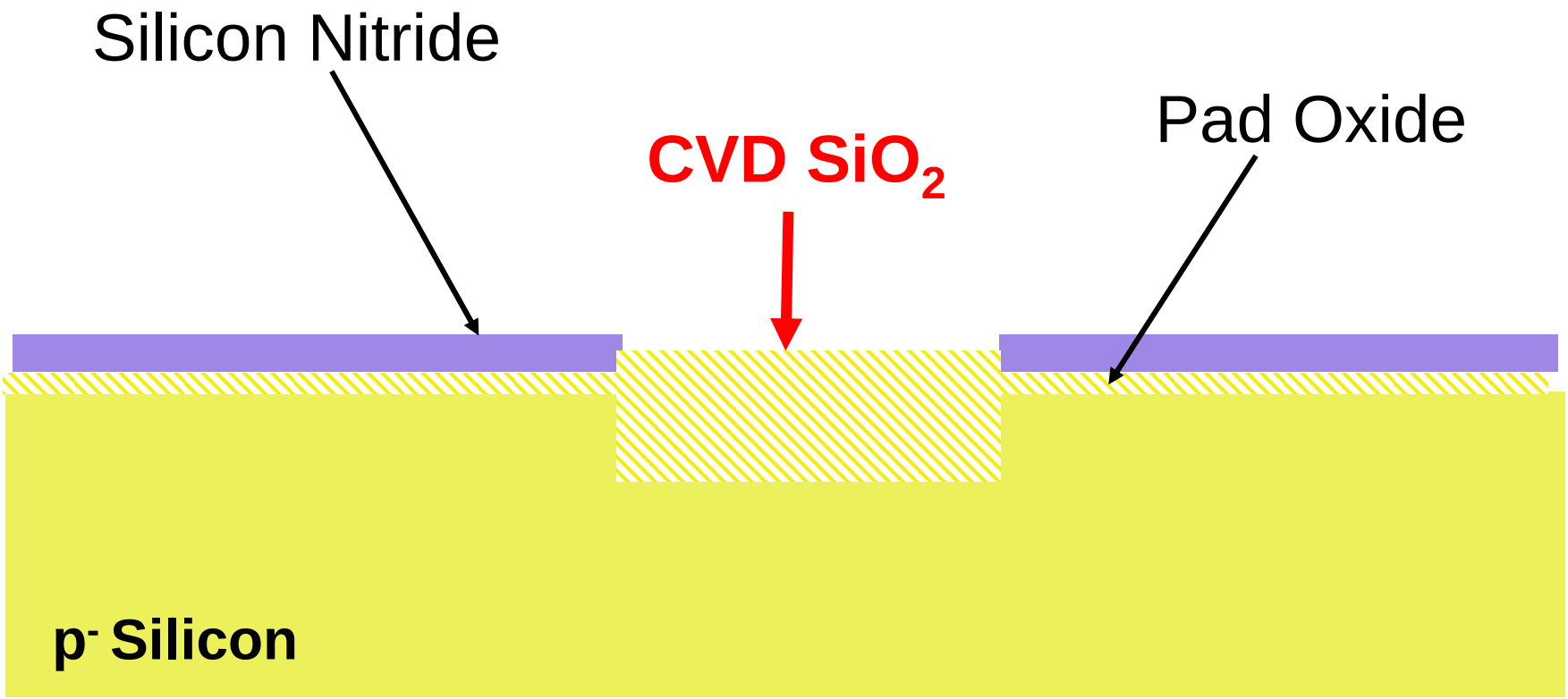
Shallow Trench Isolation (STI)

Oxidation



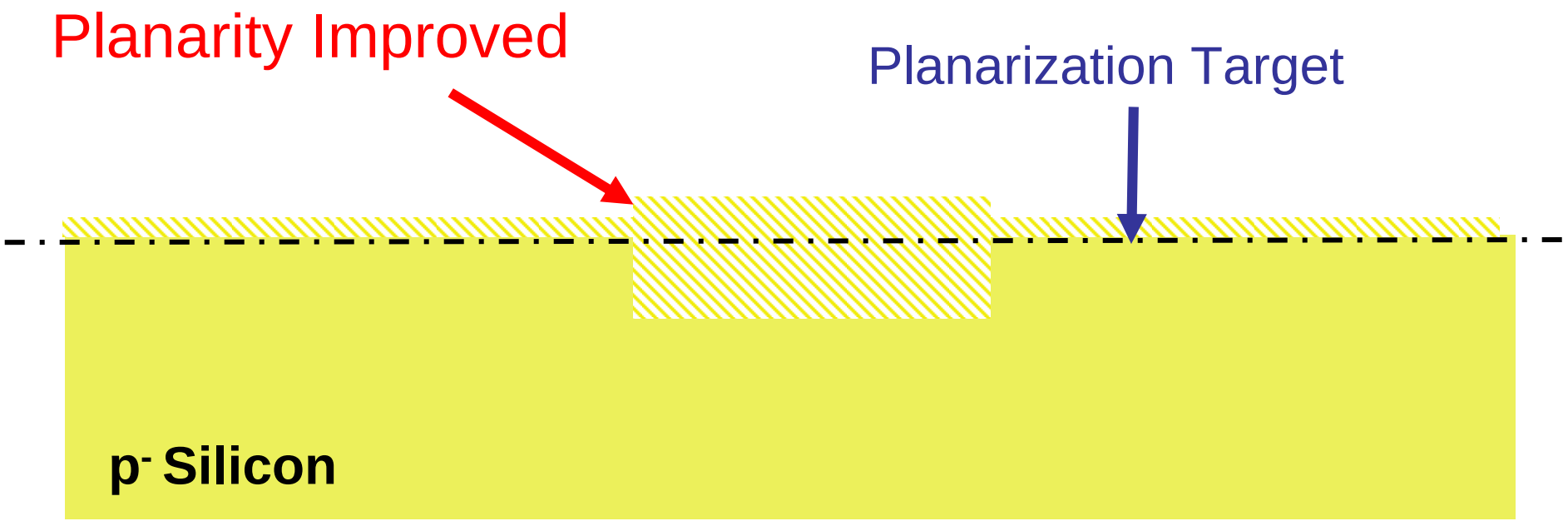
Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

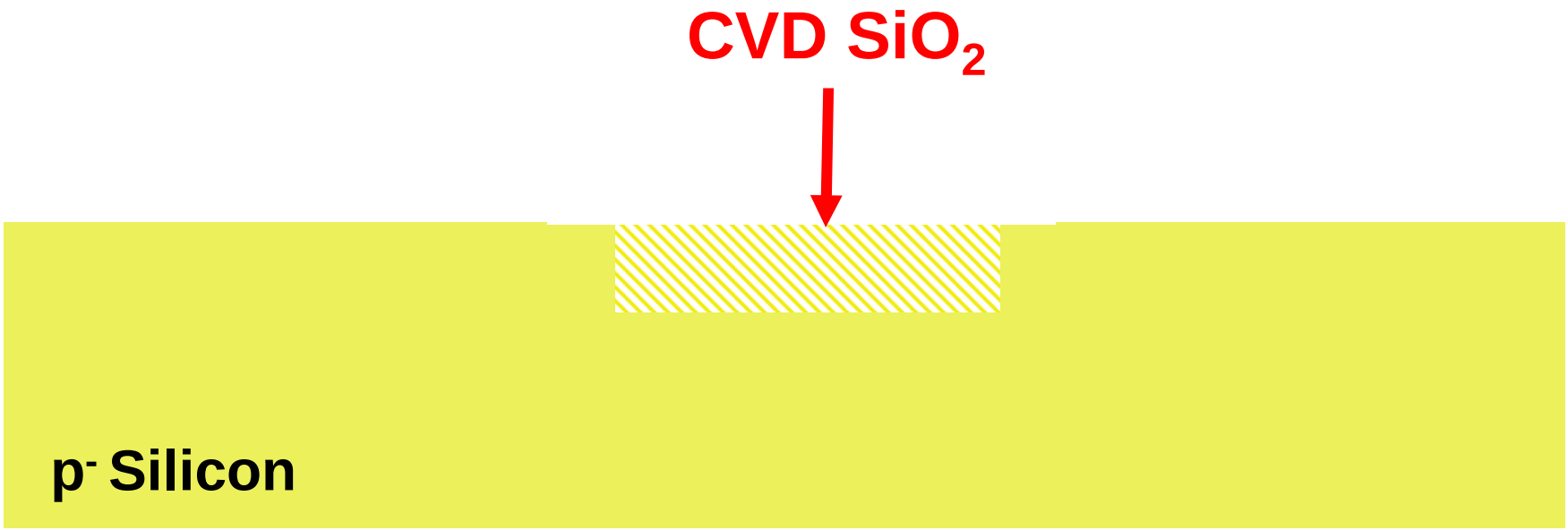
Oxidation



Shallow Trench Isolation (STI)

Oxidation

After Planarization



Shallow Trench Isolation (STI)

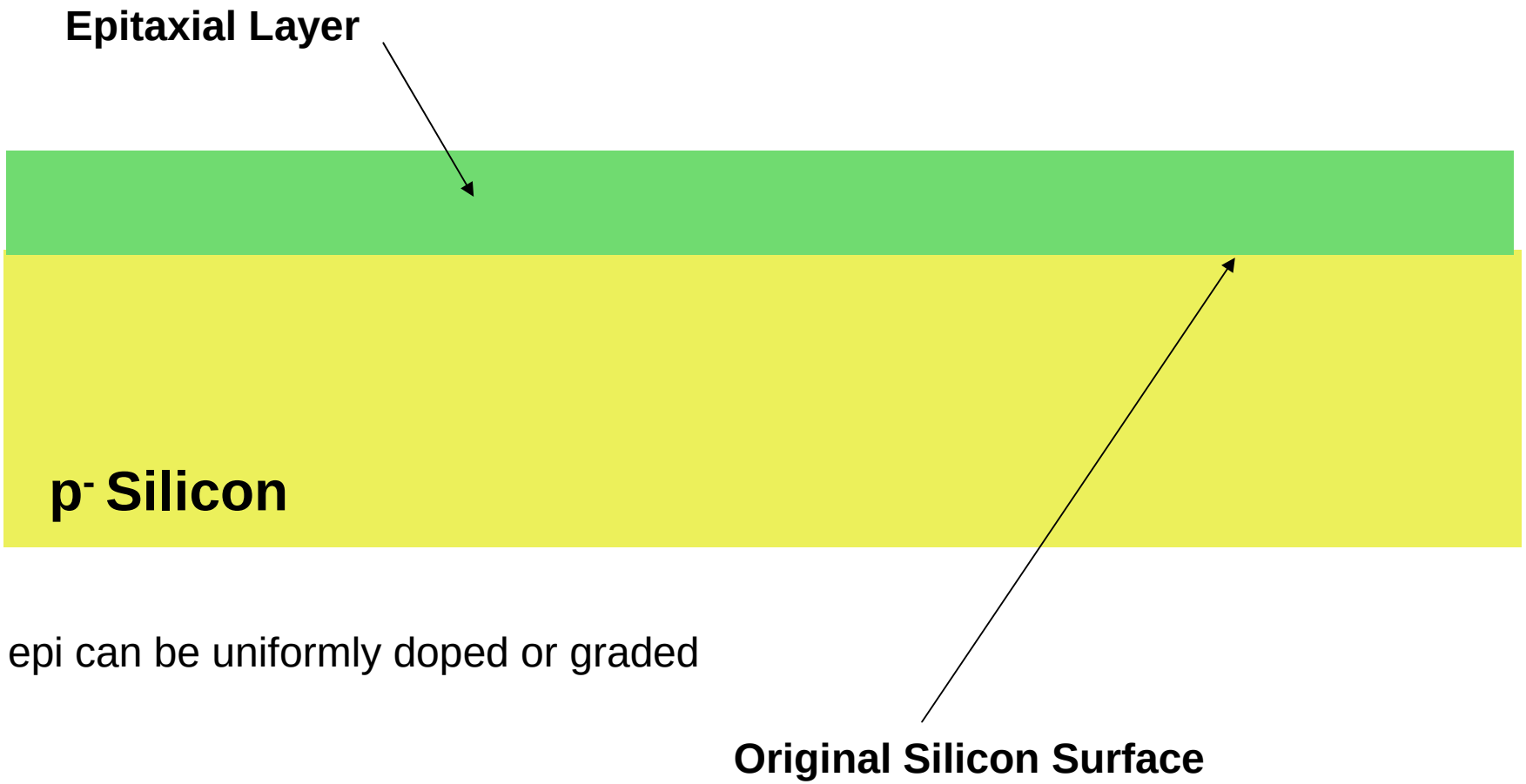
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Epitaxy

- Single Crystaline Extension of Substrate Crystal
  - Commonly used in bipolar processes
  - CVD techniques
  - Impurities often added during growth
  - Grows slowly to allow alignmnt with substrate

Epitaxy



epi can be uniformly doped or graded

Question: Why can't a diffusion be used to create the same effect as an epi layer ?

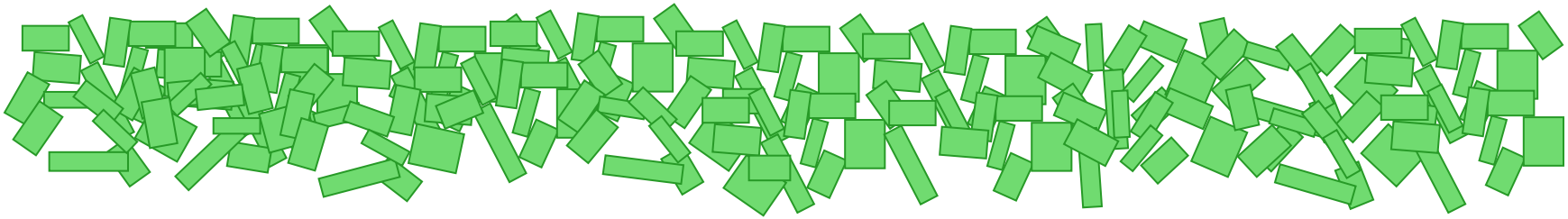
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)

Polysilicon



Polysilicon

Single-Crystaline Silicon

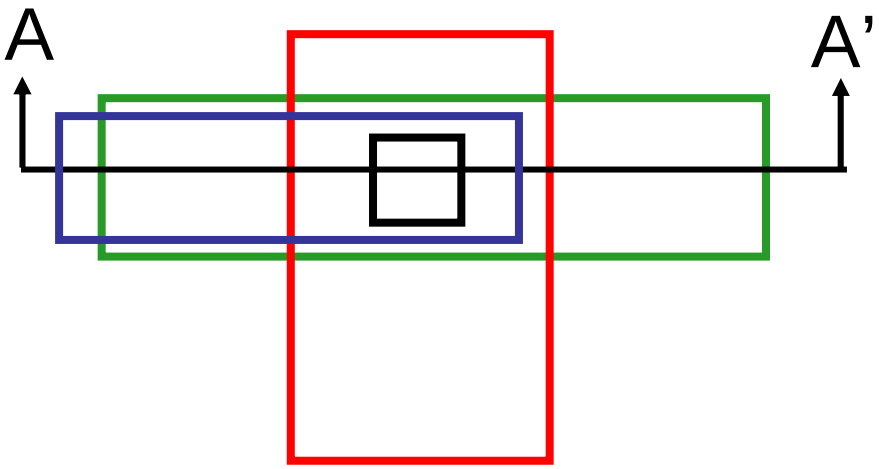
IC Fabrication Technology

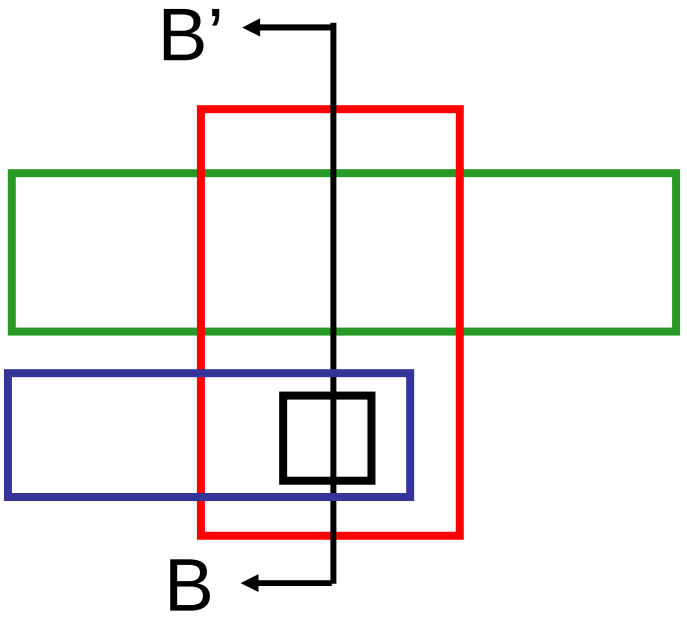
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Contacts, Interconnect and Metalization

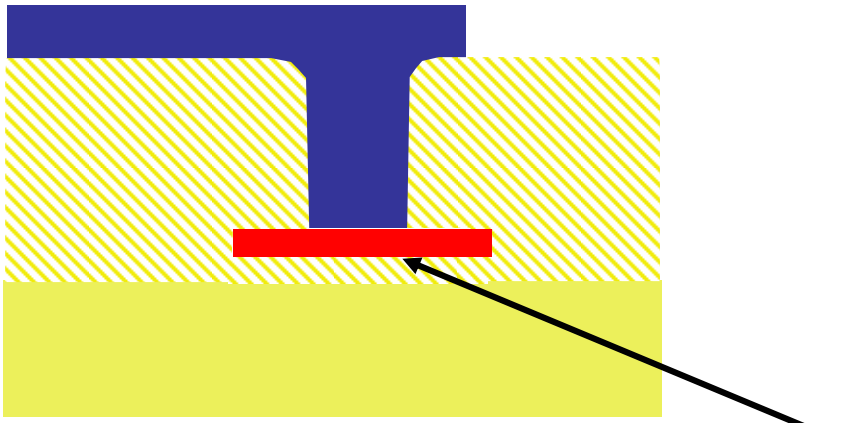
- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

Contacts





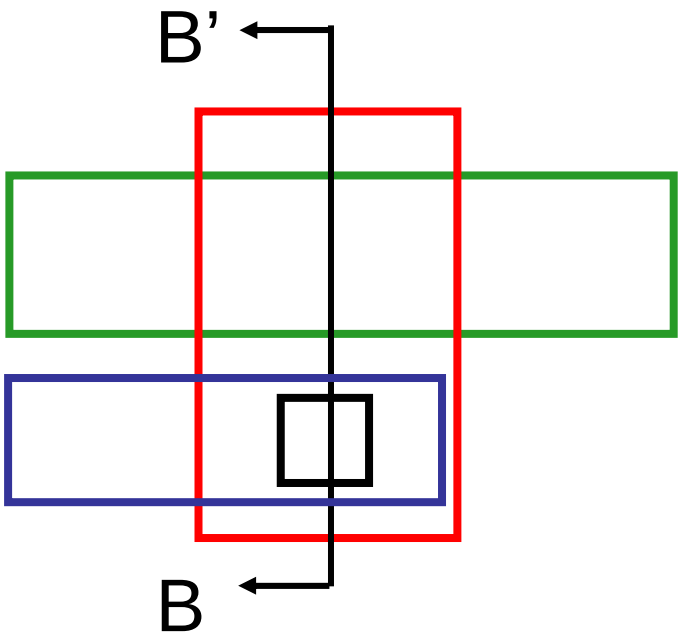
Acceptable Contact

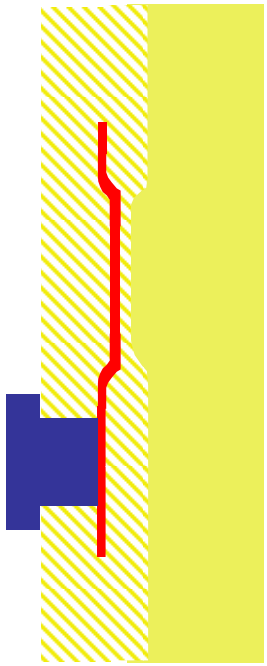


Unacceptable Contact

Vulnerable to pin holes

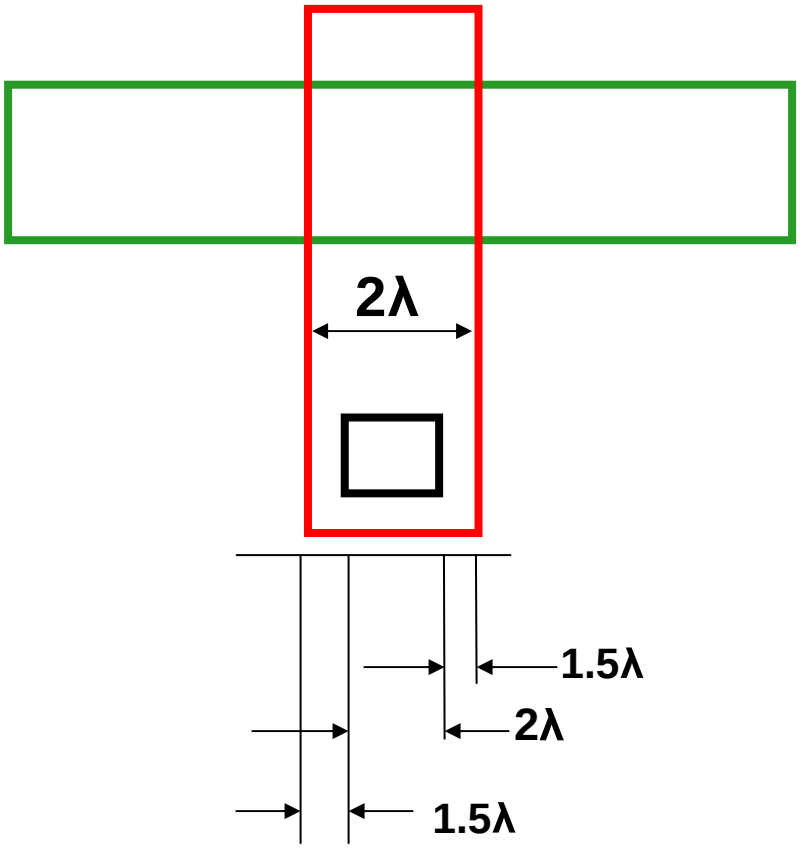
Contacts



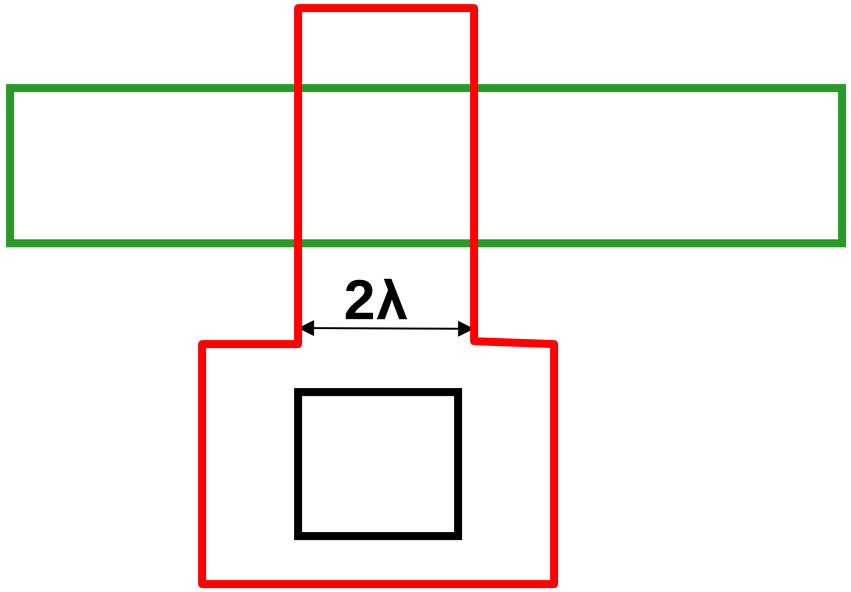


Acceptable Contact

Contacts

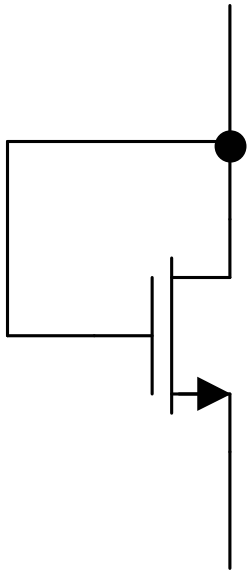


Design Rule Violation

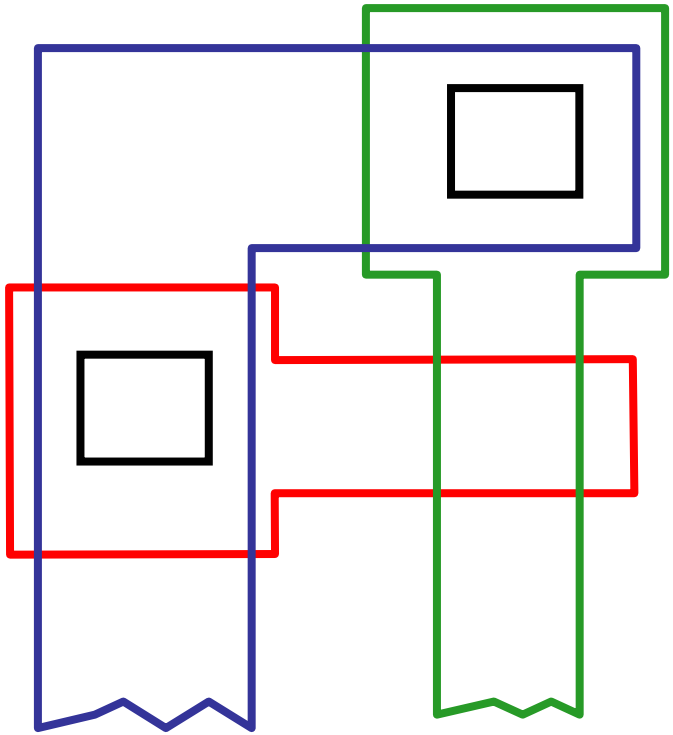


“Dog Bone” Contact

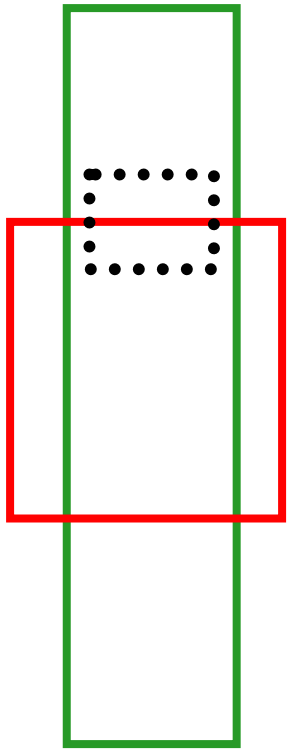
Contacts



Common
Circuit
Connection



Standard Interconnection



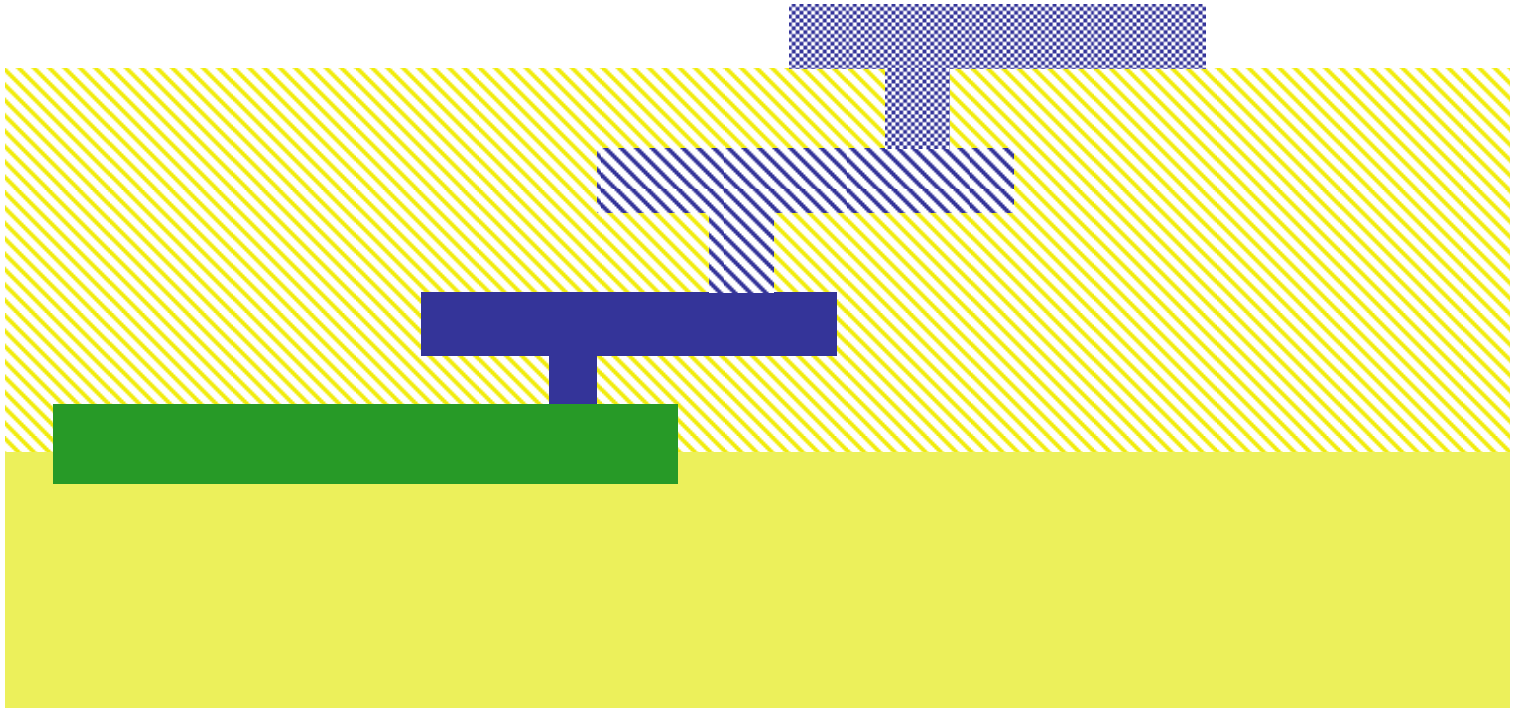
Buried Contact

Can save area but not
allowed in many processes

Metalization

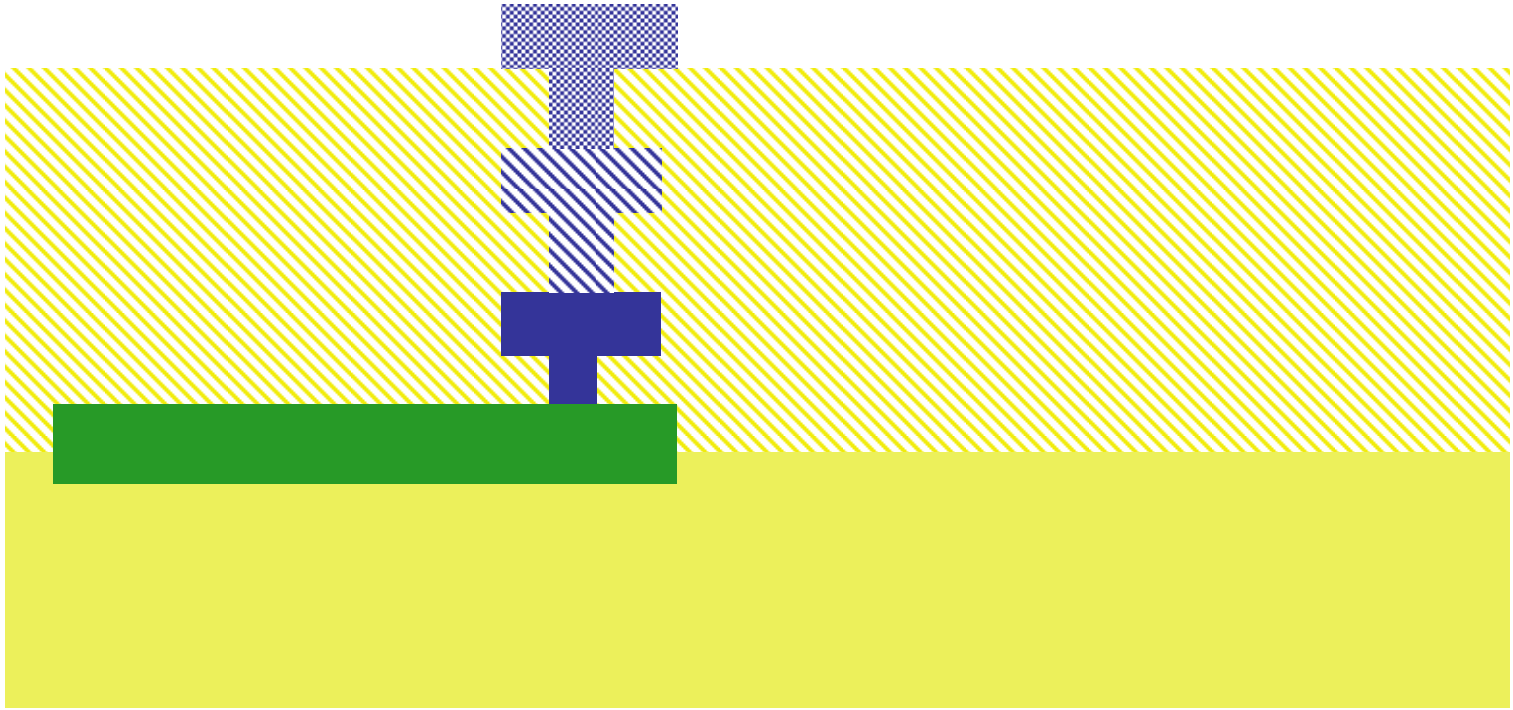
- Aluminum widely used for interconnect
- Copper finding some applications
- Must not exceed maximum current density
  - around 1ma/u
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Multiple Level Interconnects



3-rd level metal connection to n-active without stacked vias

Multiple Level Interconnects

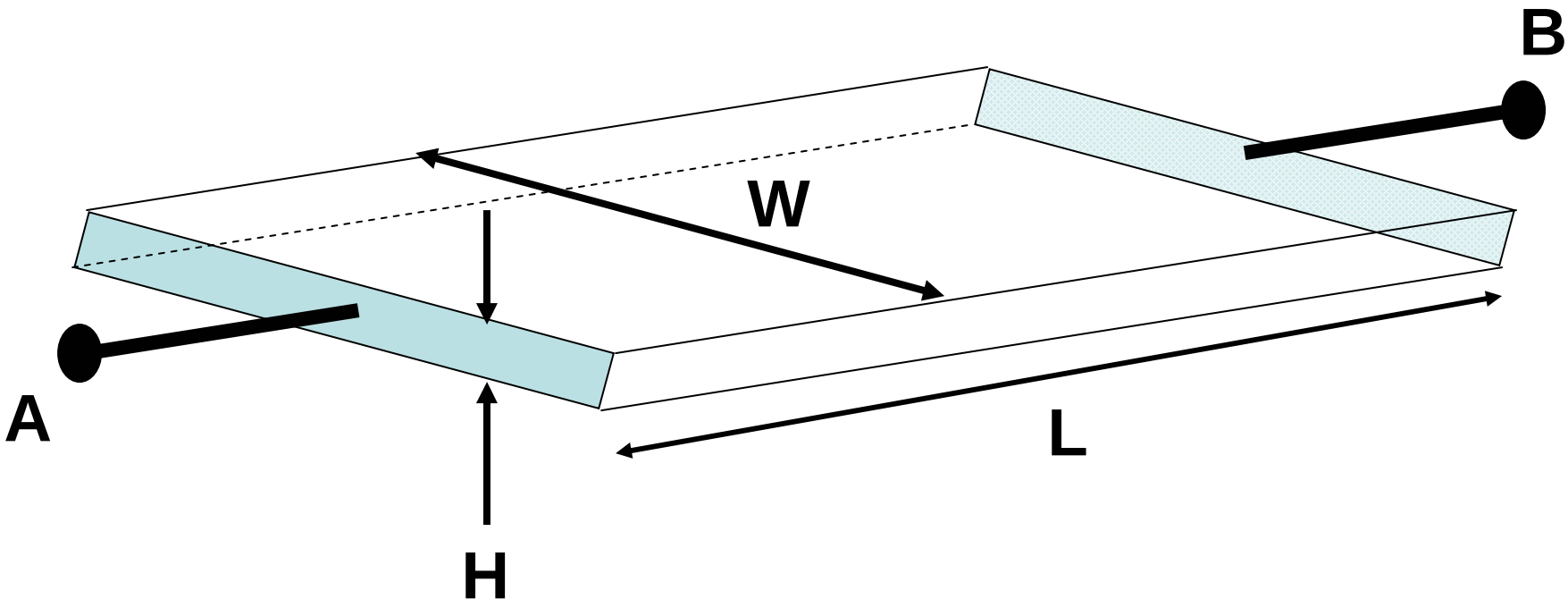


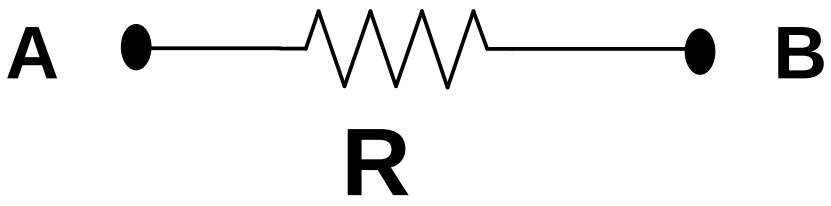
3-rd level metal connection to n-active with stacked vias

Interconnects

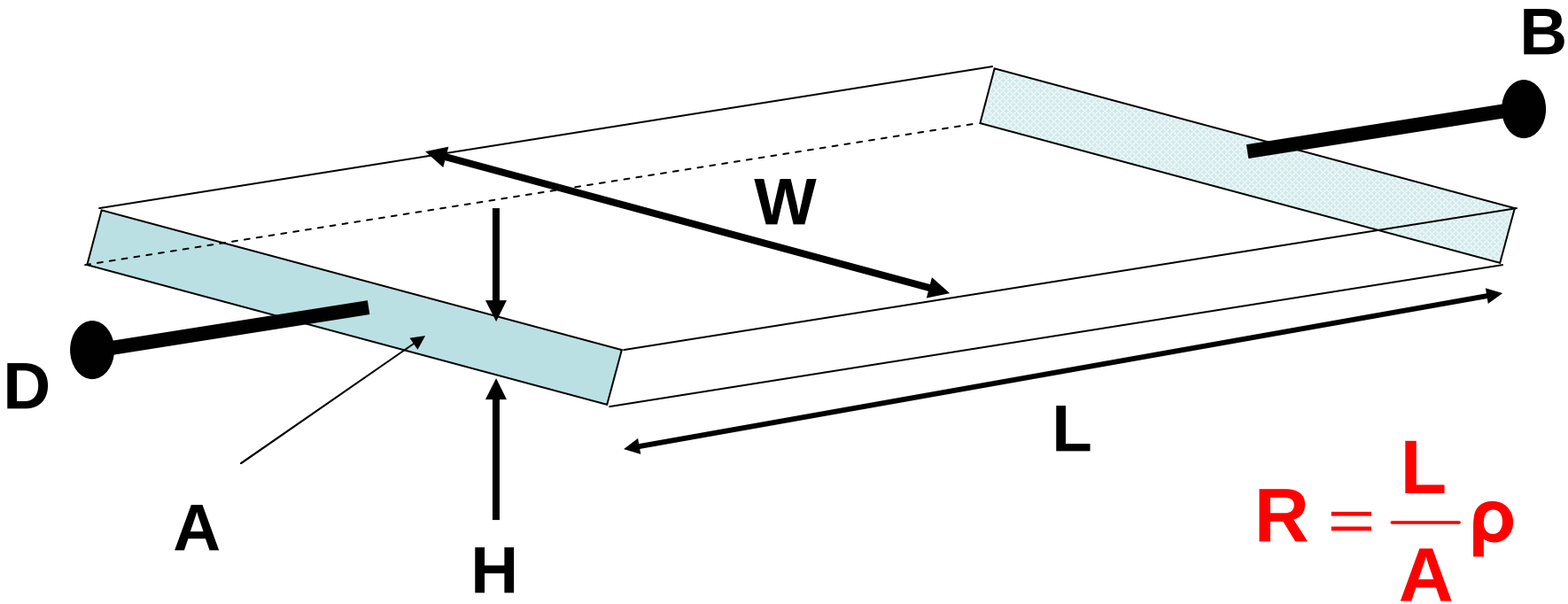
- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Resistance in Interconnects

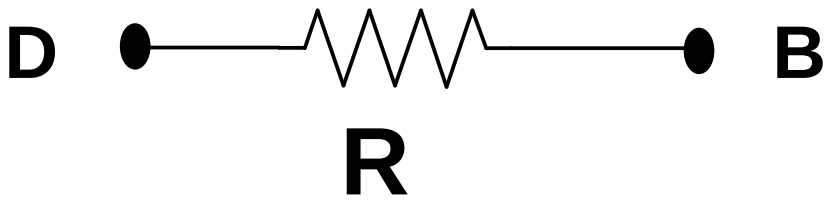




Resistance in Interconnects



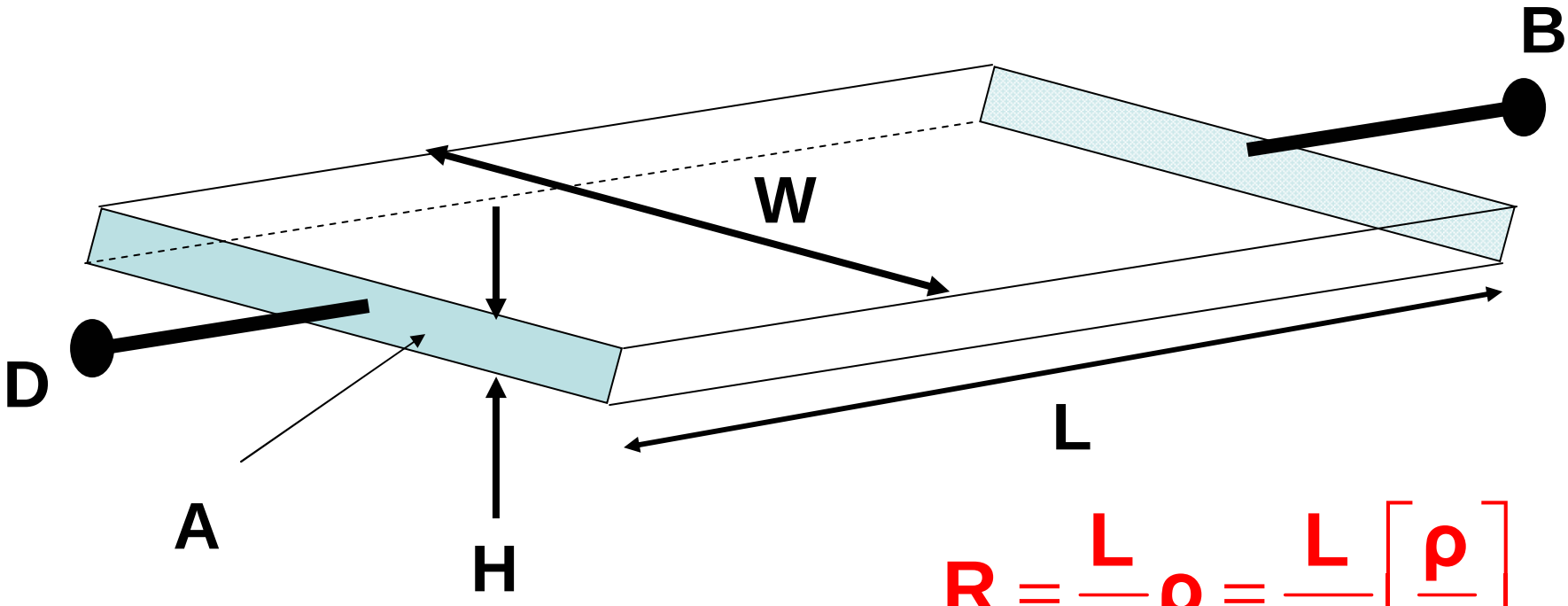
$$R = \frac{L}{A}\rho$$



A=HW

ρ independent of geometry and characteristic of the process

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

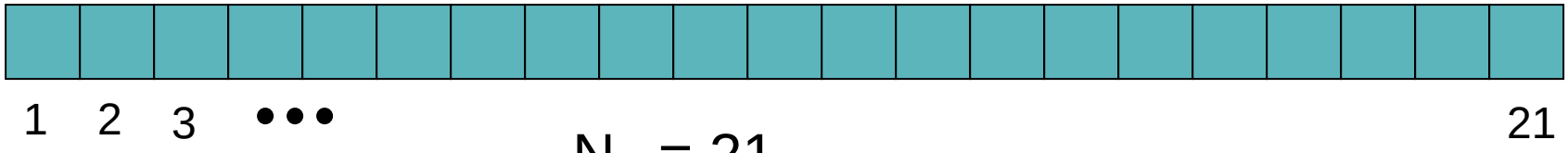
$R_{\square}=\rho/H$ $R=R_{\square}[L / W]$

Resistance in Interconnects

L

$$\mathbf{R = R_{\square}[L / W]}$$

The “Number of Squares” approach to resistance determination in thin films

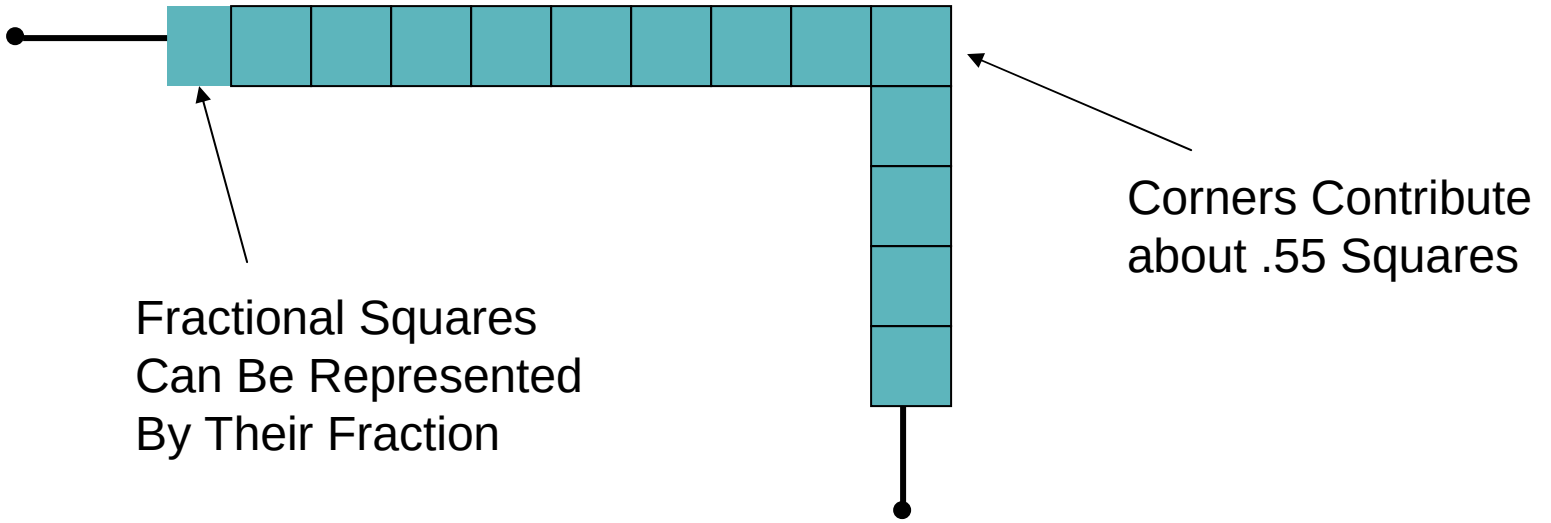


$N_S = 21$

$L / W = 21$

$$\mathbf{R = R_{\square} N_S}$$

Resistance in Interconnects



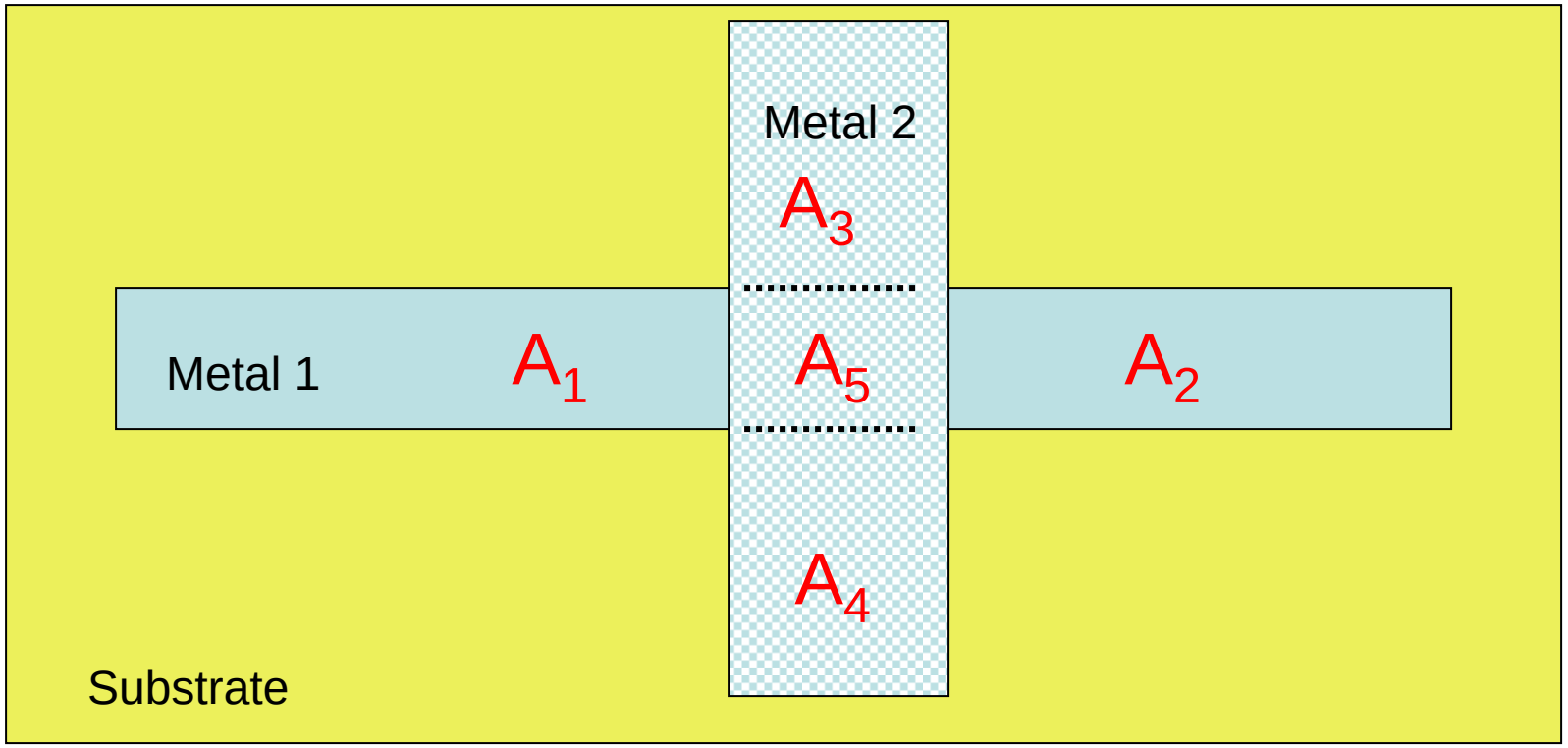
The “squares” approach is not exact but is good enough for calculating resistance in almost all applications

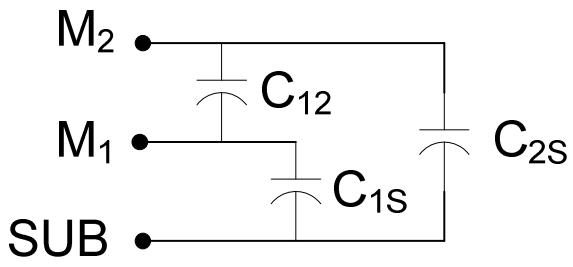
In this example:

$$N_S = 12 + .55 + .7 = 13.25$$

$$\mathbf{R = R_{\square} 13.25}$$

Capacitance in Interconnects





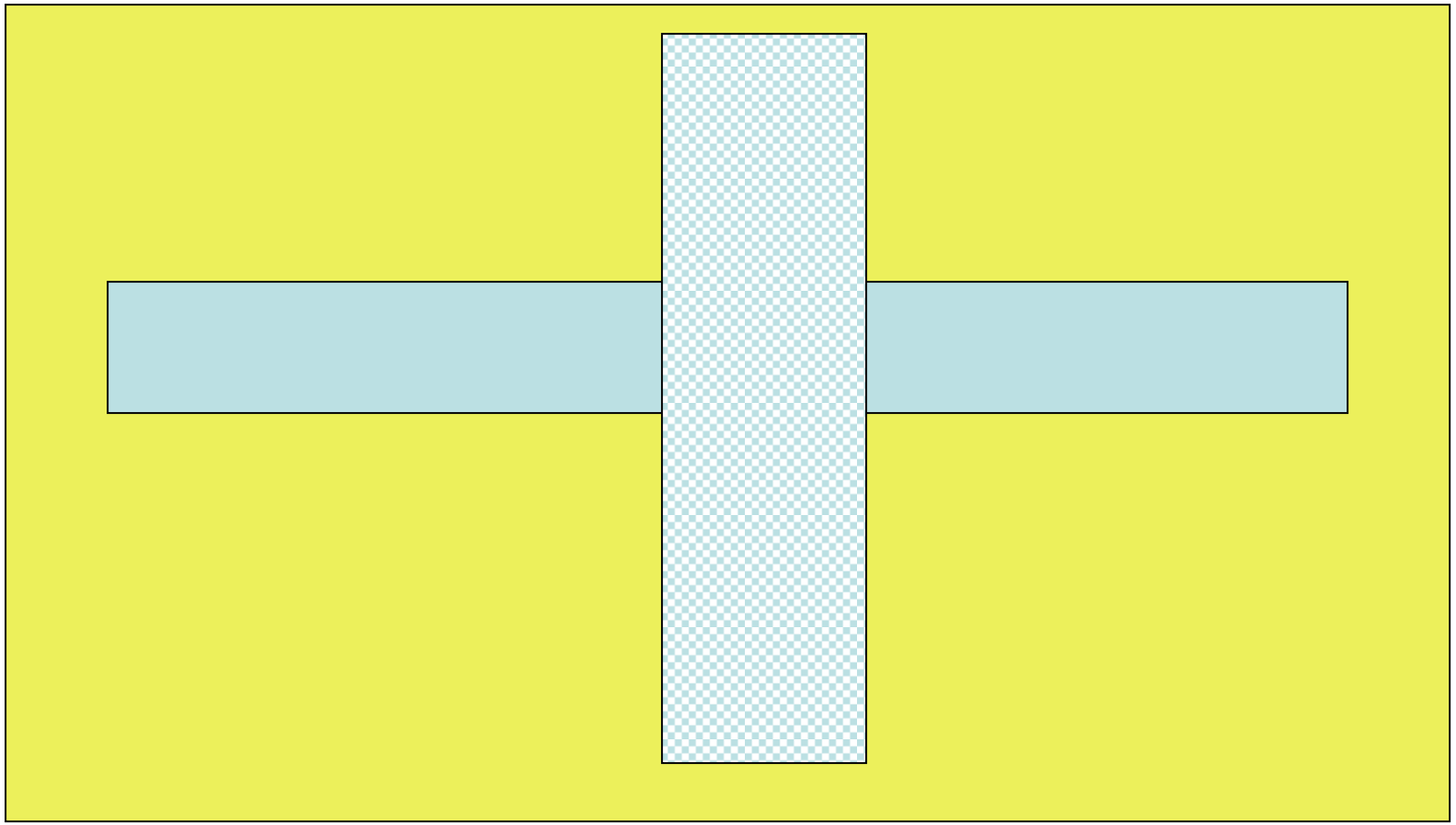
Equivalent Circuit

$$C_{12}=CD_{12}\,A_5$$

$$C_{1S}=CD_{1S}\,(A_1+A_2)$$

$$C_{2S}=CD_{2S}\,(A_3+A_4)$$

Capacitance in Interconnects



$C=C_DA$

C_D is the capacitance density and A is the area of the overlap

Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quility layers in subsequent processing steps
  - Mechanically planarized