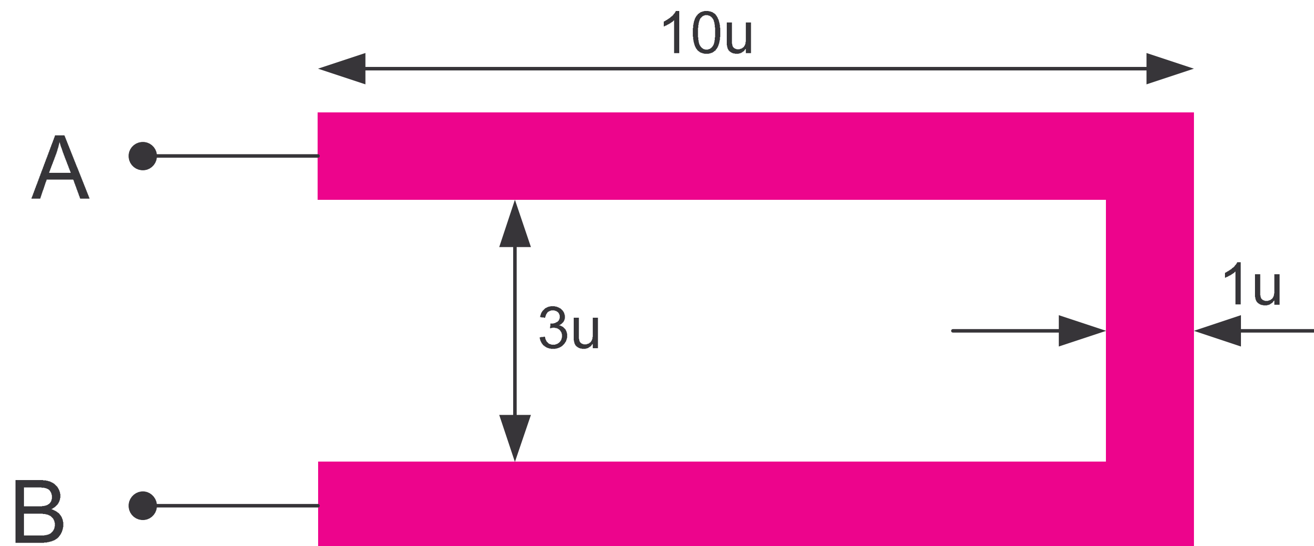
EE 434
Lecture 9

IC Fabrication Technology

Quiz 7

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 Ω/□, determine the resistance between nodes A and B.



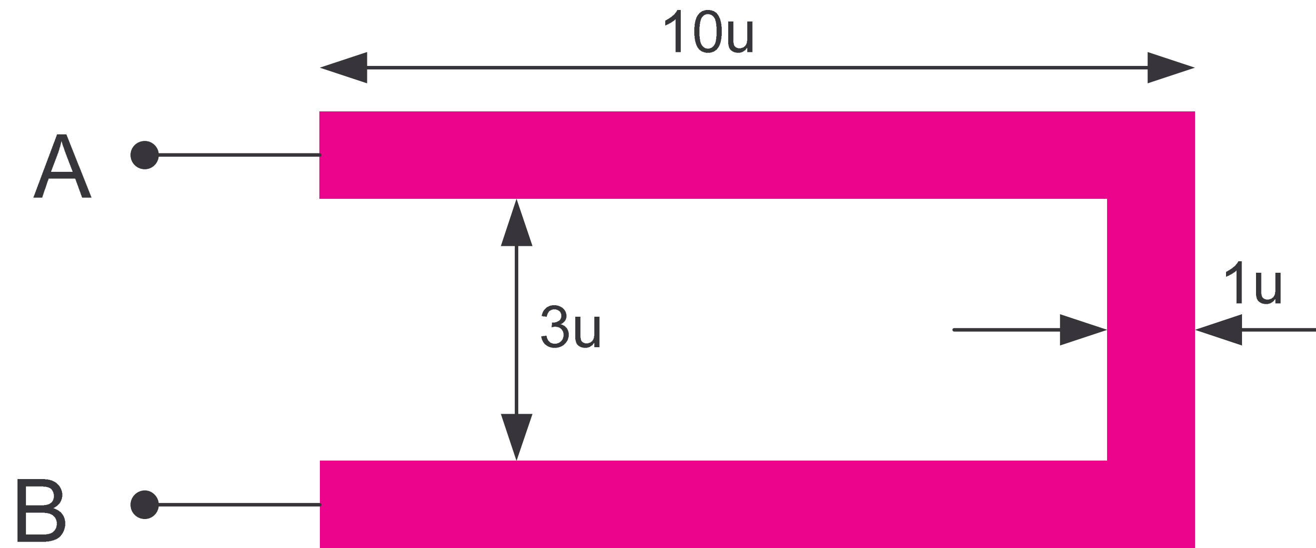
And the number is ….

1 8 7 5 3

6 9 4 2

5

Quiz 7 Solution



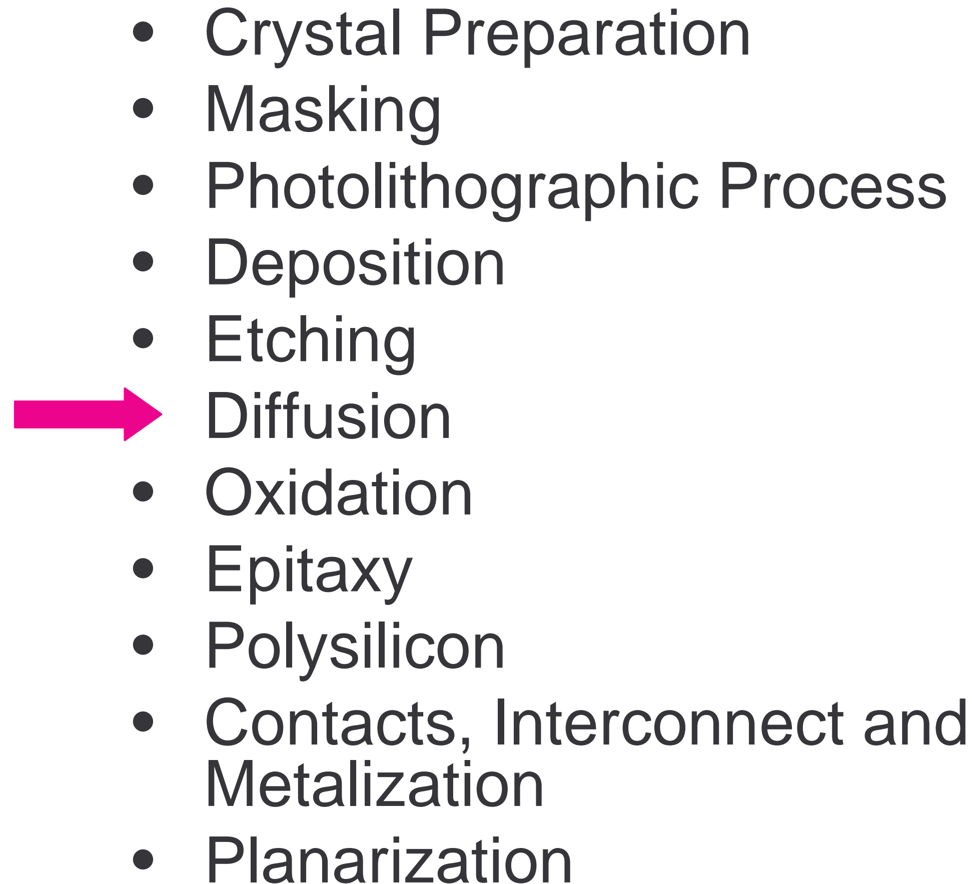
$N_S = 9+9+3+2(.55)=22.1$

$R_{AB}=R_{\square}N_S=40x22.1=884\Omega$

Review from Last Time

- Silicon Wafers made by pulling silicon crystals from molten silicon
- Mask costs are high for state of the art processes (over $1M) and mask quality is critical
- Reticles rather than masks are regularly used although distinction in terminology between mask and reticle is usually not made
- Etching used to selectively remove materials during processing
  - Wet etches
  - Dry etches
- Photolithographic process is used repeatedly in existing IC fabrication flows
- Thin films characterized by sheet resistance form resistors that may be desired or unwanted

IC Fabrication Technology

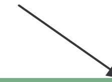


Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800^oC to 1200^oC
- Source of Impurities
  - Deposition
  - Ion Implantation
    - Only a few A^o deep
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion

Diffusion

Source of Impurities Deposited on Silicon Surface

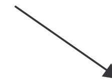


Before Diffusion

After Diffusion

Diffusion

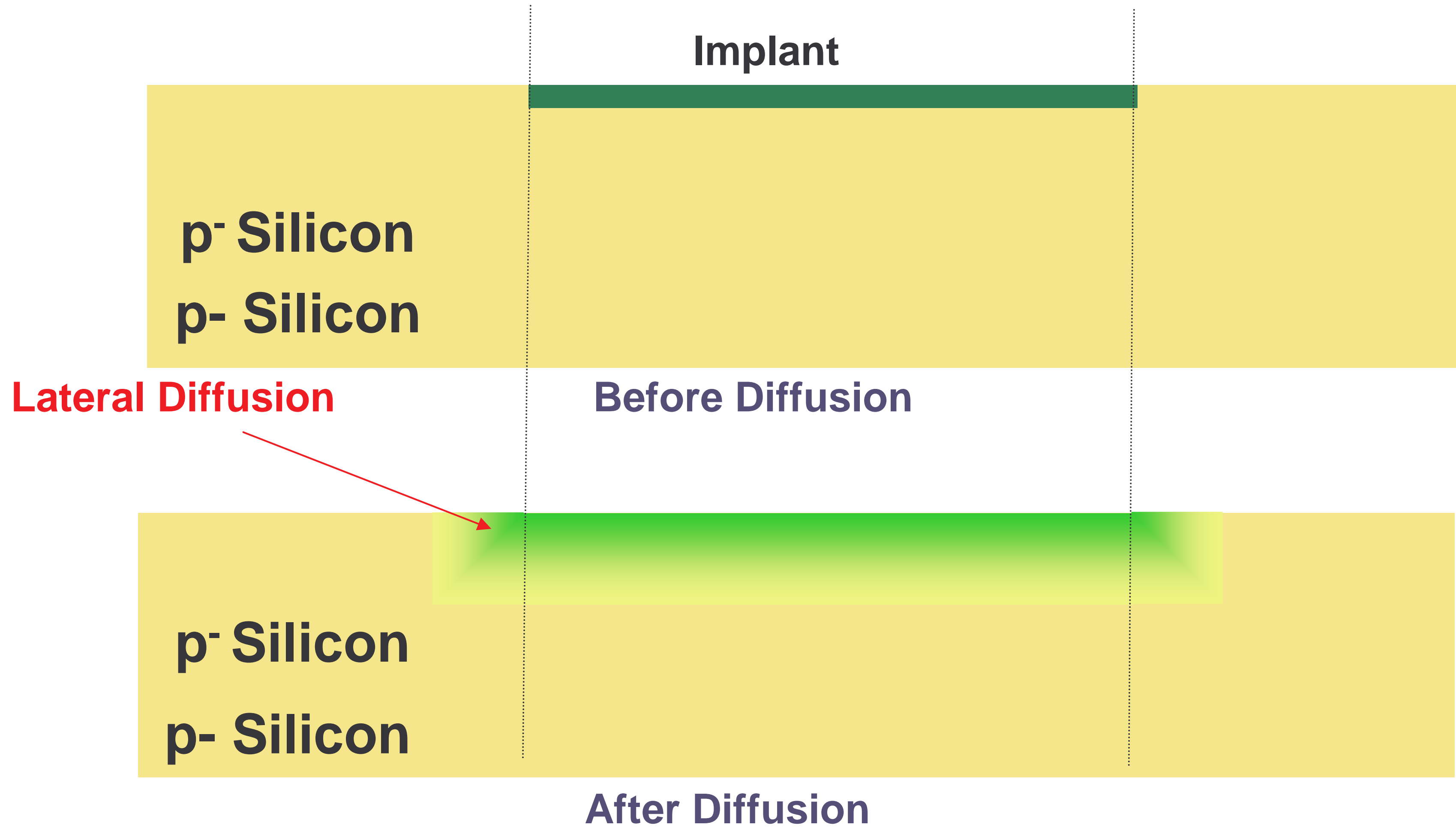
Source of Impurities Implanted in Silicon Surface



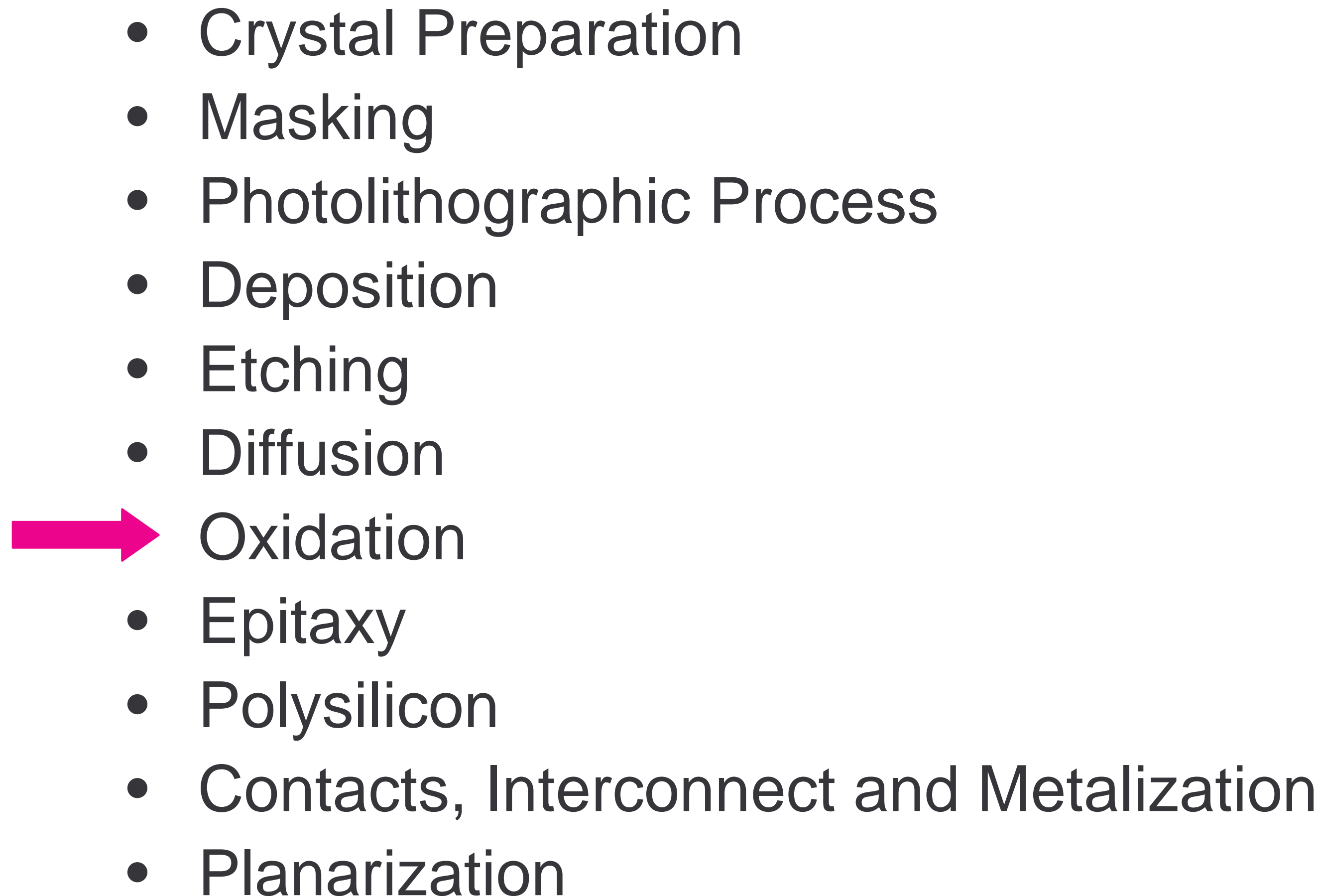
Before Diffusion

After Diffusion

Diffusion



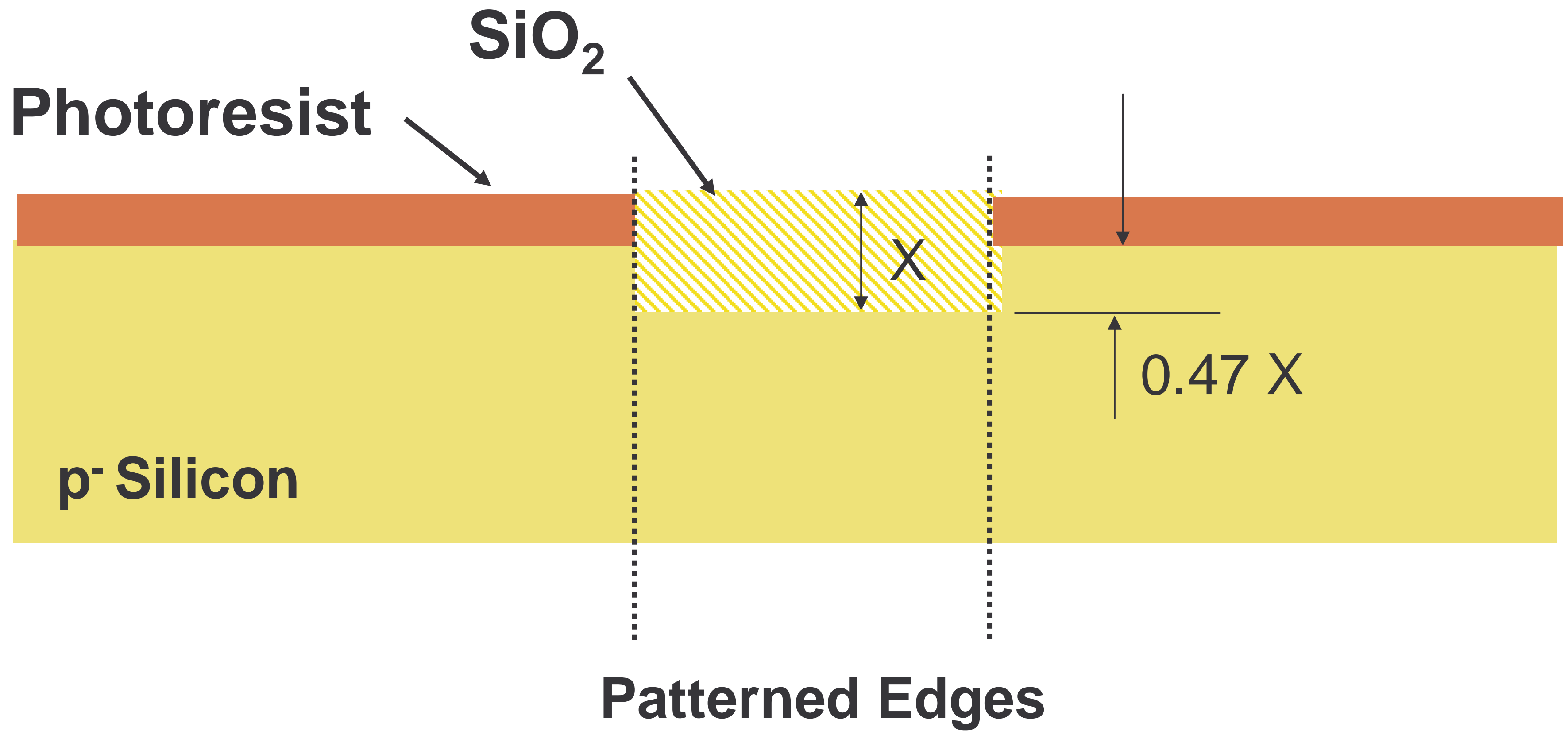
IC Fabrication Technology



Oxidation

- SiO_2 is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO_2 consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO_2 on materials other than Si

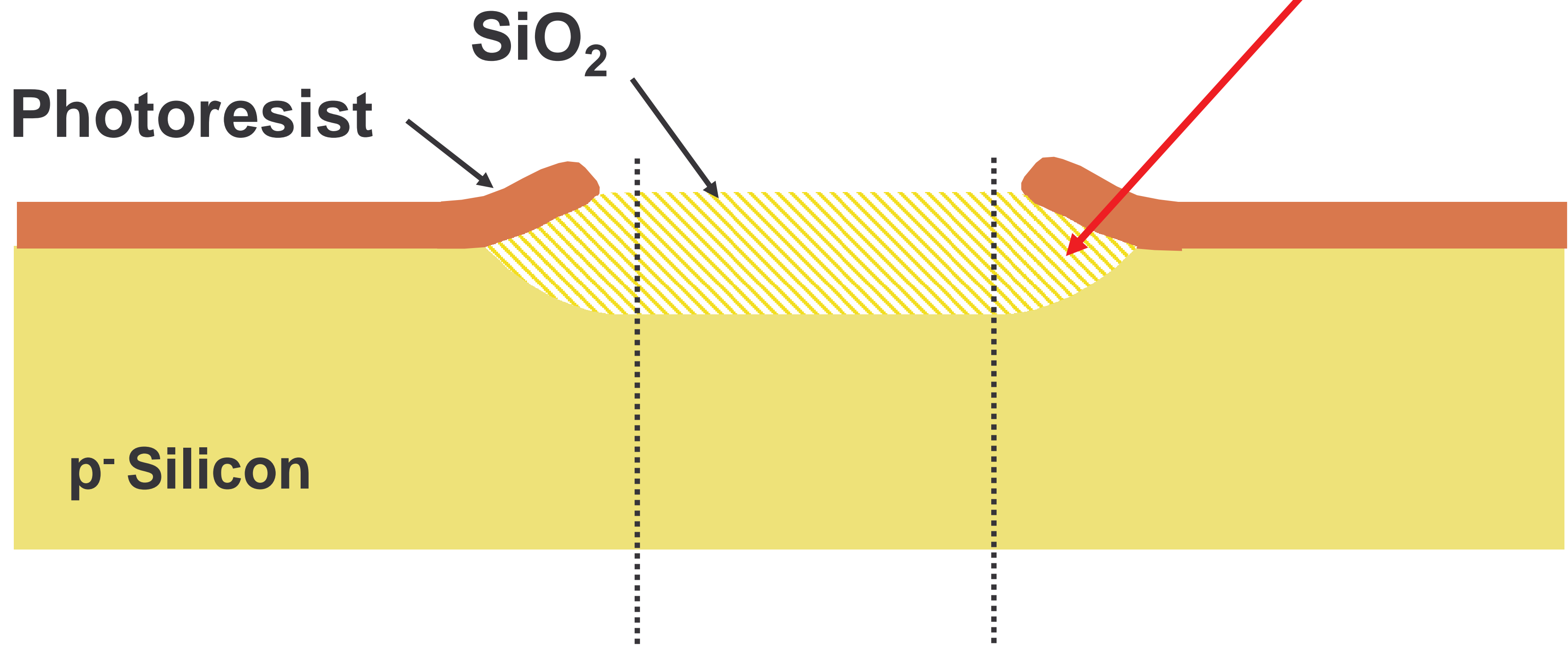
Oxidation



Thermally Grown SiO_2 - desired growth

Oxidation

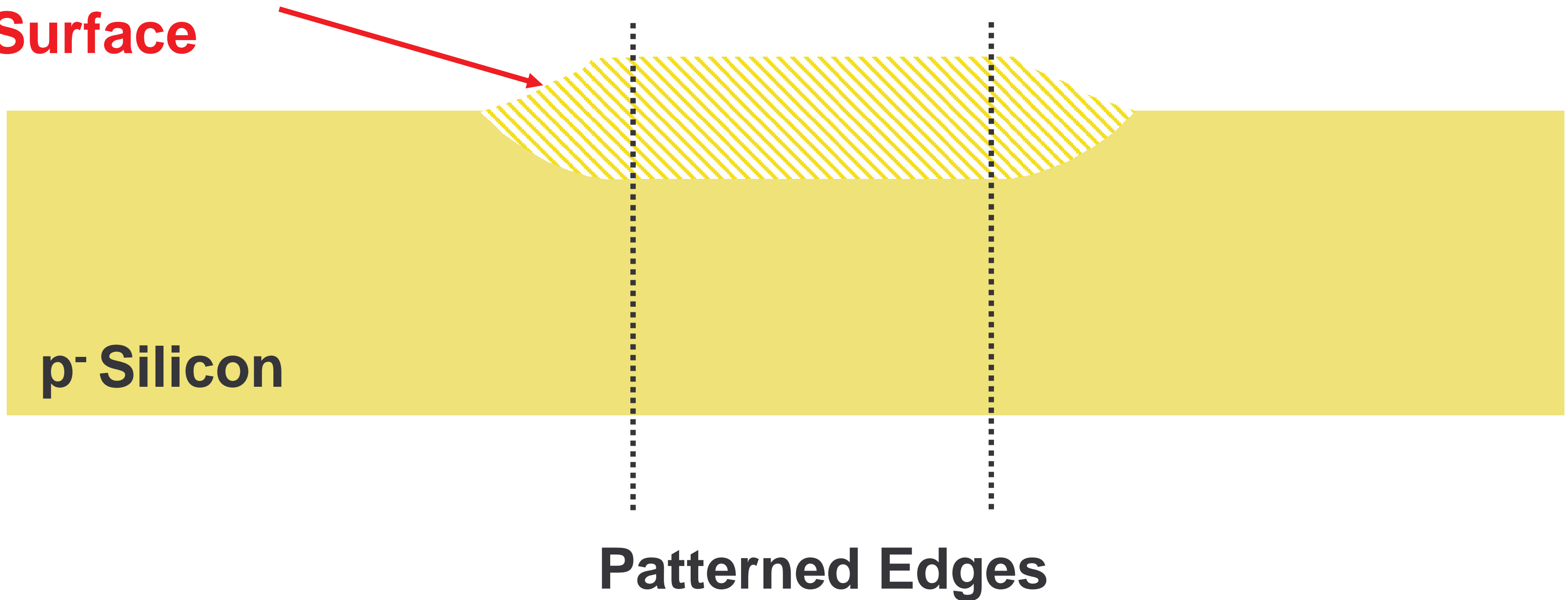
Bird's Beaking



Patterned Edges

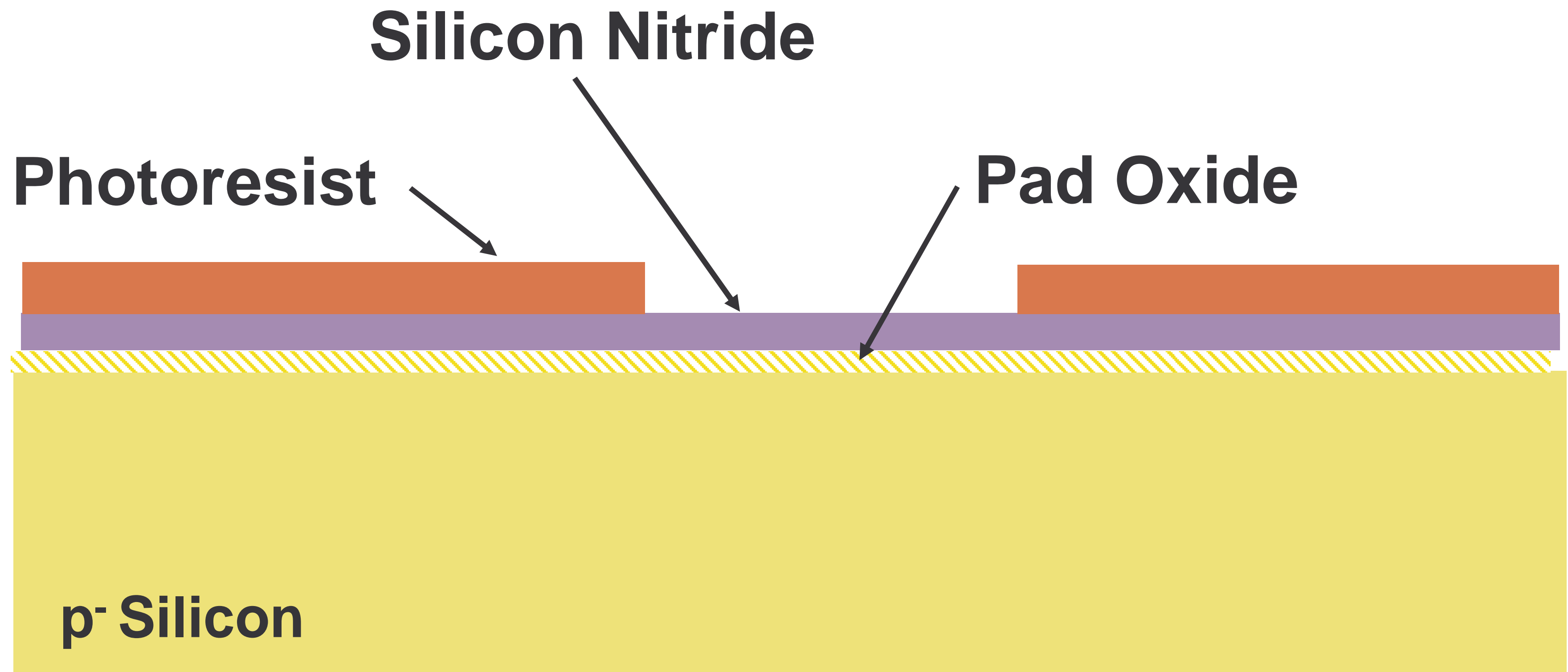
Thermally Grown SiO_2 - actual growth

Oxidation



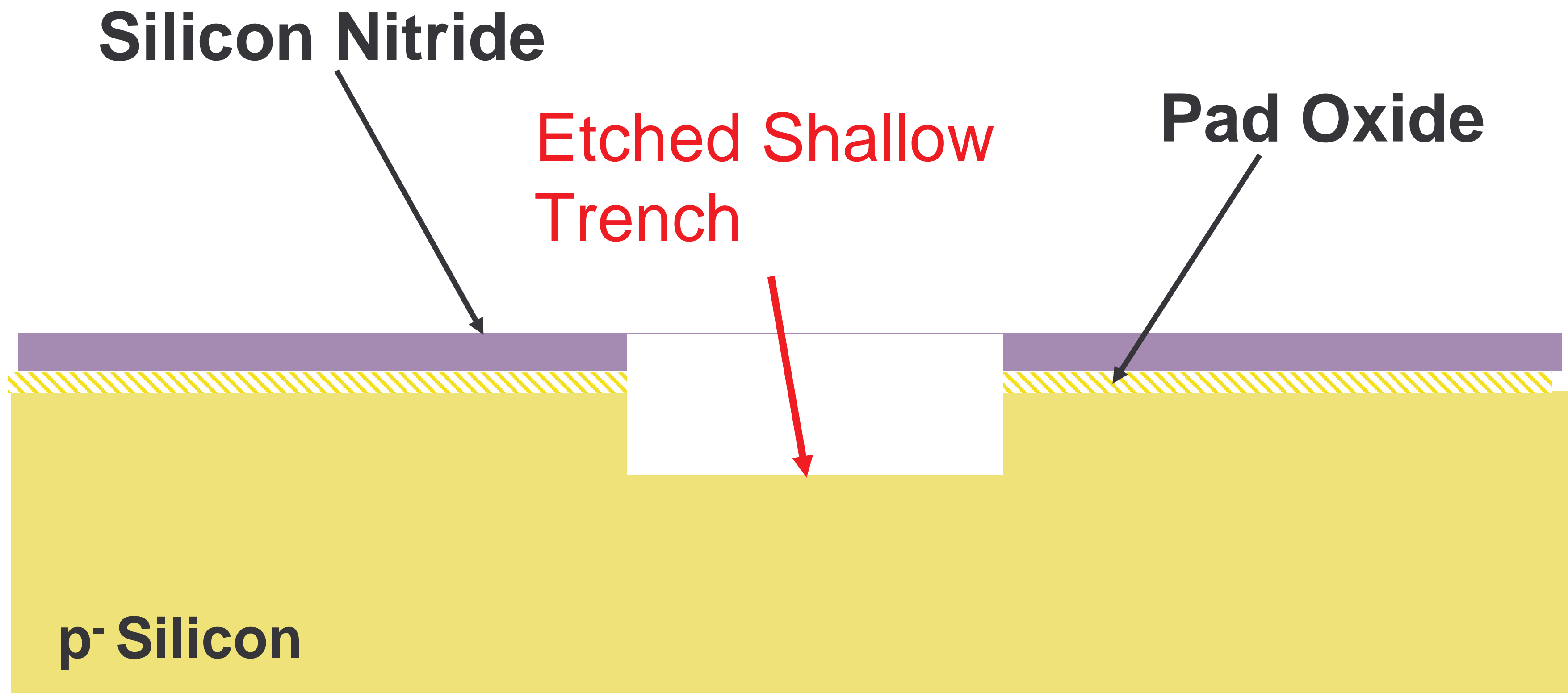
Thermally Grown SiO_2 - actual growth

Oxidation



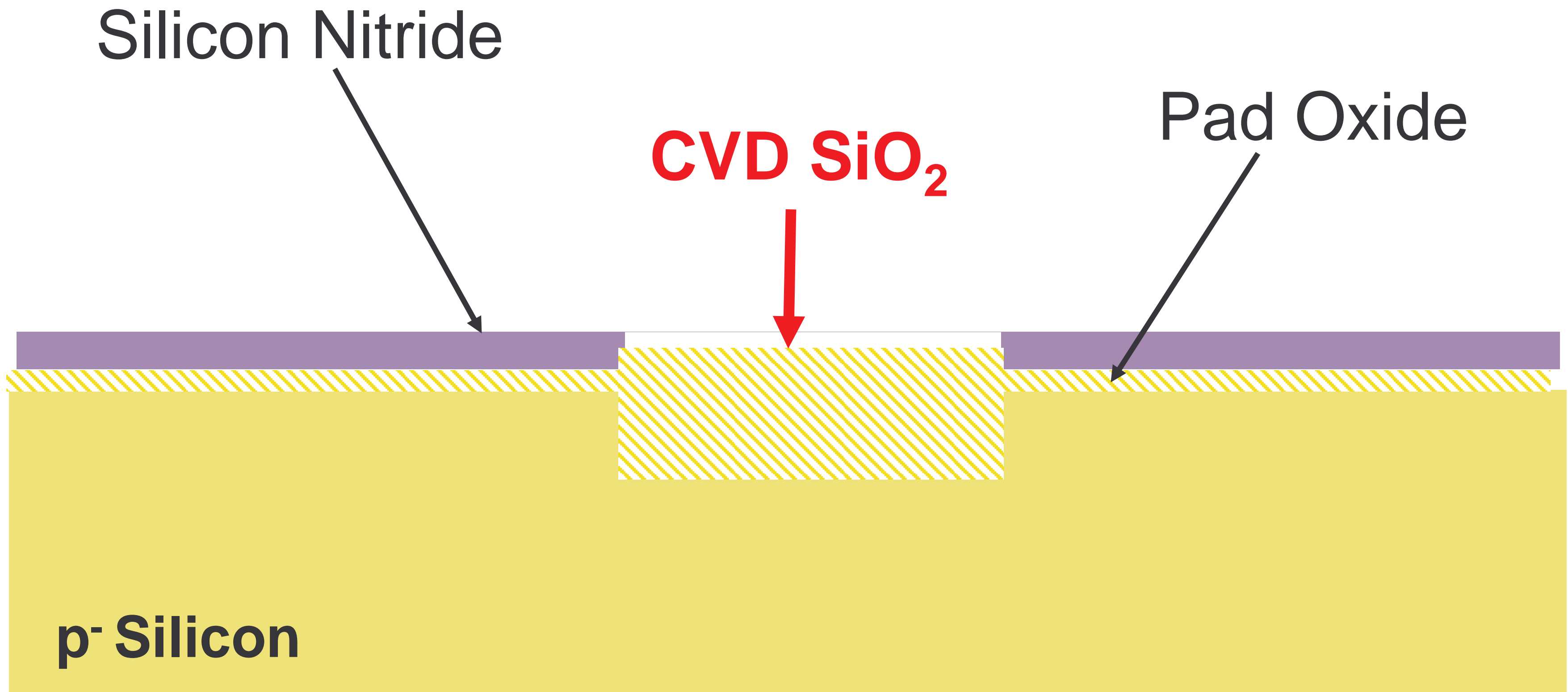
Shallow Trench Isolation (STI)

Oxidation



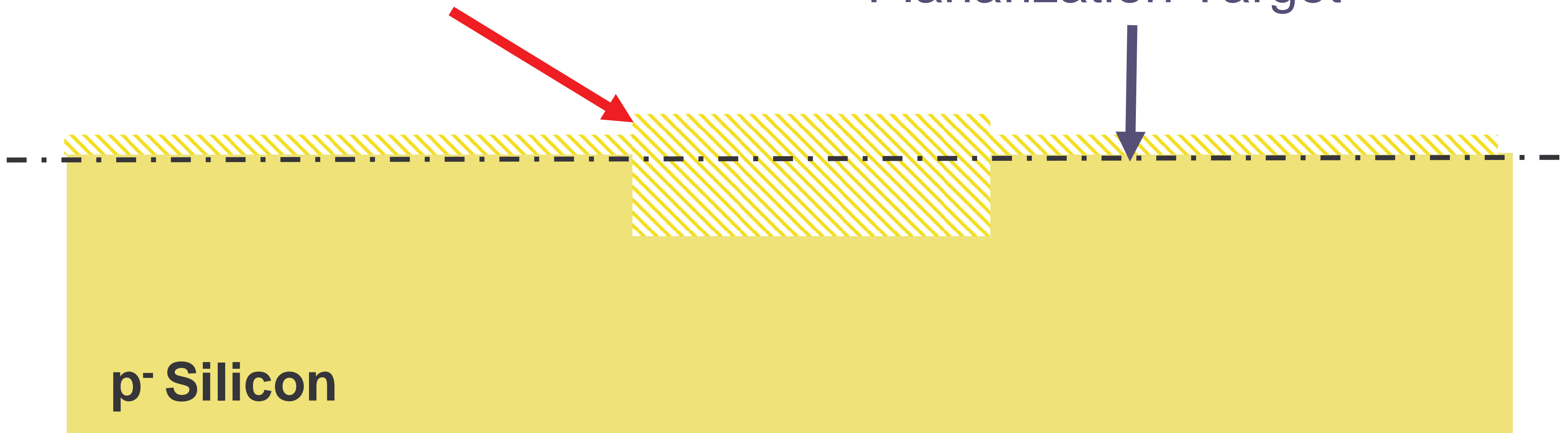
Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

Oxidation

After Planarization

Shallow Trench Isolation (STI)

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Epitaxy

- Single Crystaline Extension of Substrate Crystal
  - Commonly used in bipolar processes
  - CVD techniques
  - Impurities often added during growth
  - Grows slowly to allow alignmnt with substrate

Epitaxy

epi can be uniformly doped or graded

Question: Why can't a diffusion be used to create the same effect as an epi layer ?

IC Fabrication Technology

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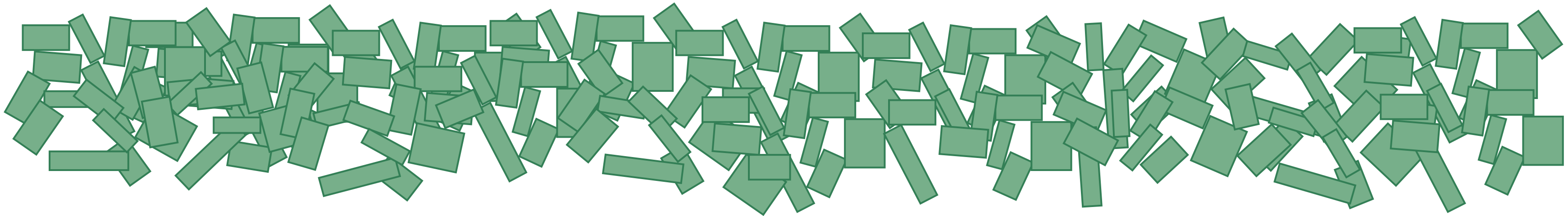
Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)

Polysilicon



Polysilicon

Single-Crystaline Silicon

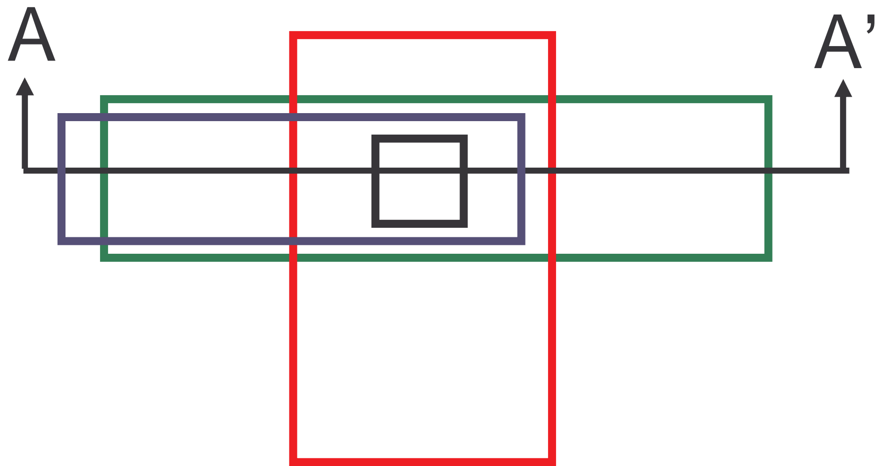
IC Fabrication Technology

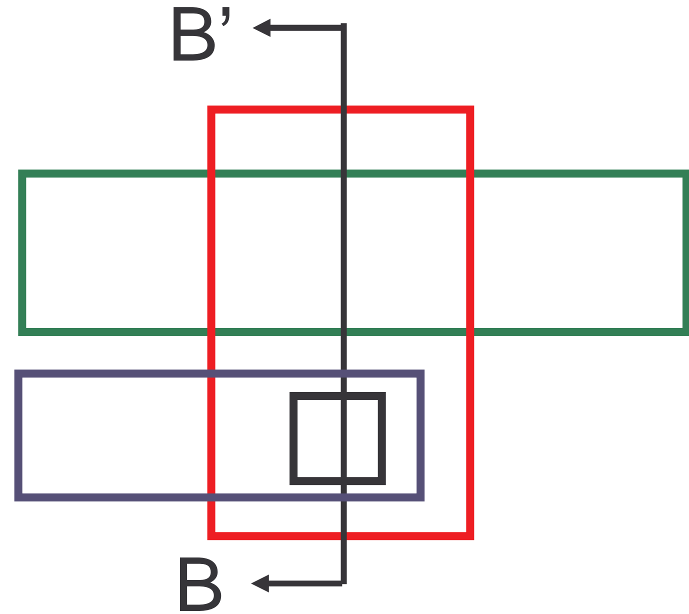
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- ➡ Contacts, Interconnect and Metalization
- Planarization

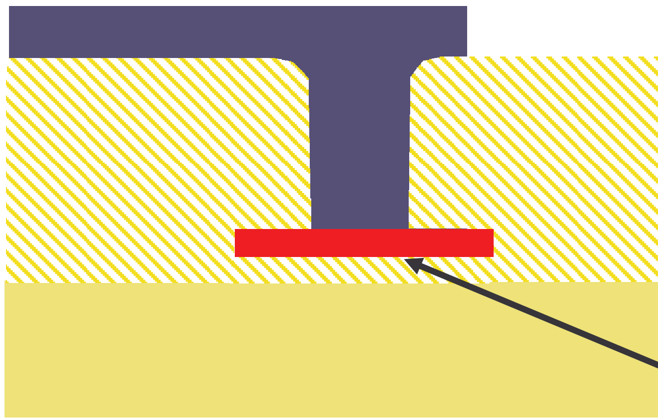
Contacts, Interconnect and Metalization

- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

Contacts





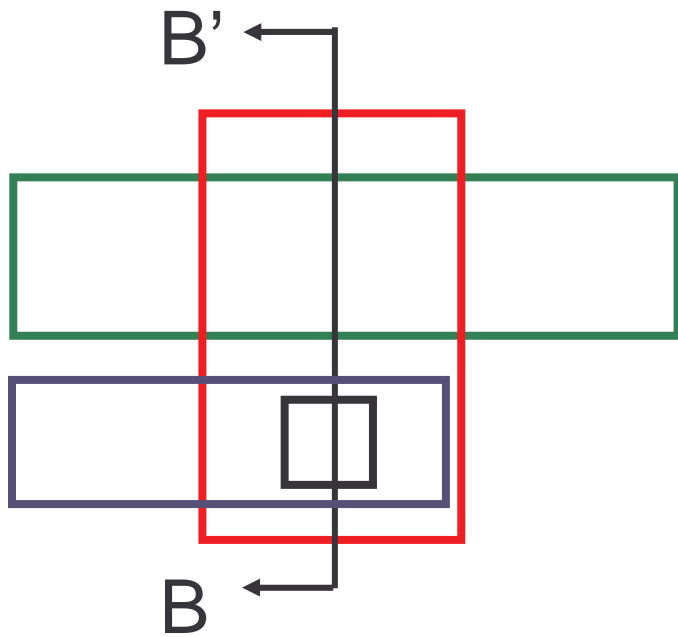


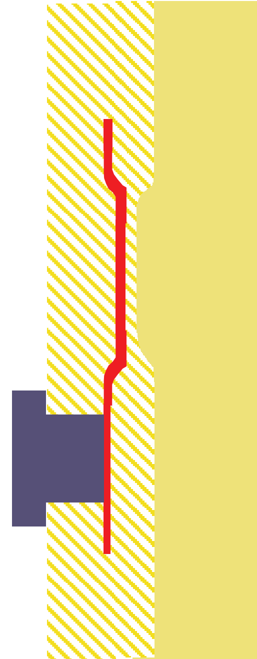
Acceptable Contact

Unacceptable Contact

Vulnerable
to pin holes

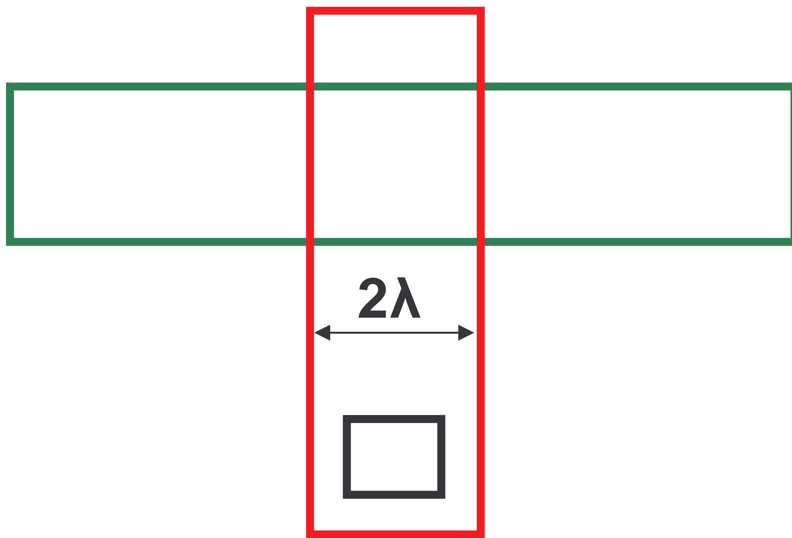
Contacts

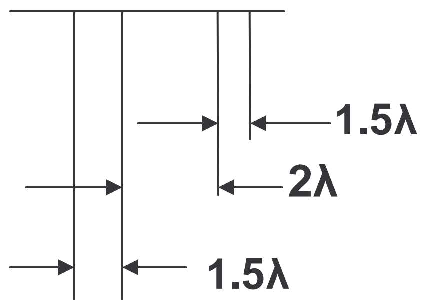




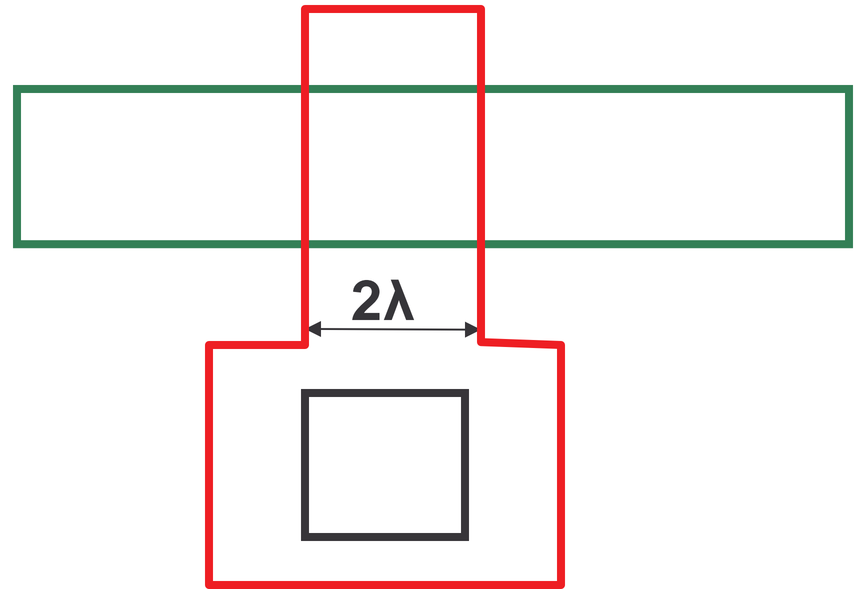
Acceptable Contact

Contacts



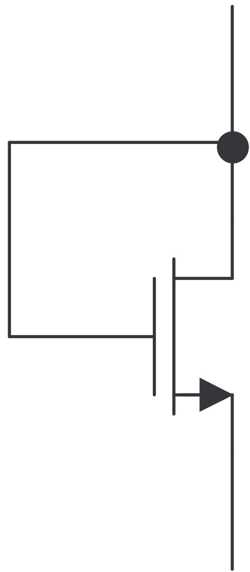


Design Rule Violation

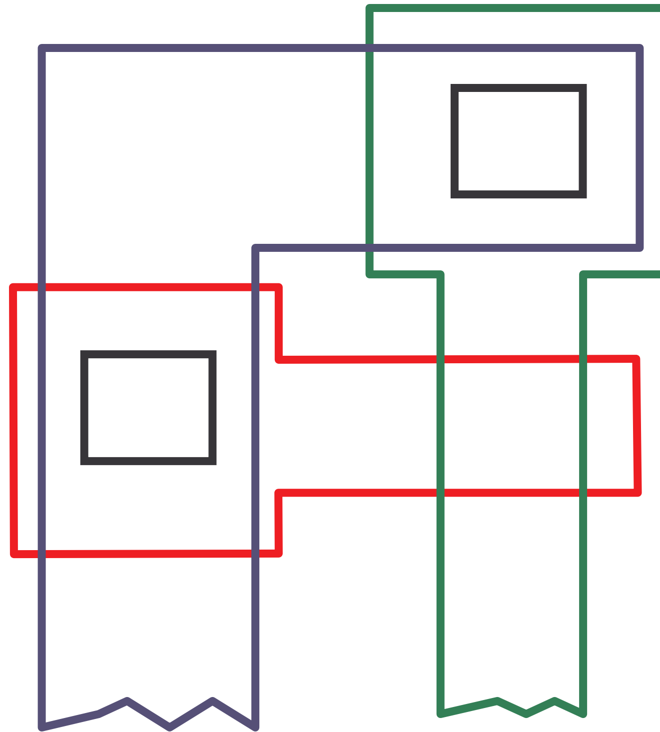


“Dog Bone” Contact

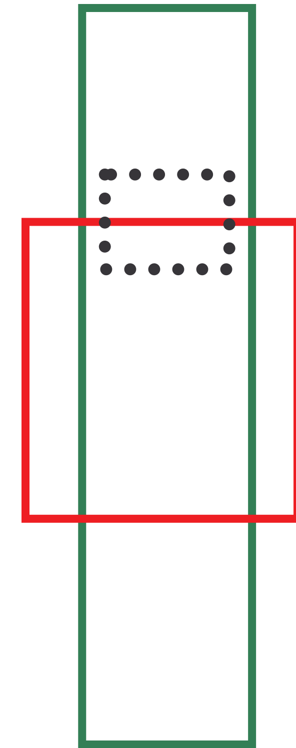
Contacts



Common Circuit Connection



Standard Interconnection



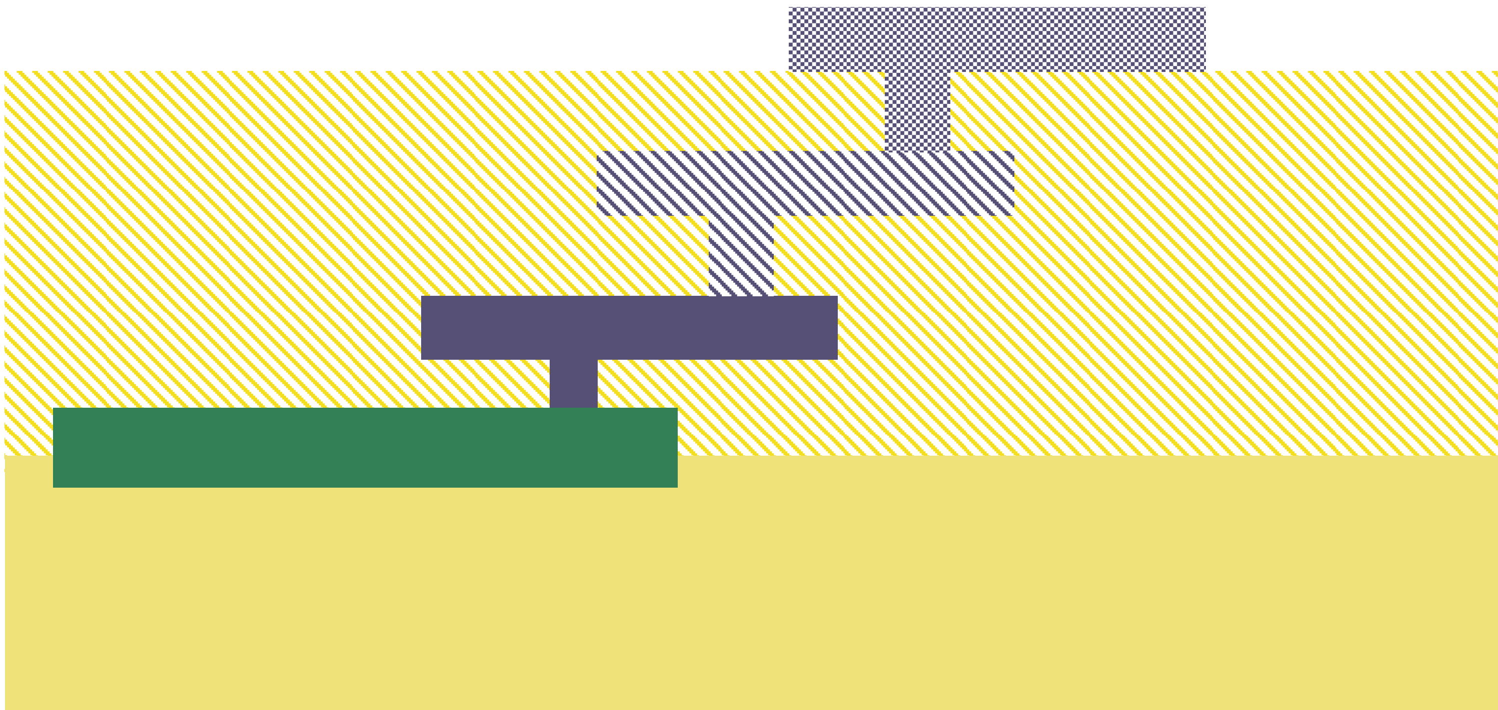
Buried Contact

Can save area but not allowed in many processes

Metalization

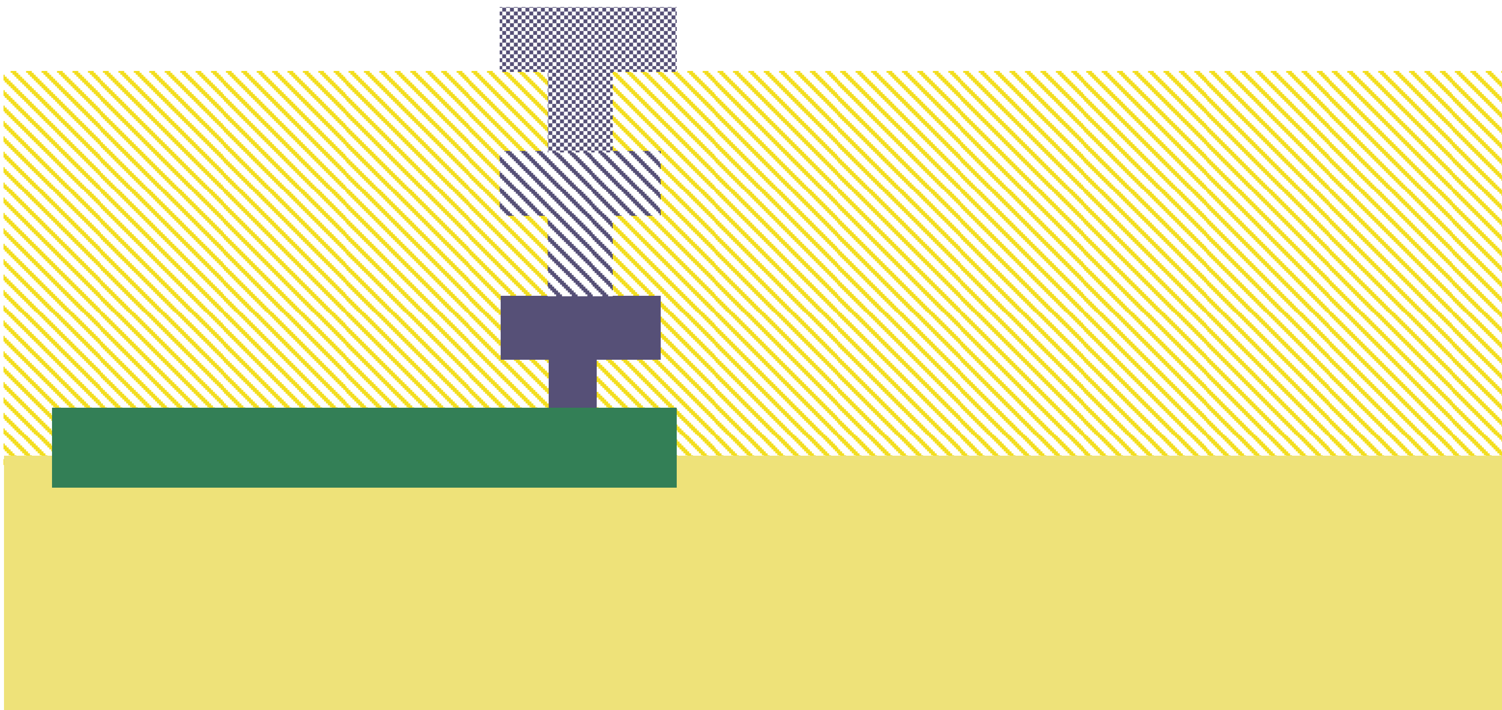
- Aluminum widely used for interconnect
- Copper finding some applications
- Must not exceed maximum current density
  - around 1ma/u
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Multiple Level Interconnects



3-rd level metal connection to n-active without stacked vias

Multiple Level Interconnects

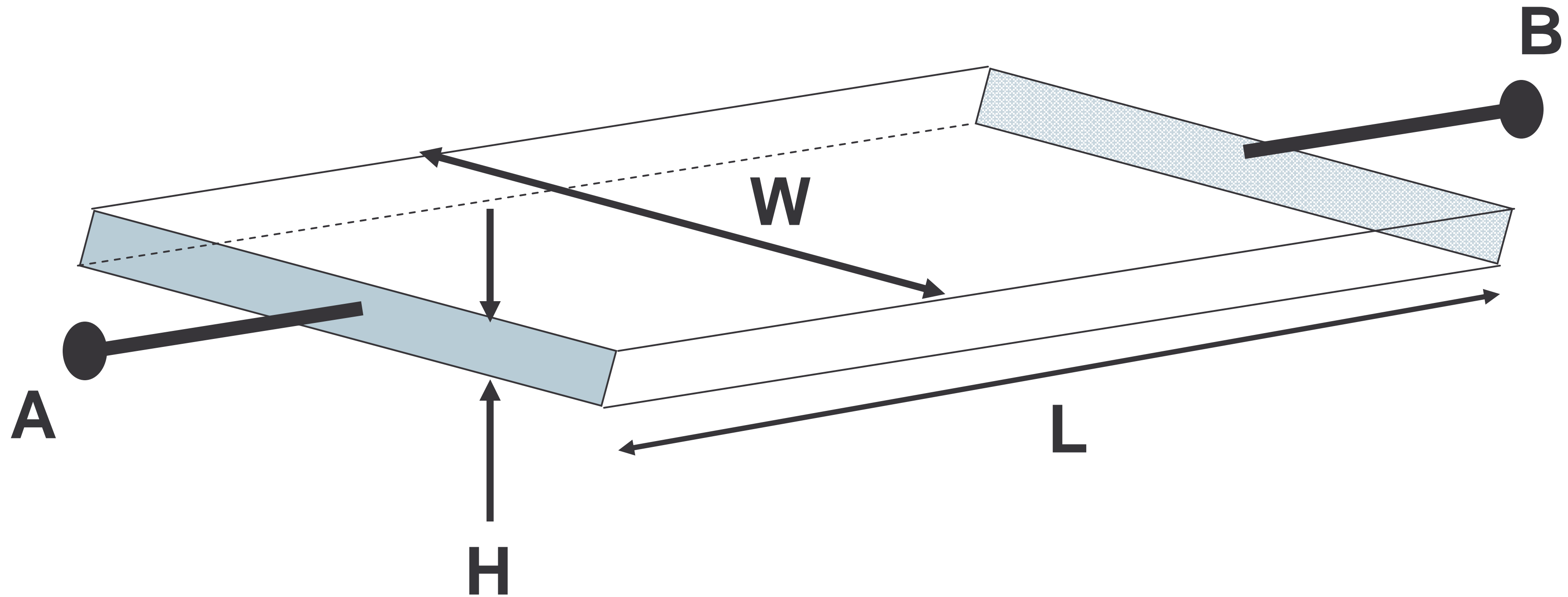


3-rd level metal connection to n-active with stacked vias

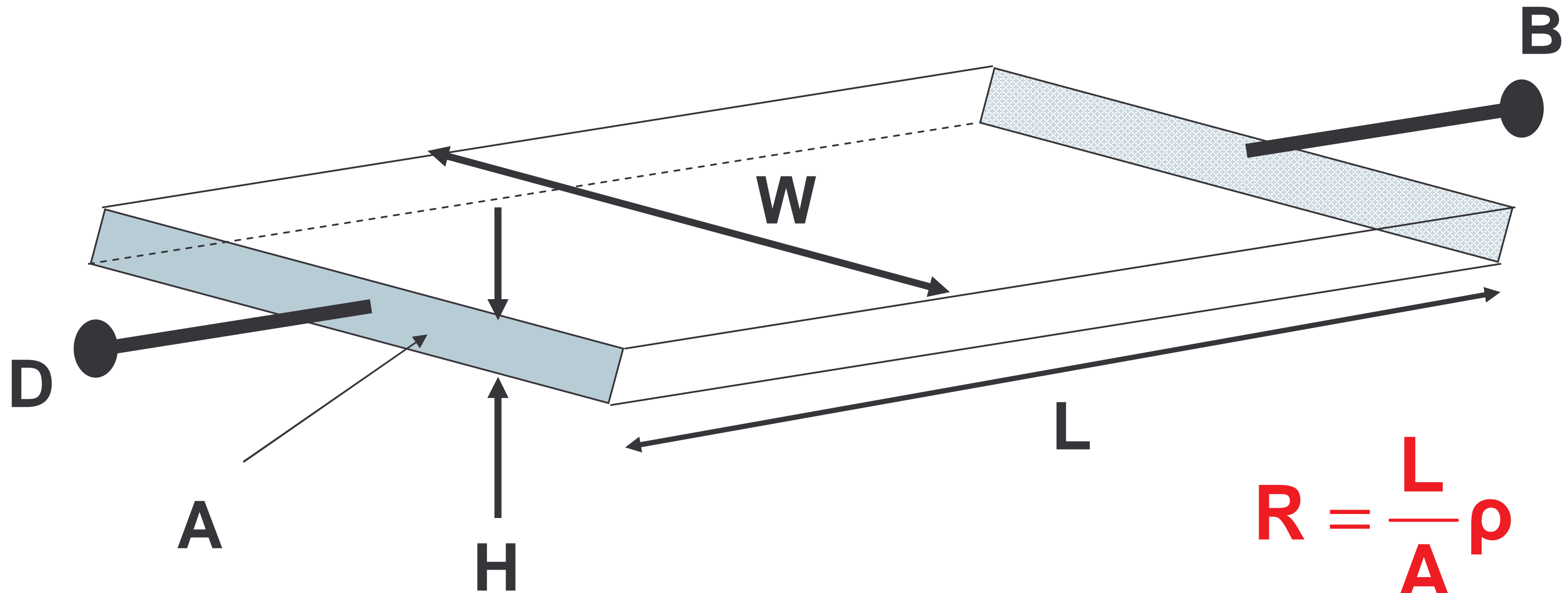
Interconnects

- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Resistance in Interconnects



Resistance in Interconnects

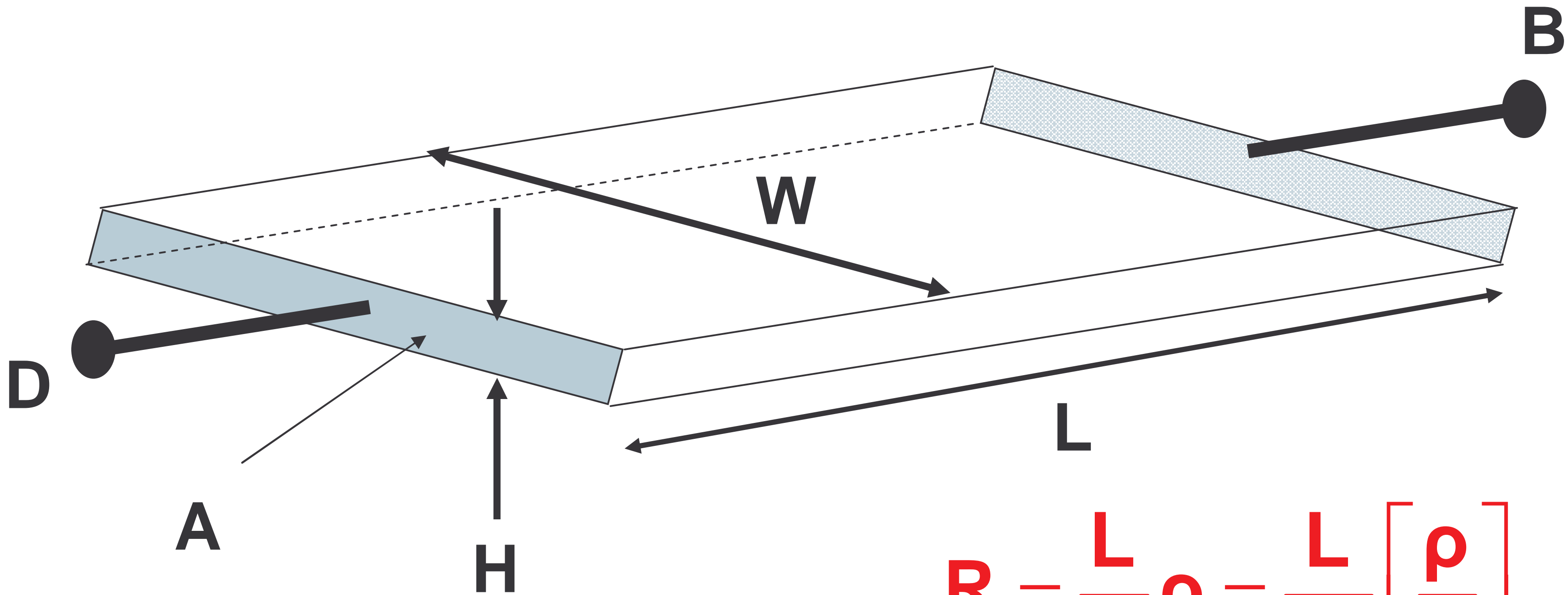


$$R = \frac{L}{A}\rho$$

$A = HW$

ρ independent of geometry and characteristic of the process

Resistance in Interconnects



$$R = \frac{L}{A}\rho = \frac{L}{W}\left[\frac{\rho}{H}\right]$$

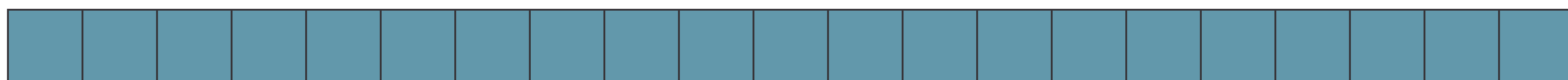
H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

$R_{\square} = \rho / H$ $\quad$ $R = R_{\square}[L / W]$

Resistance in Interconnects

$$R = R_{\square}[L / W]$$

The “Number of Squares” approach to resistance determination in thin films



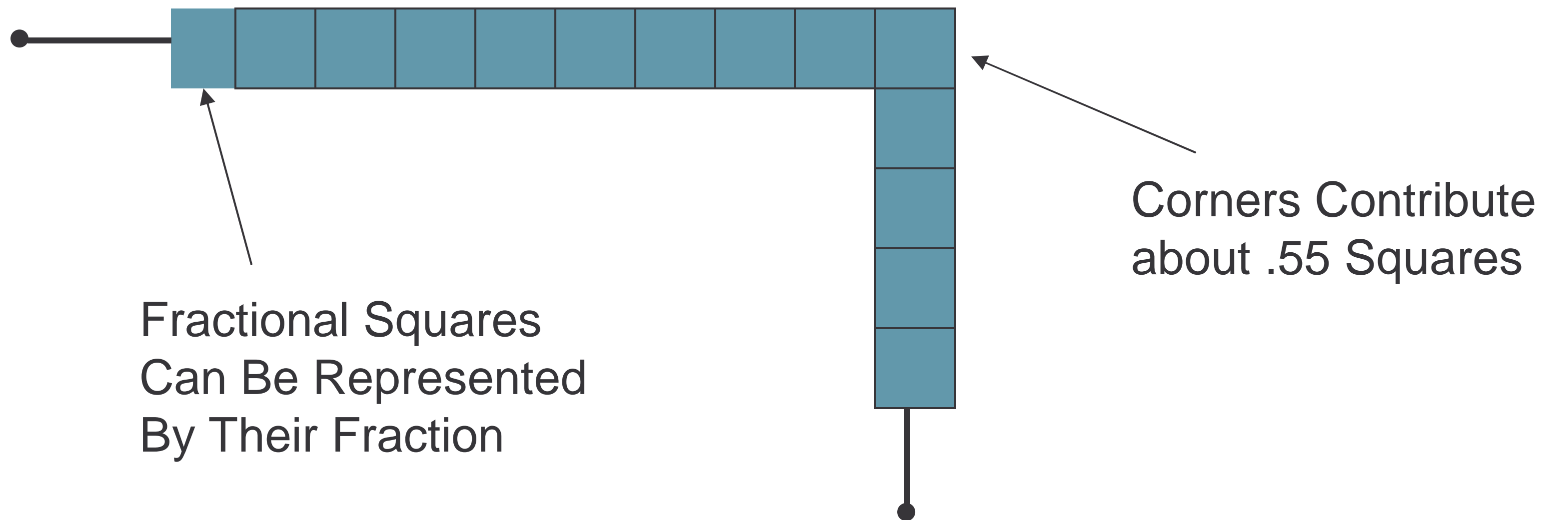
1 2 3 • • • 21

$N_S = 21$

$L / W = 21$

$$R = R_{\square} N_S$$

Resistance in Interconnects



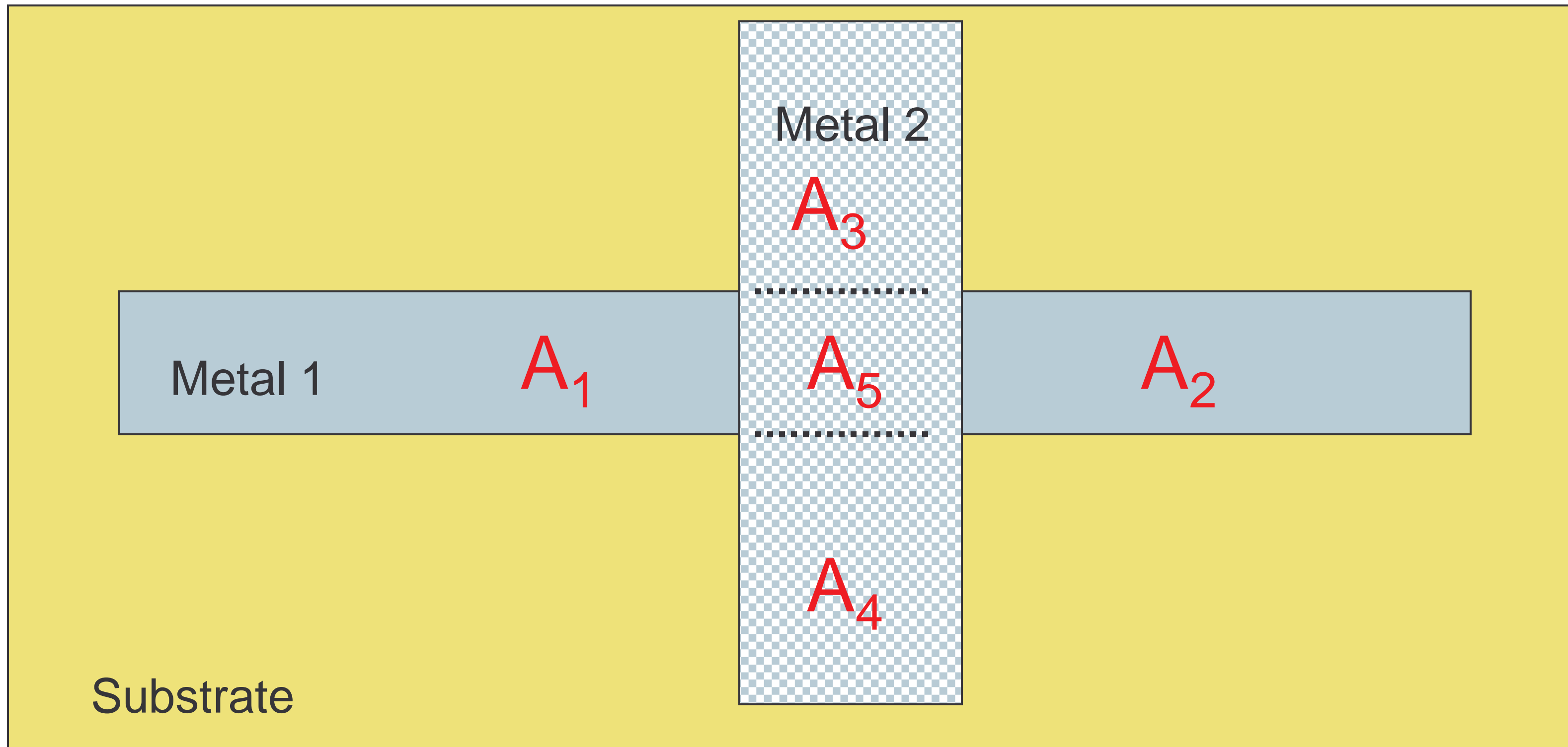
The “squares” approach is not exact but is good enough for calculating resistance in almost all applications

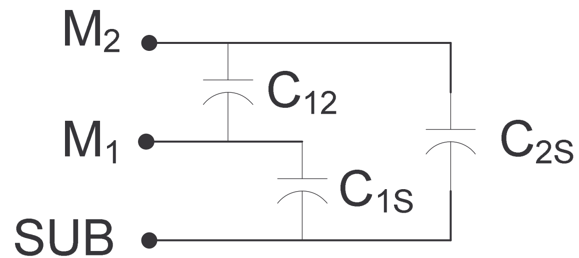
In this example:

$$N_S=12+.55+.7=13.25$$

$$\mathbf{R=R_{\square}13.25}$$

Capacitance in Interconnects





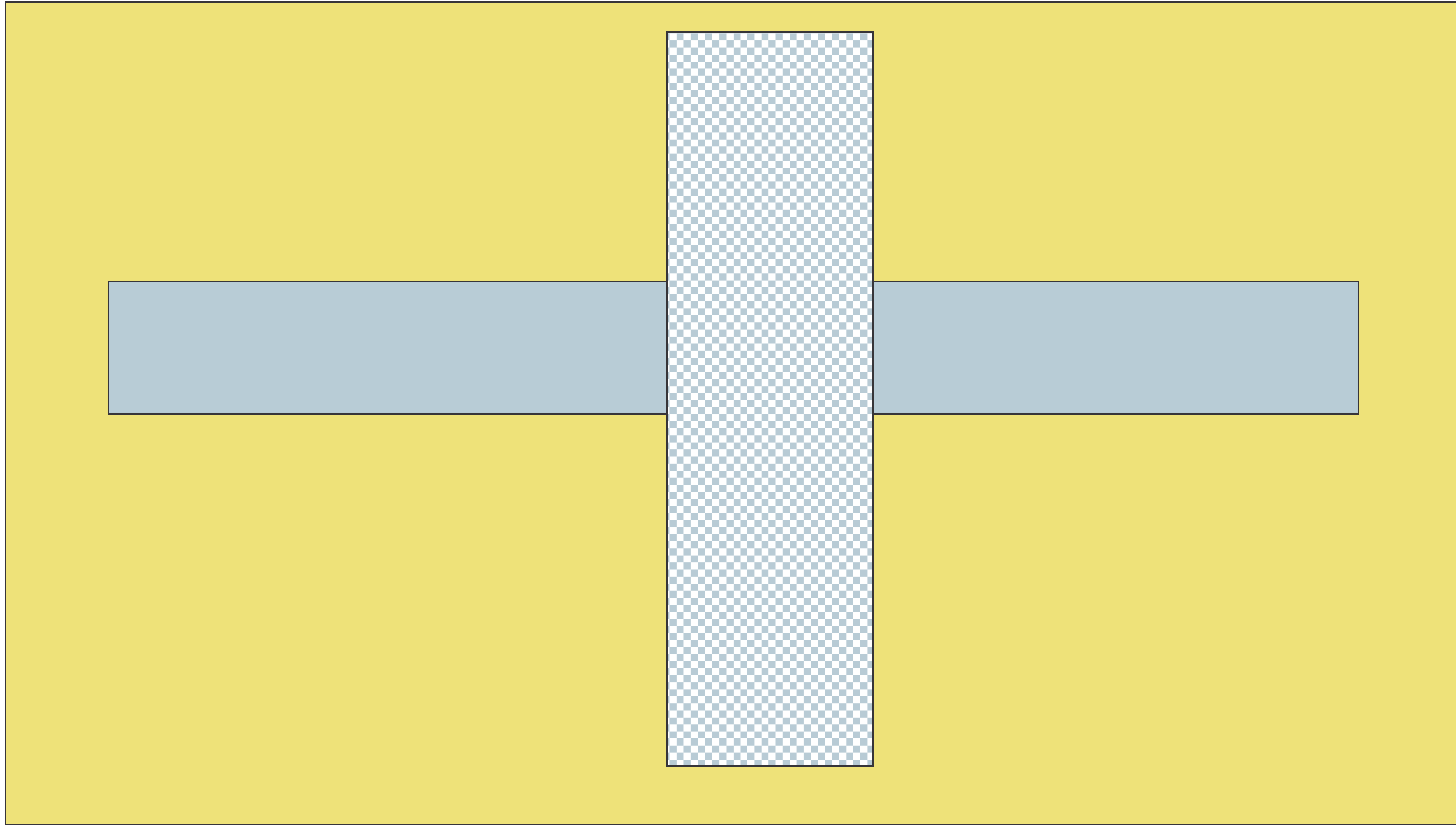
Equivalent Circuit

$$C_{12}=CD_{12}\,A_5$$

$$C_{1S}=CD_{1S}\,(A_1+A_2+A_5)$$

$$C_{2S}=CD_{2S}\,(A_3+A_4)$$

Capacitance in Interconnects



$$C = C_D A$$

C_D is the capacitance density and A is the area of the overlap

Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org

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Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quility layers in subsequent processing steps
  - Mechanically planarized