EE 434
Lecture 10

Process Flow (animated)
Backend Processing Steps
Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from $M_1$ to substrate of $0.05 \text{fF}/\mu\text{m}^2$, from $M_1$ to $M_2$ of $0.07 \text{fF}/\mu\text{m}^2$ and from $M_2$ to substrate of $0.025 \text{fF}/\mu\text{m}^2$. 

\[ \text{Capacitance} = \int \frac{dQ}{dV} = \int \frac{	ext{charge}}{	ext{voltage}} \]
And the number is ....

1 8 7 5 3
6 9 4 2
The capacitance density from $M_1$ to $M_2$ is $0.07 \text{fF/\mu}^2$

$$A_{C1C2} = (20 \mu)^2 = 400 \mu^2$$

The capacitance density from $M_1$ to $M_2$ is $0.07 \text{fF/\mu}^2$

$$C_{12} = A_{C1C2} \cdot C_{D12} = 400 \mu^2 \cdot 0.07 \text{fF/\mu}^2 = 28 \text{fF}$$
• Diffusion is used to force migration of impurity atoms into substrate
  – Time and temperature dependent
  – Type of grading can be controlled
  – Subject to subsequent movement when other warm processing steps are done

• Epitaxy
  – Single crystalline extension of substrate
  – Grows slowly to maintain crystalline structure

• Polysilicon

• Used for gates of transistors
  – Comprised of many small crystals
  – Makes good conductor if heavily doped
  – Makes good resistor if moderately doped

Review from Last Time
Basic Devices

- **Standard CMOS Process**
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
- Diodes
- BJT (in some processes)
  - npn
  - pnp

- **Niche Devices**
  - Photodetectors
  - MESFET
  - Schottky Diode *(not Shockley)*
  - MEM Devices
  - ....

Primary Consideration in This Course

Limited Consideration in This Course
Generic Process Flow

**Front End**
- Wafer Fabrication
- Mask Fabrication
- Epitaxy
- Grow or Apply
- Photoresist
- Deposit or Implant
- Etch
- Strip
- Planarization
- Wafer Probe
- Wafer Dicing
- Die Attach
- Wire Attach (bonding)
- Package
- Test
- Ship

**Back End**
Front-End Process Flow

- Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary
Wafer Dicing

Gang of slitting blades

Rotary stage indexer

Silicon wafer

X axis

Y axis

www.renishaw.com
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy
Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding
Wire Bonding

Wire – gold or aluminum
25 μ in diameter
Wire Bonding

Excellent Animation showing process at:

http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf
Wire Bonding

Ball Bond

Wedge Bond

www.kns.com
Ball Bonding Steps
Ball Bonding Tip

Approx 25µ
Wire Bonding

Ball Bond

Termination Bond

Ball Bond Photograph
Bump Bonding
Packaging

1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models
Packaging

IC package

Insertion type
- Standard DIP
  - SIP
  - PGA

Surface mounting type
- SOP
- TSOP
- QFP
- SDJ
- QFJ
- QFN
- TCP
- BGA

www.necel.com
Packaging