

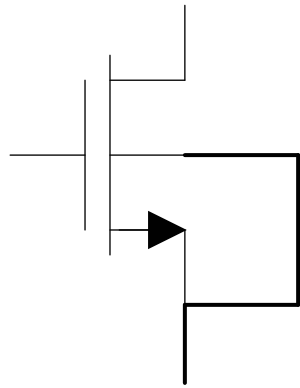
# EE 434

## Lecture 15

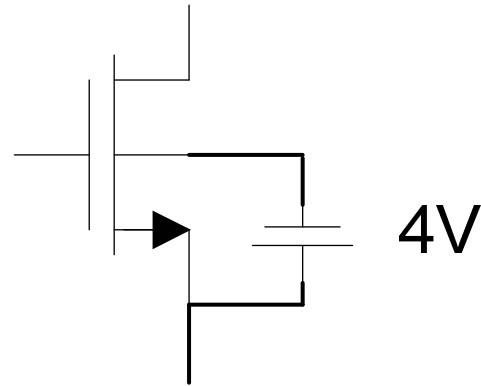
Modeling – the big picture

## Quiz 12

An n-channel MOS transistor has a nominal threshold voltage of 1V with no bulk bias. What will that threshold voltage change to if the bulk bias is -4V? State typical values for any process parameters that you need to solve this problem and use them.



$$V_T = 1V$$



$$V_T = ?$$

And the number is ....

1            8            7            5            3  
6            9            4            2

**1**

## Quiz 12

An n-channel MOS transistor has a nominal threshold voltage of 1V with no bulk bias. What will that threshold voltage change to if the bulk bias is -4V? State typical values for any process parameters that you need to solve this problem and use them.

### Solution

$$V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

$$\gamma = 0.5 \text{V}^{\frac{1}{2}} \quad \phi = 0.6 \text{V}$$

$$V_T = 1 \text{V} + 0.5 \left( \sqrt{0.6 - -4} - \sqrt{0.6} \right) = 1.69 \text{V}$$

Note: Threshold shift with bulk bias can be significant !!

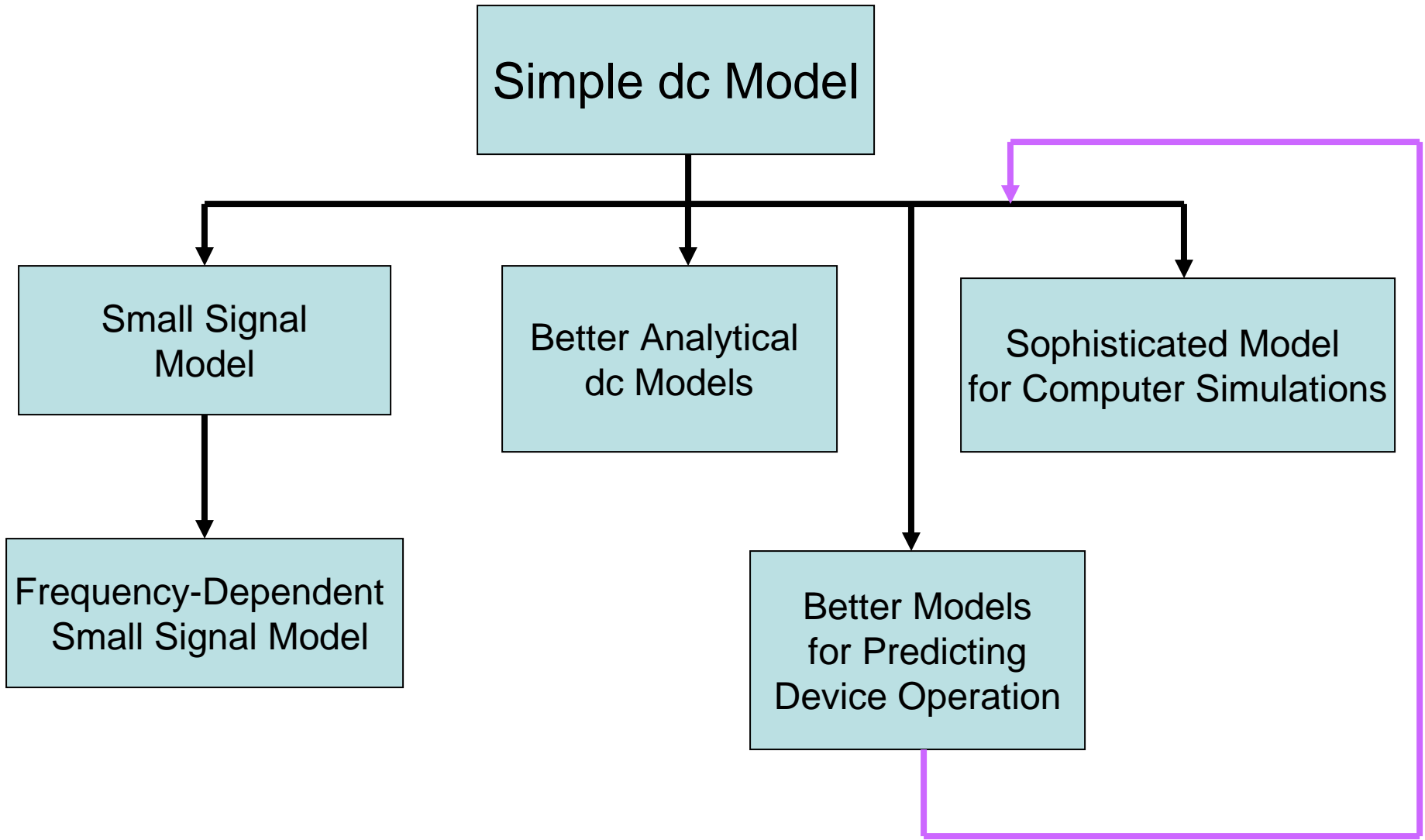
## Review from Last Time

- Reasonably good MOSFET model characterized by 6 process parameters and 2 design parameters

$$\{V_{T0}, C_{OX}, \mu, \gamma, \phi, \lambda\} \quad \{W, L\}$$

- Only a single degree of freedom (W/L)
- Small signal model can be very easily developed from large signal model
- Small signal model developed in saturation region
- Small signal model can be readily derived from the dc model
- Small signal model parameters strongly operating point dependent

# Modeling Summary



How complete or mature are the models for  
the MOS Transistor?

How good are the existing MOS device  
models?

How good are the existing MOS device models?

**Pretty Good** (sometimes)

**Good Enough** (sometimes)

**Lousy** (sometimes)



# How complete or mature are the models for the MOS Transistor?

Many researchers continuing to work on modeling of MOS transistors

Efforts seem to be increasing in recent years

Driven, in part, by changes in performance experienced by deep sub-micron devices