EE 434
Lecture 23

Logic Design

This lecture will focus on the various hierarchical levels used in the design of digital systems. Comments will be made about Hardware Description Languages (HDL) which is an integral part of essentially all digital system design. There are two widely used hardware description languages. One is VHDL and the other is Verilog. In this lecture comments will be made about VHDL. In the balance of this course we will focus on Verilog. There is still debate about which is most popular and that continues in this department. We will focus on Verilog in the balance of this course because we believe most ISU students have more familiarity with Verilog than with VHDL. Both will be used in industry and designers will usually be expected to be comfortable working in both.

Design Domains:

Behavioral:

Structural:

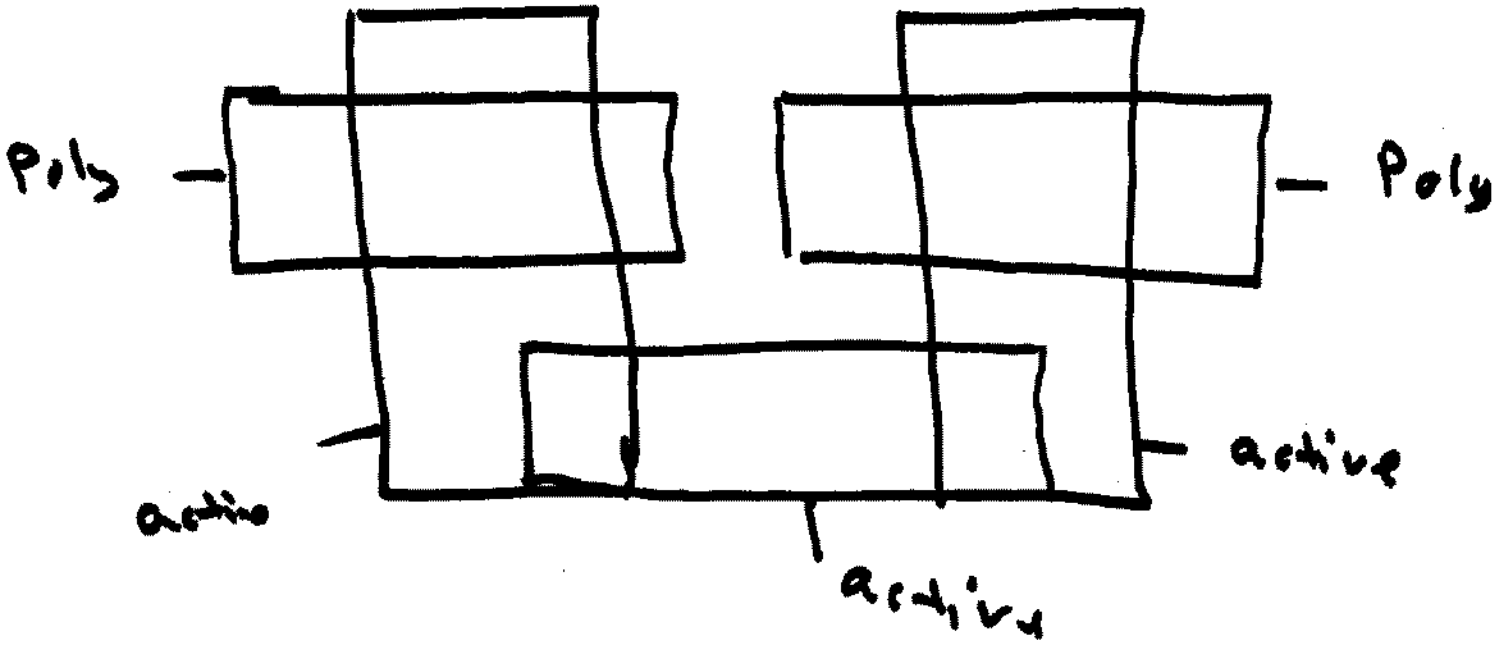
Physical

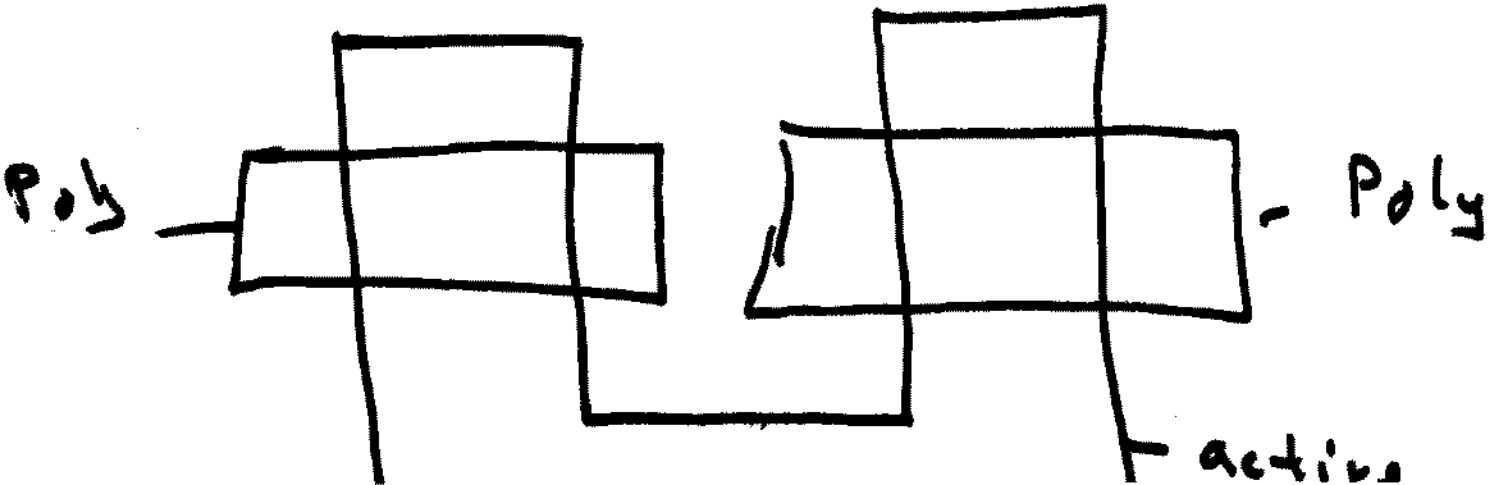
Behavioral: Describes what a system does or what it should do

Structural: Identifies constituent blocks and describes how these blocks are interconnected and how they intract

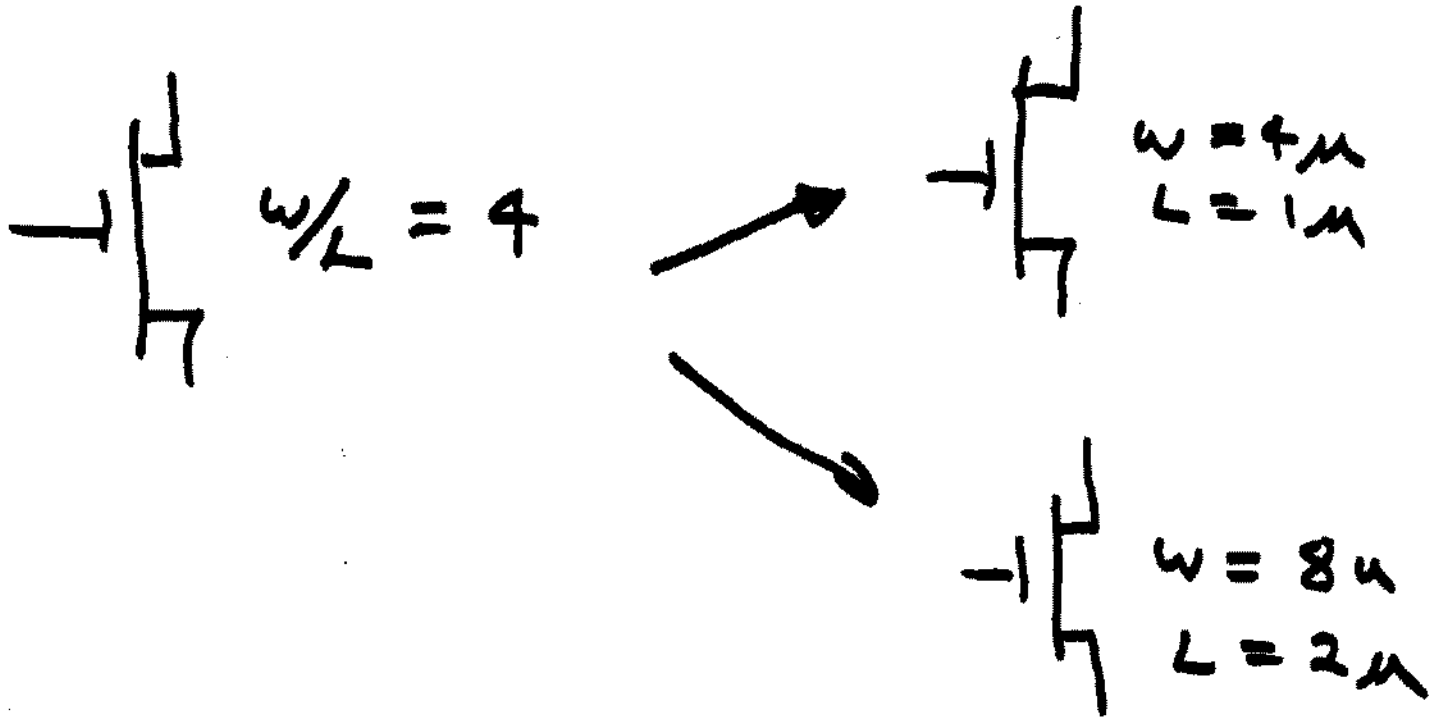
Physical: Describes the constituent blocks to both the transistor and polygon

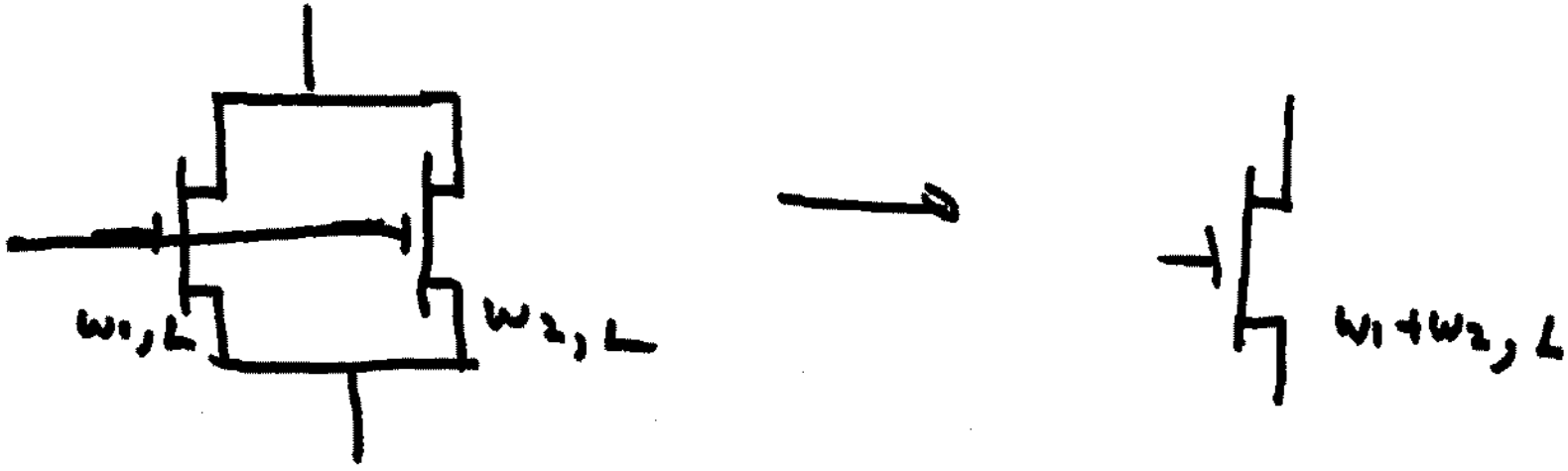
Ex:





Example

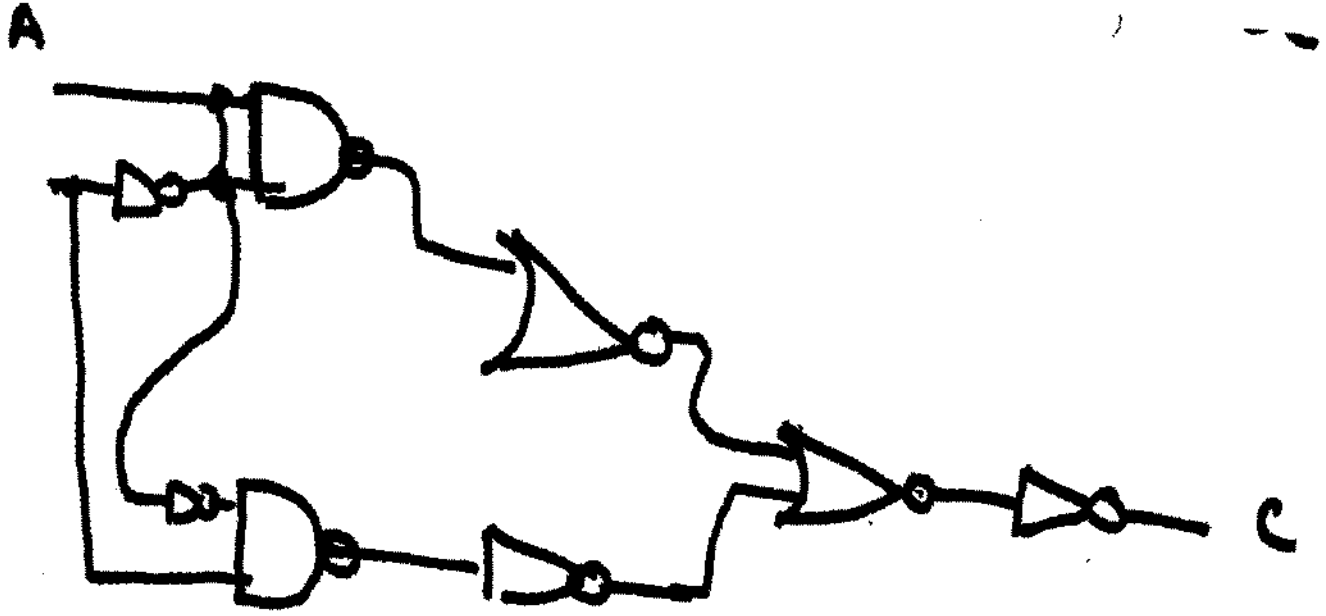


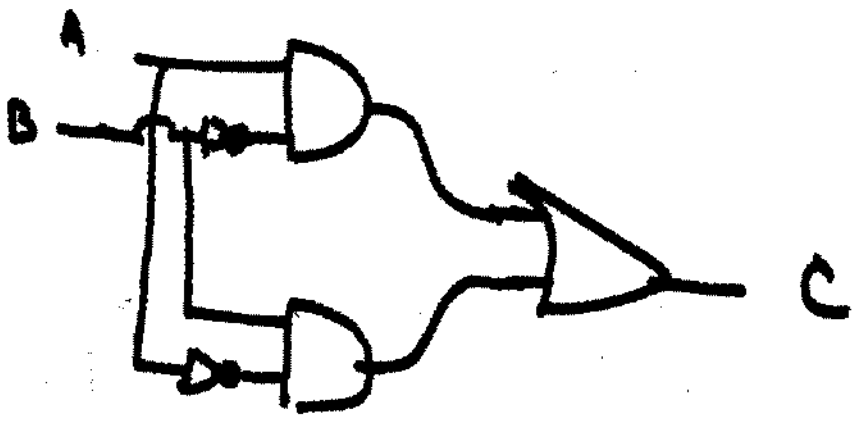


Example:

$C = A \oplus B$

$= A\bar{B} + B\bar{A}$





In each domain, multiple levels of abstraction are generally used.

Consider Physical Domain

Database:
G.D.F
Netlist

- consider lowest level to highest
  - 0 - placement of diffusions, thin oxide regions, field oxide, etc. on a substrate.
  - 1 - polygons identify all mask information (not unique)
  - 2. - transistors (not unique)
  - 3. - gate level (not unique)

Structural Level

- HDL
- Netlists

- DSP
- Blocks (Adders, Memory, Registers, etc.)
- Gates
- Transistor

Behavioral Level (top down)

- Application
- Programs
- Subroutines
- Boolean Expressions

High-Level Language
HDL

Example!

Behavioral Level: System which will give a command to dial an emergency number if a temperature indicator identifies a problem and a humidity indicator indicates no problem or if the temperature indicator indicates no problem but the humidity indicator indicates a problem

hum: humidity
tem: temp
call: time to dial emergency number.

VHDL code.

```
entity alarm is
port (hum, tem : in bit ;
      call : out bit) ;
end alarm
```

entity declaration

```
architecture acontroller of alarm is
begin
    call <= (hum XOR tem)
end acontroller
```

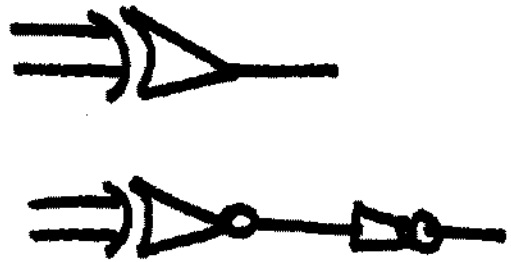
architecture construct

Structural Level

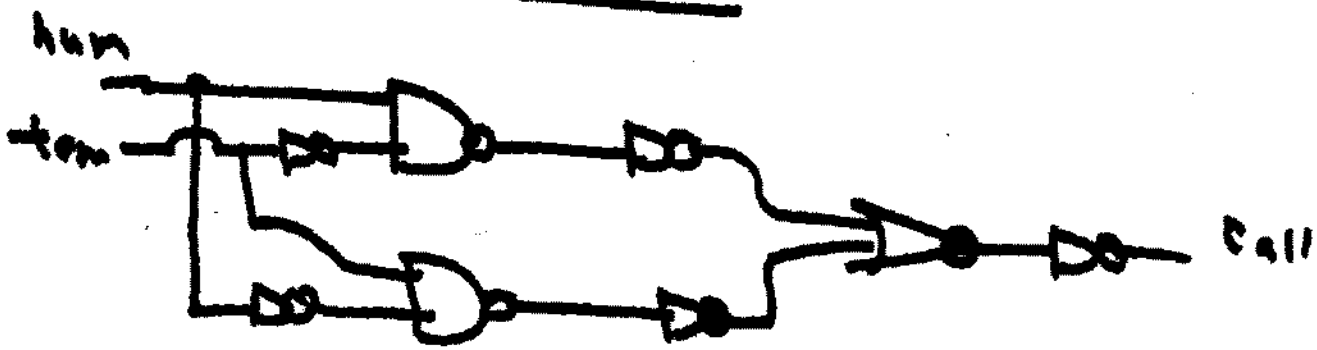
Call = hum ⊕ tem

XOR #1

g1(call, hum, tem)



Physical Level



Static CMOS gates

Representation of Digital Systems

Standard Approach to Digital Circuit Design

1. Behavioral Description — HDL
   - technology independent
2. RTL Description — HDL
   (must verify (1) & (2))
3. RTL Compiler
   Registers & Combinational Logic Functions
4. Logic Optimizer
5. Logic Synthesis
   generally use a standard cell library for synthesis

6. Place & Route
   (physically locates all gates & registers and interconnects them)

7. Layout Extraction

   DRC
   Back Annotation

8. Post layout simulation

   may necessitate a return to ~~the~~ a higher level in the design flow