EE 434

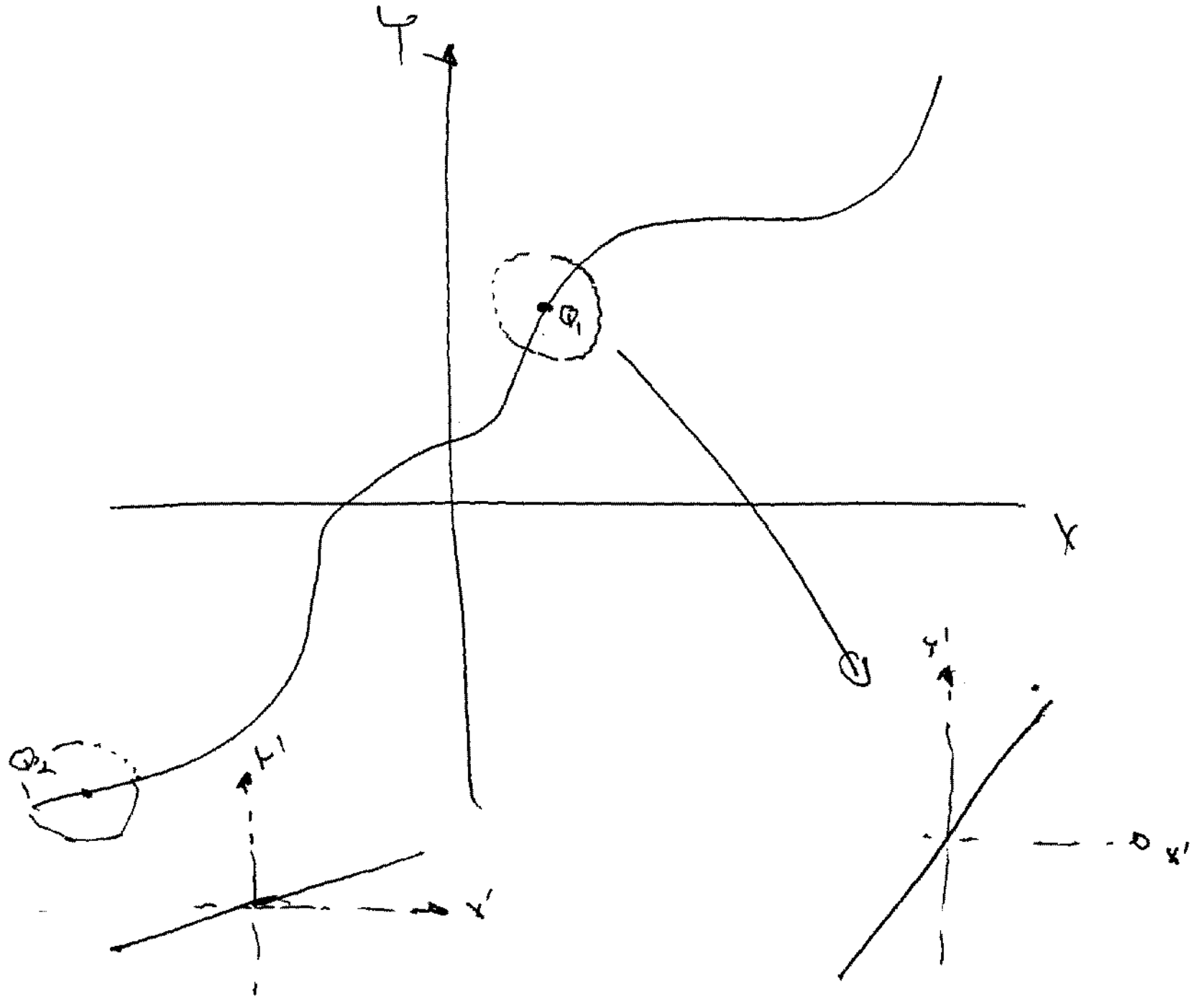## Lecture 26

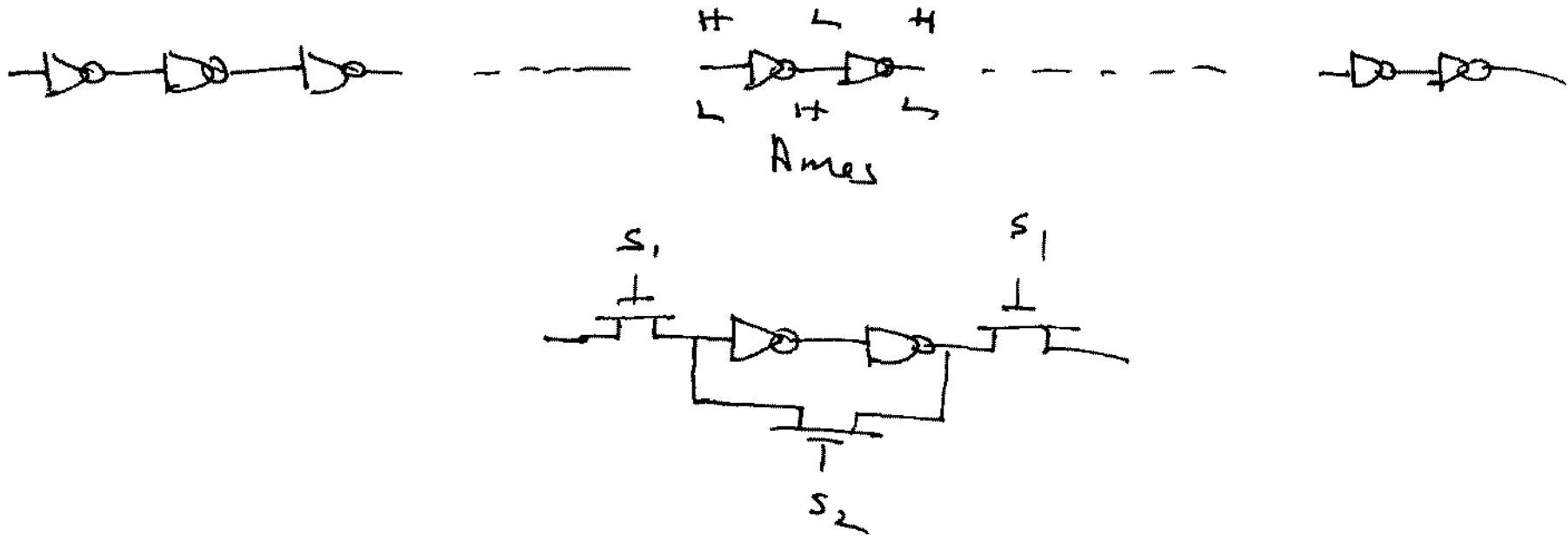Determination of Boolean
Logic Levels

From discussion about Q-point and small signal model:
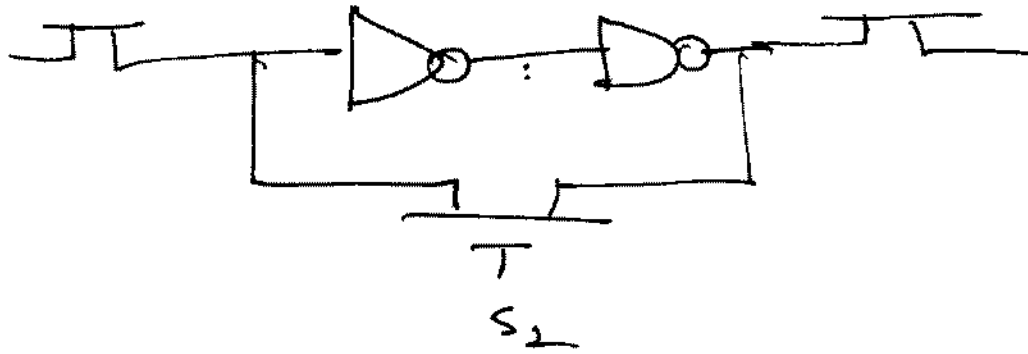
Observation (Claim)

Characteristics of a logic family are determined by characteristics of the inverter in that logic family
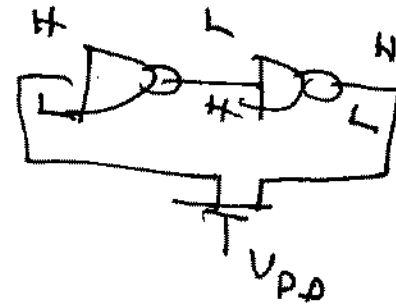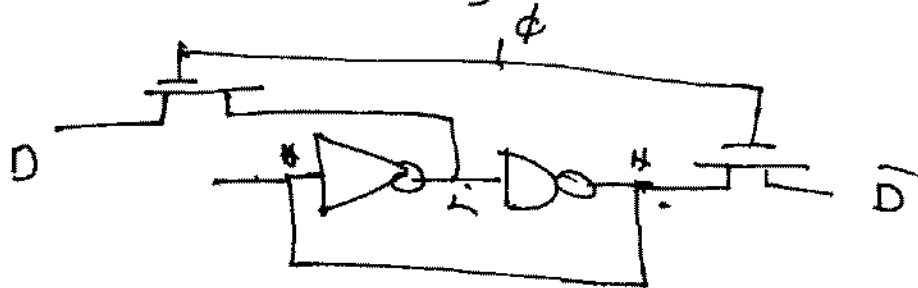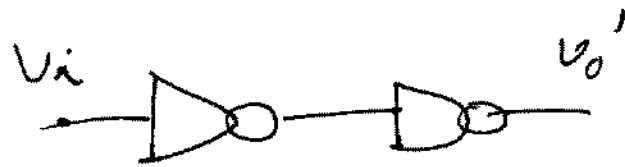
Consider Inverter Chain

what is this circuit?

S_2

1) Buffer

2) Buffer, Memory, Latch...
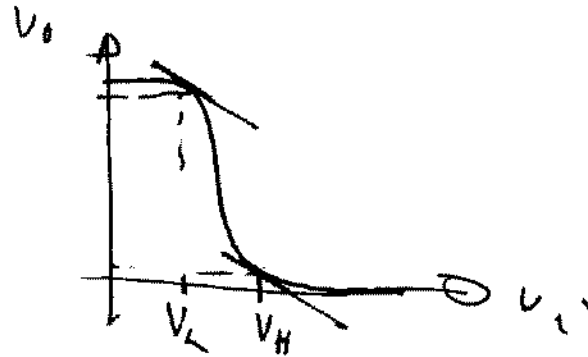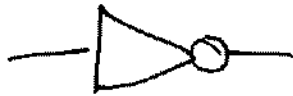

ϕ

D

$\bar{D}$

V_{DD}

consider inverter pair

What are V_H & V_L for this logic family
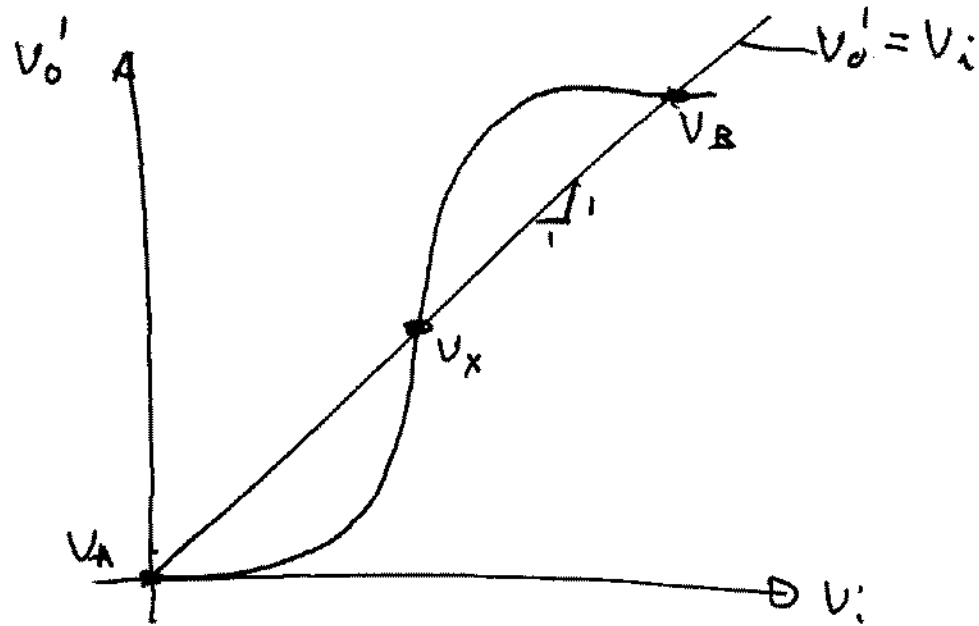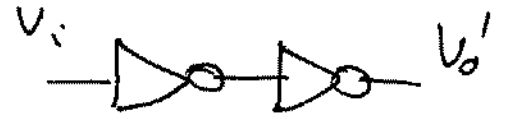
V_i ▷o▷o V_o'

Some authors do the following

▷o

This "legislates" the definition of V_H and V_L but may not tell how the circuit really defines or recognizes high and low logic levels

Consider Inverter Pair Transfer Characteristics V_i

— At $V_i = V_H$, $V_o' = V_H$ and at $V_i = V_L$, $V_o' = V_L$

— $\therefore$ V_H and V_L must lie on the intersection of the $V_o' = V_i$ line with the inverter pair transfer characteristics

— But which of the three points V_A, V_X, V_B correspond to V_H and V_L?

What if V_x were present on the input to both inverter?
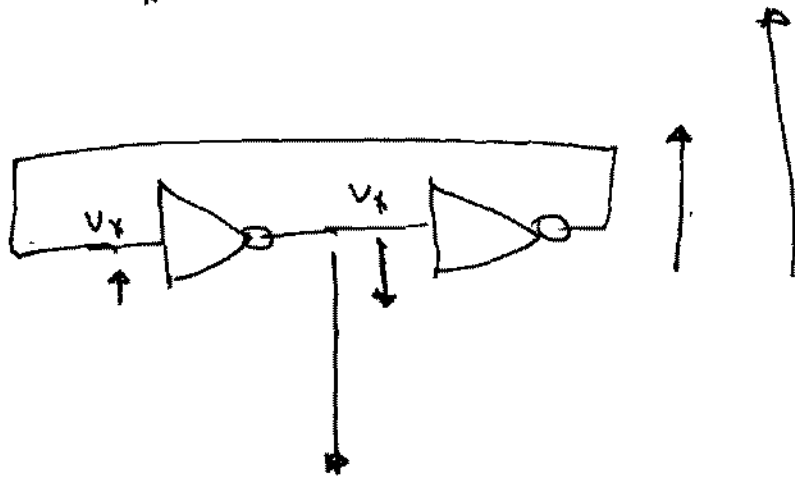
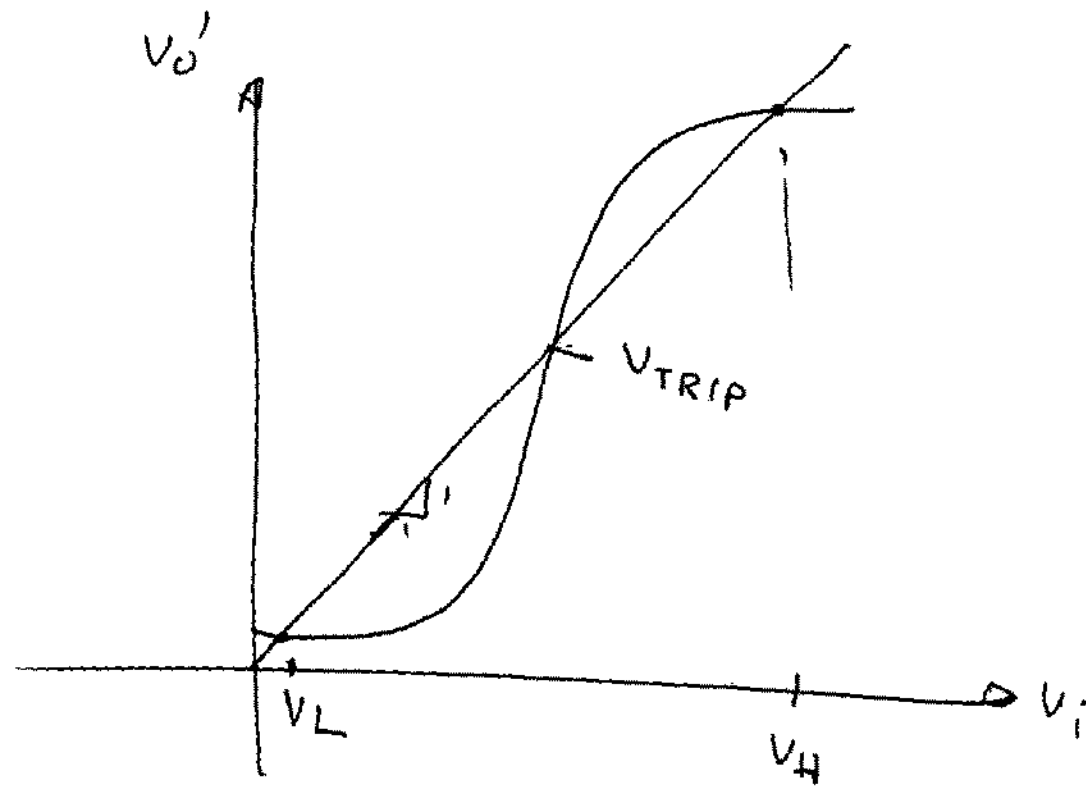- If a small positive deviation were to occur on the input to the first inverter, a larger negative variation would be forced on the output which would, in turn, increase the input even more!

- The point V_x is a quasi-stable point and is neither V_H or V_L !

- Thus $V_L = V_A$ and $V_H = V_B$

The quasi-stable point is termed V_{TRIP}

Key Criteria for Boolean Functionality

Transfer chan. must have three intersection points with the $V_o' = V_i$ line

- upper is V_H
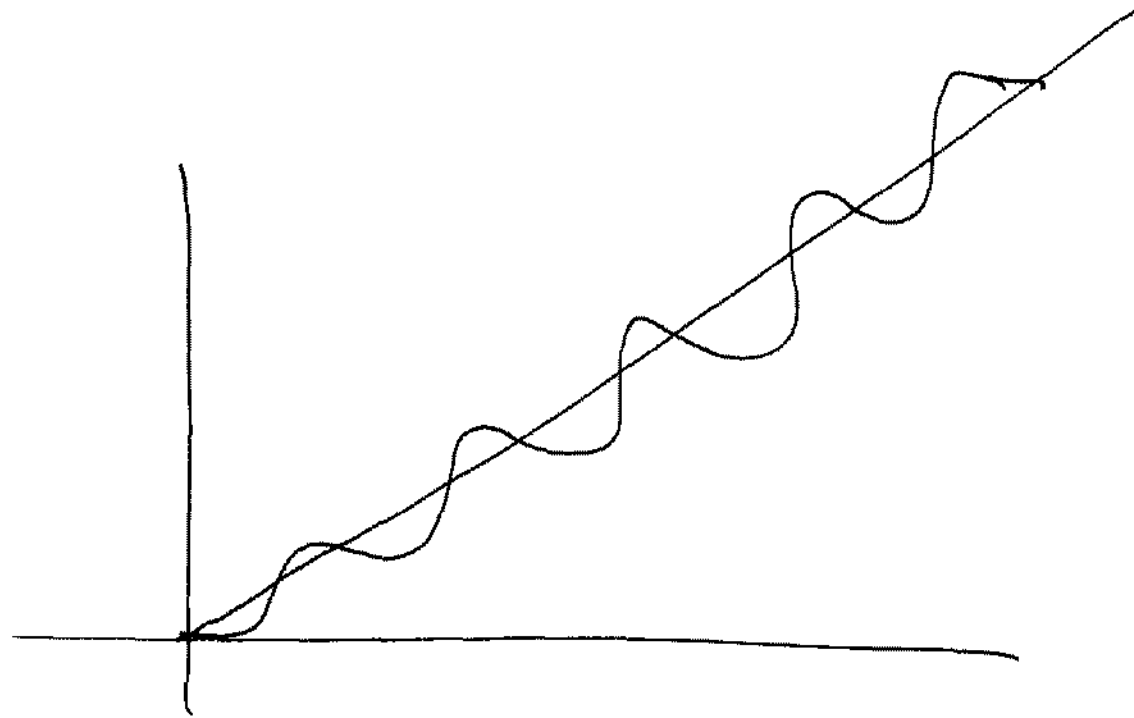- Lower is V_L
- middle is V_{TRIP} (quasi-stable)

• Desirable Properties

> Reasonable Separation between V_H & V_L

  (enough separation so that noise does not cause circuit to interpret level correctly)

> $V_{TRIP} \simeq \dfrac{V_H + V_L}{2}$ (to provide adequate noise margins)

what if

Device can store multiple bits of information!

If any device or simple circuit had these properties, (more than 3 intersections) ∧ there would be considerable interest in it!