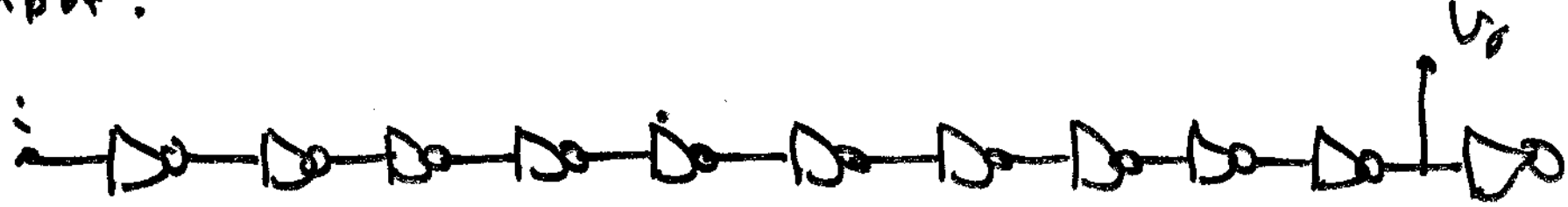
EE 434

Lecture 28

Propagation Delay in Digital Circuits - Continued

Question: If an inverter drives a cascade of 10 inverters, what delay will be experienced as the signal propagates from the input to the output?

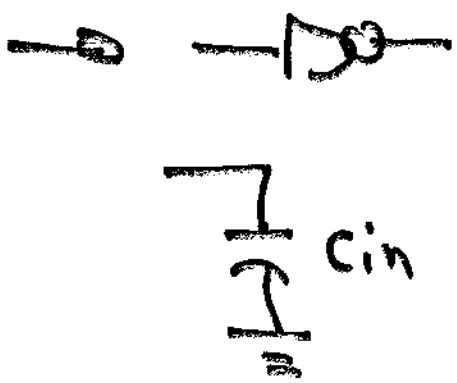


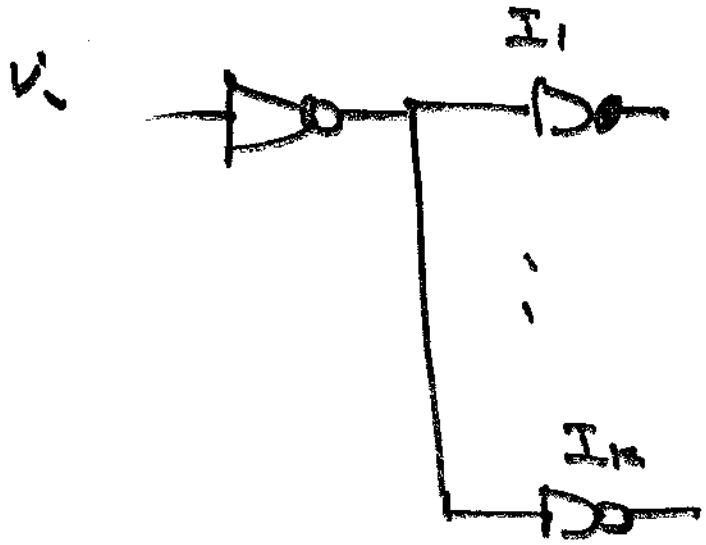
Assume that a transition on a subsequent stage doesn't start until transition is complete on previous stage and subsequent stage transition times are the same as the transition times on the first stage.

$$t_{HL\,OA} = 5t_{LH} + 5t_{HL}$$

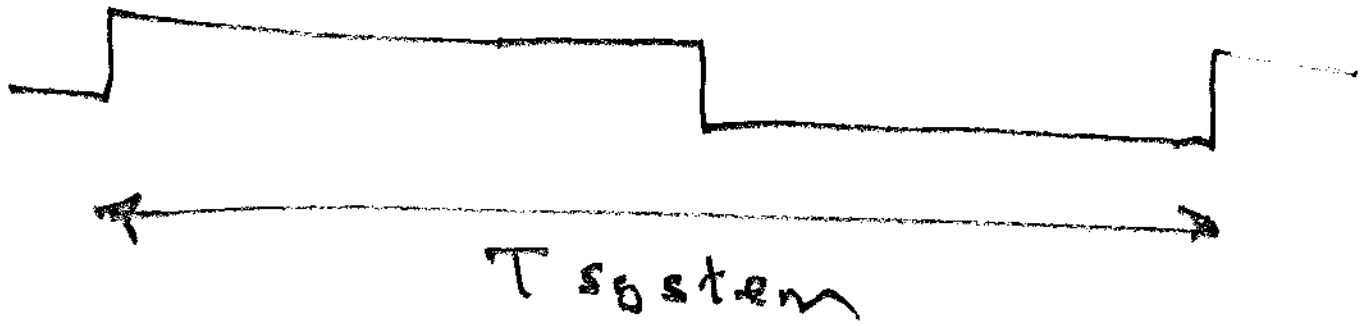
$$t = \sum_{i=1}^{10} t_i$$

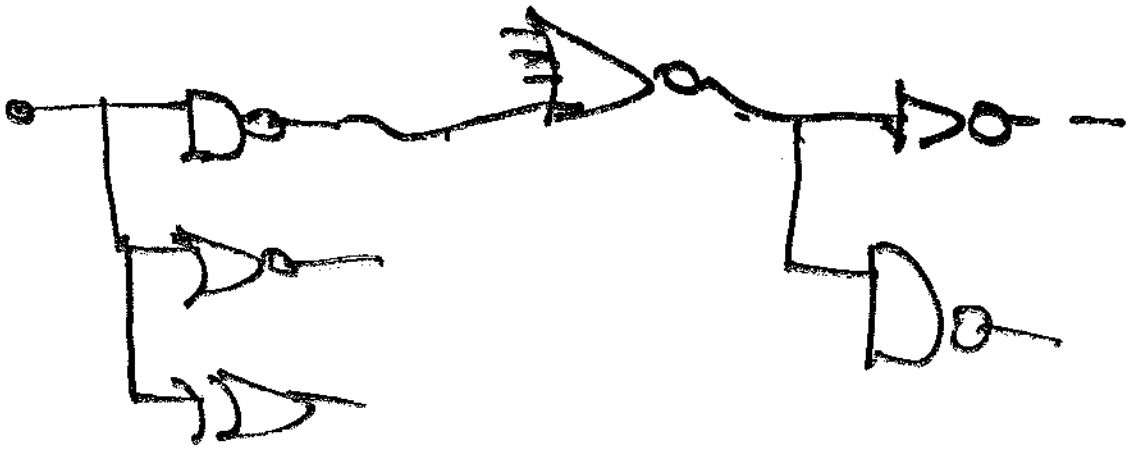

Vo
Vi

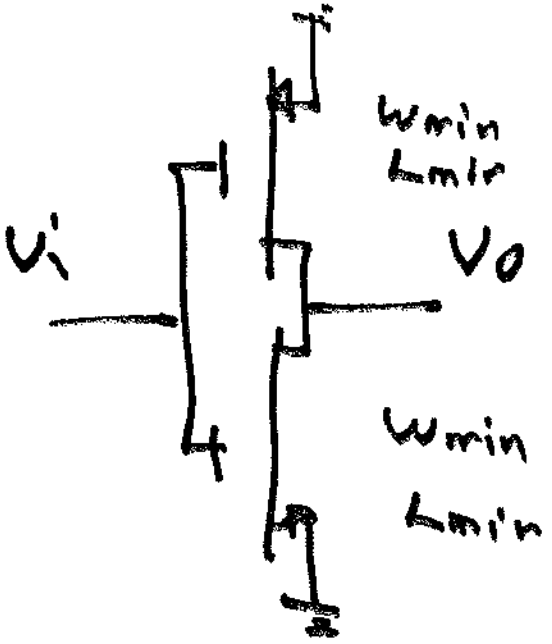

Cin


I1
Vi
Ik


K Cin


T system





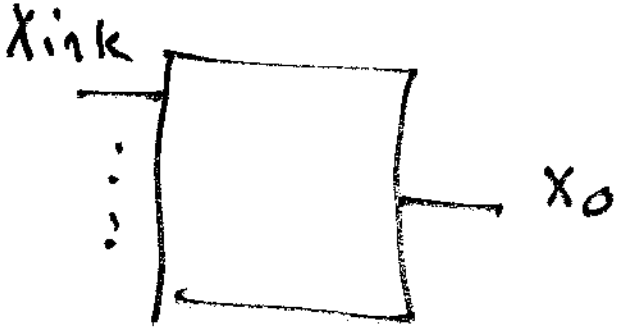
- Establish a <u>reference</u> inverter.

- give propagation data (info) in terms of how an actual gate's propagation relates to that of the reference inverter.

Assume a reference inverter exists. $C_{in} = C_{REF}$

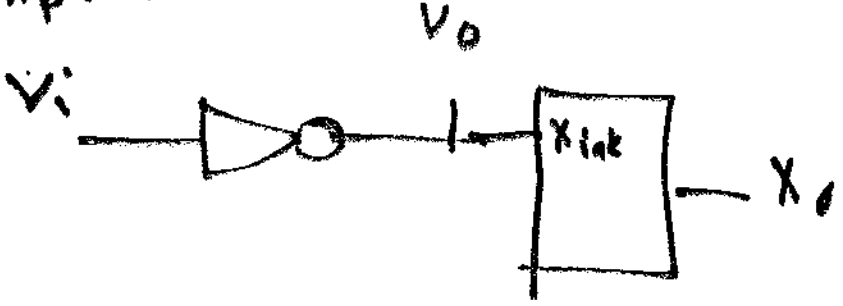
$t = t_{REF}$

Consider any gate

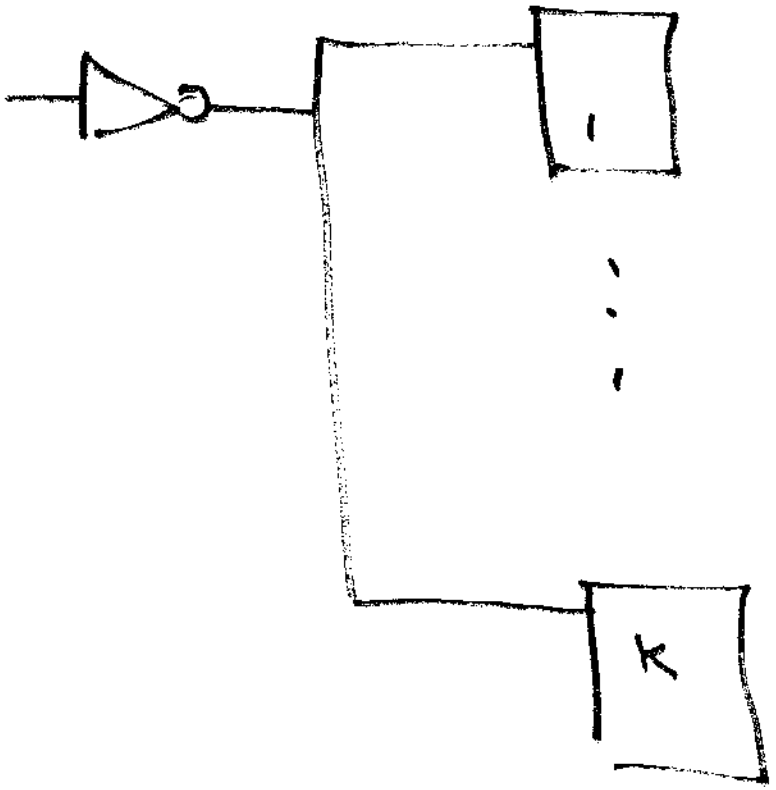


$$\text{Fan In} = \frac{C_{ink}}{C_{REF}}$$

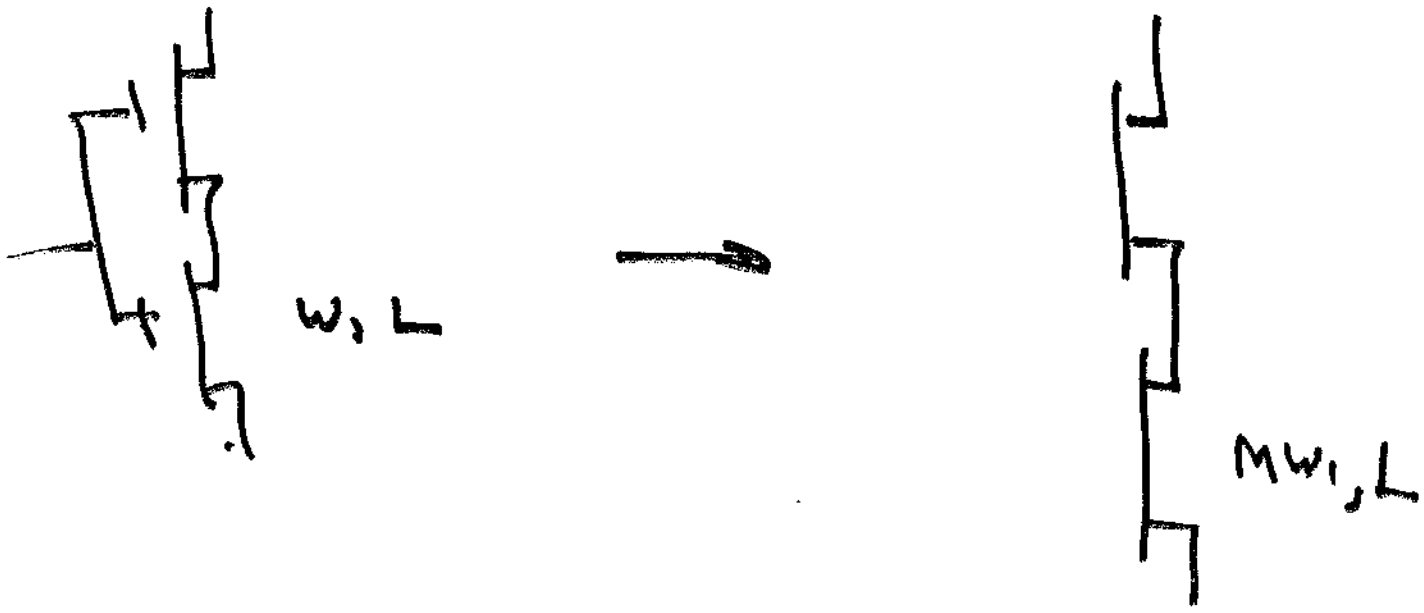
Example:



$t = t_{REF} \cdot \text{Fan In}$



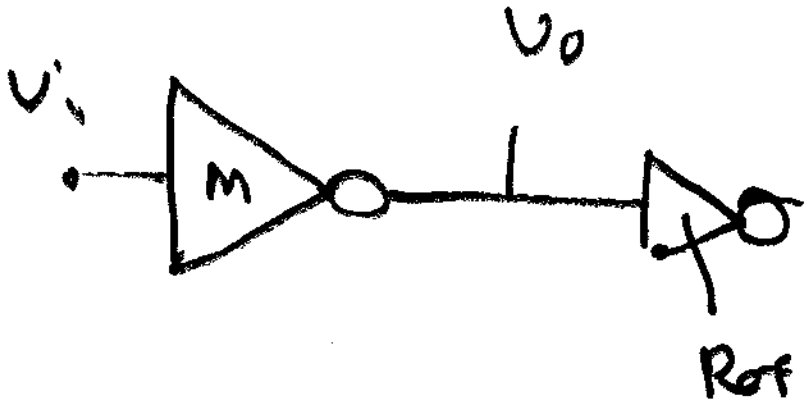
$$t = t_{REF}\left(\sum_{i=1}^{k} FI_i\right)$$



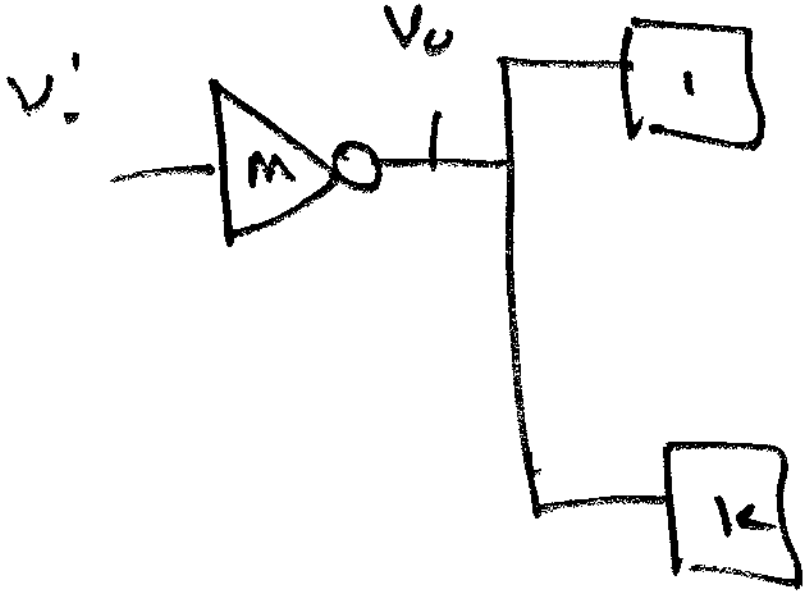
F.O. = M

If $M > 1$, then the device has a stronger drive capability than the ref. device

If $M < 1$, then the device has a weaker drive capability than the ref. device.



$$t = \frac{t_{REF}}{M}$$



$$t = \frac{t_{REF} \cdot \sum_{i=1}^{K} F_{i,i}}{M}$$

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Lecture 22

~~Timing~~

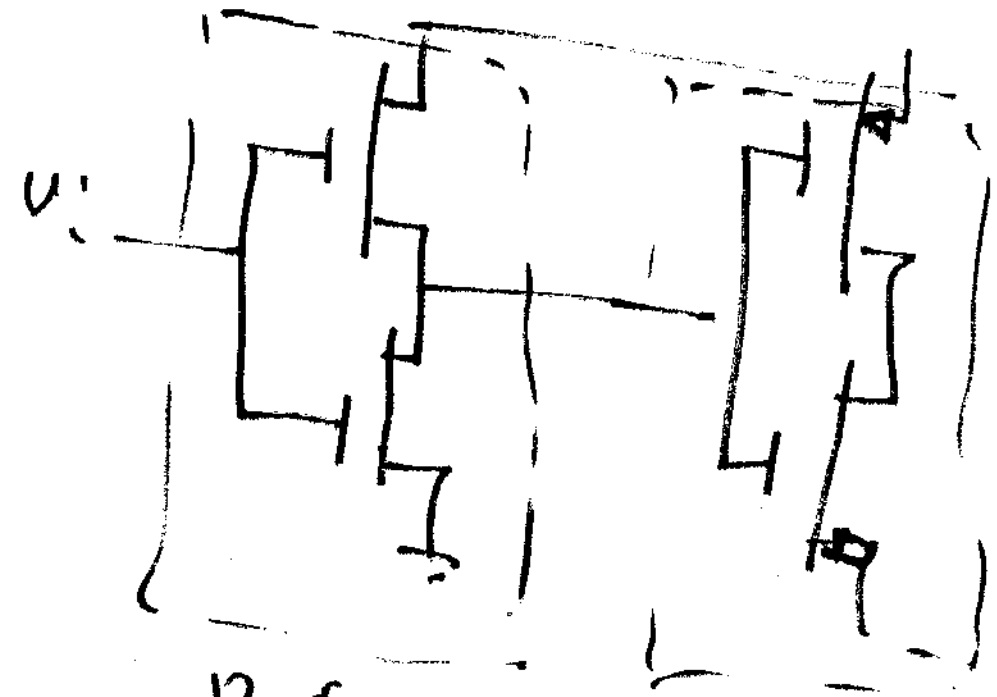
Delay Calculations

Multiple-Input Gates

Device Sizing

Recall

$$t = (Mult)\, t_{REF}$$



$$t_{REF} = C_{REF}(R_{pu} + R_{pd})$$