EE 434

Lecture 29

Multiple Input Gates

Device Sizing Strategies

Quiz: A minimum sized CMOS Inverter designed in a 0.5μ CMOS process is driving 5 identical devices. Obtain t_{HL}.

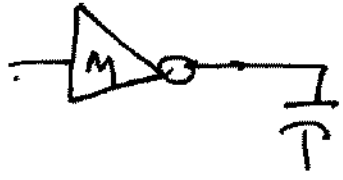
Solution: $t_{HL} = (5)(3psec) = 15psec.$

Review from Last Time

1) Select a Ref inverter to characterize the prop. delays in a process

2) Determine t_{HL}, t_{LH} for ref. inverter driving an identical device.

3)



$C_{eL} = F C_{REF}$

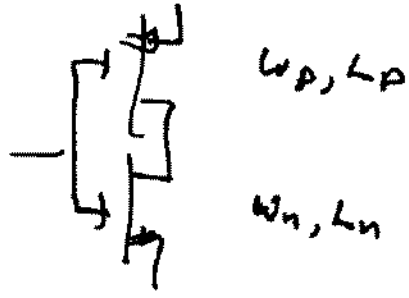
$t = (t_{REF}) \frac{F}{M}$

$W_n' = M W_n$

$W_p' = M W_p$

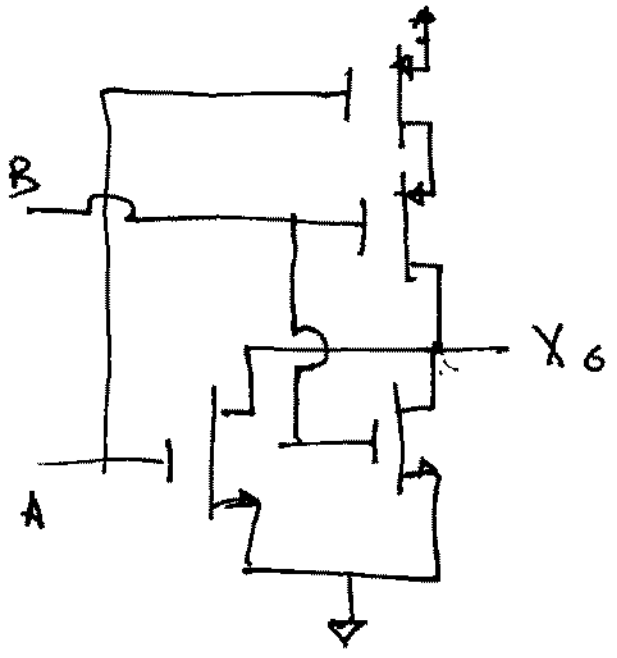
$L_n' = L_n$

$L_p' = L_p$

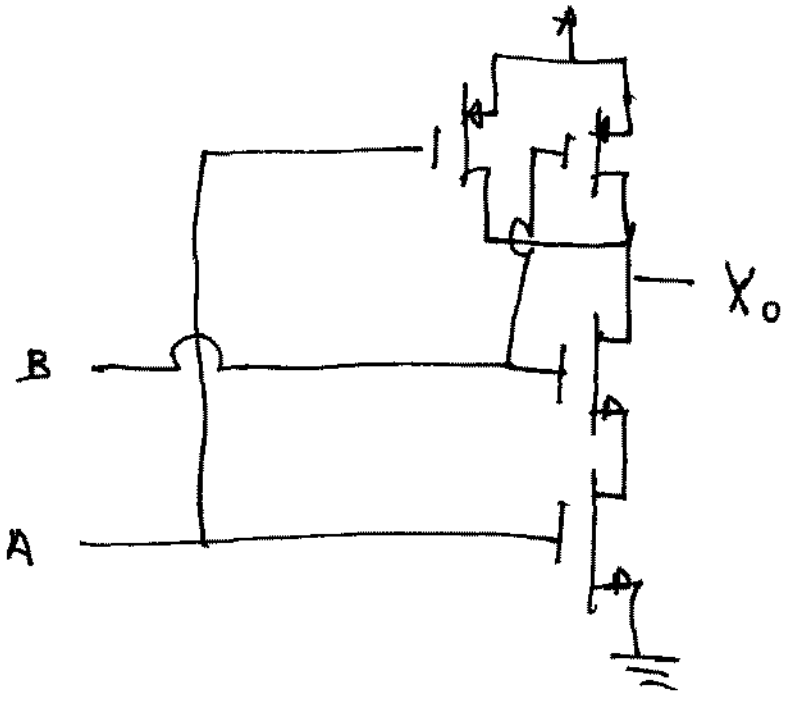


Ref Inv.

Multiple Input Gates



2 Input NOR Gate



2 input NAND Gate

If pd network extended to k transistors in parallel and pullup network extended to k transistors in series becomes k-input NOR Gate.

If pd network extended to k transistors in series ~~pu~~ and pu network extended to k transistors in parallel, becomes k-Input NAND Gate.

Note: Now have all of the tools needed to build any combinational logic function.

Either NOR gates or NAND gates form a complete logic family.

Device Sizing

Strategies:

1) minimum sized devices ☺

(2) minimum rise and fall times)

3) $t_{HL} = t_{LH}$

4) $V_{TRIP} = \frac{V_{DD}}{2}$ (equal noise margins)

5) minimum power dissipation

6) willy-nilly