EE 434
Lecture 29

Multiple Input Gates
Device Sizing Strategies
Quiz: A minimum sized CMOS inverter designed in a 0.5μ CMOS process is driving 5 identical devices. Obtain $t_{HL}$.

Solution: $t_{HL} = (5)(3\,\text{psec}) = 15\,\text{psec}$. 
Review from Last Time

1) Select a Ref inverter to characterize the prop. delays in a process.

2) Determine $\beta_H$, $\beta_L$ for ref. inverter driving an identical device.

3) \[
\frac{1}{T} C_{EL} = F C_{REF}
\]

\[
T = (T_{REF}) \frac{F}{M}
\]

\[
\omega_n = M \omega_n
\]

\[
\omega_p = M \omega_p
\]

\[
L_n = L_n
\]

\[
L_p = L_p
\]
Multiple Input Gates

2 input NOR Gate

If pull network extended to \( k \) transistors in parallel and pullup network extended to \( k \) transistors in series becomes

\[ k \text{-input NOR Gate.} \]

2 input NAND Gate

If pull network extended to \( k \) transistors in series and pullup network extended to \( k \) transistors in parallel becomes

\[ k \text{-input NAND Gate.} \]
Note: Now have all of the tools needed to build any combinational logic function.

Either NOR gates or NAND gates form a complete logic family.
Device Sizing

Strategies:

1) minimum sized devices

2) minimum rise and fall times

3) $t_{HL} = t_{LH}$

4) $V_{TRIP} = \frac{V_{PP}}{2}$ (equal noise margins)

5) minimum power dissipation

6) willy-nilly