EE 434
Lecture 31

Device Sizing of Static CMOS Circuits
Quiz: If a CMOS inverter with 
\( w_n = 2 \mu \), \( w_p = 4 \mu \), \( L_n = L_p = L \) is designed in a process with \( \mu / \sigma x = 10^{-4} \), \( V_{th} = |V_{tp}| = 1V \), \( g = 0 \) and \( \lambda = 0 \), what will the output voltage be when both devices are in saturation? Assume \( V_{dd} = 5V \)
Solution: When $M_1$ and $M_2$ are in saturation, $V_0$ is indeterminate since

$$V_{in} = V_{Th} + (V_{D0} + V_{TP}) \frac{\sqrt{\frac{M_p}{M_n}} \frac{\omega_2}{\omega_1 L_2}}{1 + \sqrt{\frac{M_p}{M_n}} \frac{\omega_2}{\omega_1 L_2}}$$
Review from Last Time:

- Elmore delay model provides quick approximate delay prediction
- Inverter and Inverter Pair Transfer Characteristics both provide \( V_{TRIP} \) from \( X_0 = X_i \) line
- DC transfer characteristics of inverter can be systematically obtained
Observations

Inverters have devices that ideally never operate in sat.

(Ideally one is in CO and other in triode)

\[ v_i \rightarrow D \rightarrow v_o \]

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\[ v_{TRIP} = V_{TN} + (v_{PD} + V_{TP}) \sqrt{\frac{1}{1 + \sqrt{\frac{v_{TP}}{v_{PD}}}}} \]

\[ v_H = v_{PD} \]

\[ v_L = 0 \]
What is $V_{TRIP}$ for the static CMOS Inverter?

In a typical process,

$$V_{TH} = 0.2V_{DD}$$

$$V_{TP} = 0.2V_{DD}$$

$$M_P \approx \frac{1}{3} M_N$$

$$V = \sqrt{\frac{1}{3} \frac{W_2 L_1}{W_1 L_2}}$$

$$V_{TRIP} = 0.2V_{DD} + (V_{BB} - 0.2V_{DD}) \sqrt{\frac{1}{1 + V}}$$

$$= V_{BB} \left( \frac{0.2 + 0.8 \sqrt{\frac{1}{1 + V}}}{1 + V} \right)$$
$U_{\text{trip}}$ for minimum sized devices:

If $w_1 = w_2 = h_1 = h_2 = l_{\text{min}}$

$$U_{\text{trip}} = V_{\text{DD}} \left( \frac{0.2 + 0.8 \sqrt{3}}{1 + \sqrt{3}} \right) = 0.42V_{\text{DD}}$$

$U_{\text{trip}}$ for $w_2/w_1 = \frac{V_{\text{DD}}}{V_{\text{TH}}}$

If $w_1 = \frac{h_2}{h_1} = h_1 = h_2 = l_{\text{min}}$

$w_2 = 3w_1$,

$$U_{\text{trip}} = V_{\text{DD}} \left( \frac{0.2 + 0.8}{1 + 1} \right) = \frac{V_{\text{DD}}}{2}$$

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Device sizing substantially affects $U_{\text{trip}}$
Device Sizing Strategies

1) Minimum Sized Devices

\[ V_H = V_{DD}, \; V_L = 0 \]

\[ V_{TRIP} \approx 0.4 V_{DD} \]

2) \[ V_{TRIP} = \frac{V_{DD}}{2} \]

From previous example, observe that

\[ \frac{M_p}{M_n} \frac{L_2}{L_1} = 1 \]

Thus

\[ M_p = M_n \]

\[ L_1 = L_2 = L_{min} \]

\[ W_1 = W_{min} \]

\[ W_2 = 3 W_{min} \]

3) Equal \( C_{TH} \) and \( C_{TT} \)

- slow in the timing

- pull up time is slow when minimum sized devices are used
For equal rise and fall:

\[ R_{PD} = R_{PU} \]

\[ \frac{L_1}{L_2} = \frac{\frac{1}{\mu N_0 C_{ox} W_1 (V_{DD} - V_{TN})}}{\mu P_0 C_{ox} W_2 (V_{DD} + V_{TP})} \]

\[ L_1 + L_2 = C_{RBE} R_{PD} \]

\[ t_{LU} = C_{REF} R_{PU} \]

\[ \frac{L_1}{L_2} \cdot \frac{W_2}{W_1} = \frac{\mu N_0}{\mu P_0} \left( \frac{V_{DD} - V_{TN}}{V_{DD} + V_{TP}} \right) \]

\[ W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right) \left( \frac{V_{DD} - V_{TN}}{V_{DD} + V_{TP}} \right) \]

If \( V_{TN} = 0.2V_{DD}, V_{TP} = -0.2V_{DD} \)

\[ W_2 = \left( \frac{\mu_n}{\mu_p} \right) W_1 \]

Note: with these threshold choices, \( V_{TRIP}/2 \) sizing is identical to equal rise/fall criteria. 😊
How does the total delay for the minimum sized inverter compare to that of the equal rise/fall time inverter?

Case I. minimum sized

Define $C^*$ to be the input capacitance to this inverter.

$$ C^* = 2 C_{ox} W_{min} L_{min} $$

$$ R_{pd}^* = \frac{L_{min}}{m_{ox} C_{ox} W_{min} (V_{DD} - V_{Tn})} $$

$$ \therefore \quad t_{HL} + t_{ LH} = R_{pd}^* C^* + R_{pu}^* C^* = R_{pd}^* C^* + 3 R_{pd}^* C^* = 4 R_{pd}^* C^* $$
Case 2. Equal Rise & Fall Time:

\[ w = 3 \omega \text{min} \]
\[ \omega \text{min} \]

\[ C_{REF} = \cos \theta \sin \theta \mu \text{rad} + \cos \theta 3 \omega \text{min} \mu \text{rad} \]

\[ = 4 \cos \omega \omega \text{min} \mu \text{rad} \]

\[ C_{HL} = R_{PD} C_{REF} \]

\[ 6 H + 6 L = 2 R_{PD} C_{REF} \]

\[ = 2 R_{PD} + 4 \cos \omega \omega \text{min} \mu \text{rad} \]

\[ = 4 R_{PD} C_{REF} \]

\[ \therefore \text{speed is identical} \]

There is no speed improvement with the equal rise/fall time sizing but the total switched capacitance has doubled and the area is modestly larger.