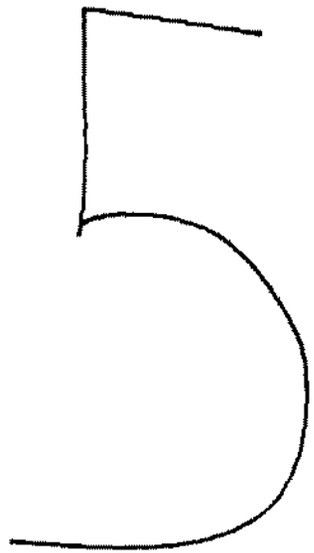
EE 434
Lecture 31

Device Sizing of Static CMOS Circuits

Quiz: If a CMOS inverter with $W_n = 2\mu$, $W_p = 4\mu$, $L_n = L_p = 1\mu$ is designed in a process with $\mu C_{ox} = 10^{-4}$, $V_{TN} = |V_{Tp}| = 1V$, $\gamma = 0$ and $\lambda = 0$, what will the output voltage be when both devices are in saturation? Assume $V_{DD} = 5V$



Solution: When M_1 & M_2 are in saturation, V_O is indeterminate since

$$V_{in} = \frac{V_{TN} + (V_{DD} + V_{TP})\sqrt{\frac{\mu_p}{\mu_n}\frac{W_2 L_1}{W_1 L_2}}}{1 + \sqrt{\frac{\mu_p}{\mu_n}\frac{W_2 L_1}{W_1 L_2}}}$$

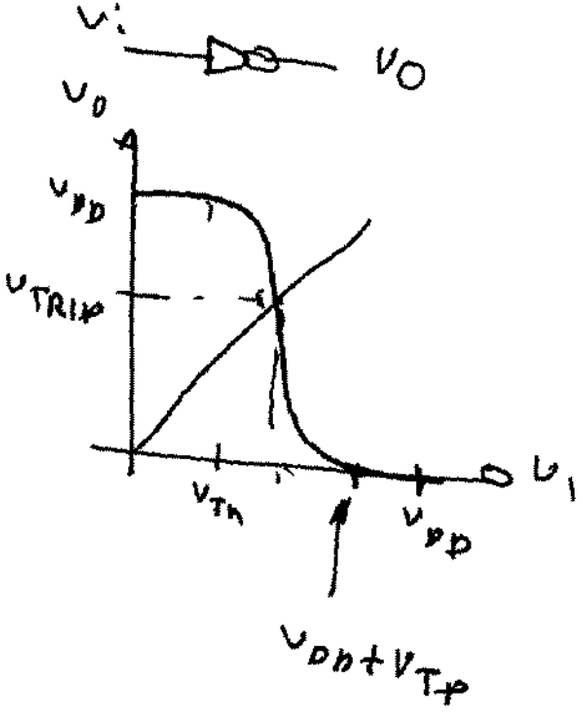
Review from Last Time:

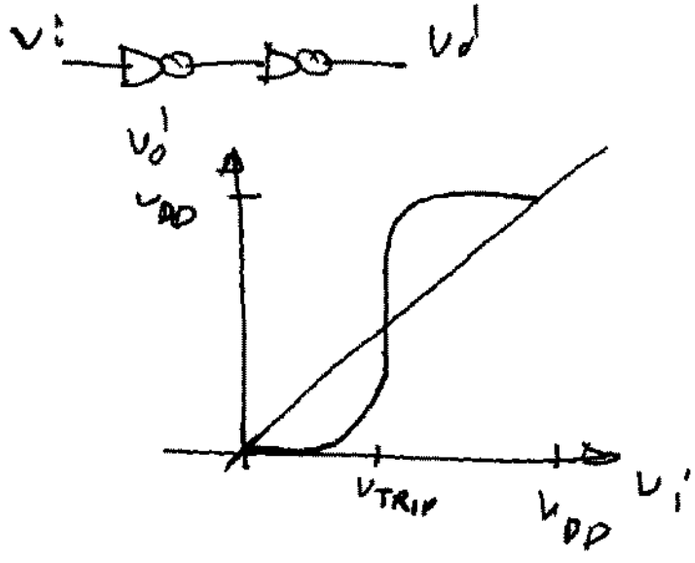
- Elmore delay model provides quick approximate delay prediction
- Inverter and Inverter Pair Transfer Characteristics both provide V_{TRIP} from $X_0 = X_i$ line
- DC transfer characteristics of inverter can be systematically obtained

Observations

— Inverters have devices that ideally never operate in sat.

(Ideally one is in co and other in triode)





$v_H = v_{DD}$

$v_L = 0$

$$\sqrt{} = \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}$$

$$v_{TRIP} = \frac{v_{Tn} + (v_{DD} + v_{Tp})\sqrt{}}{1+\sqrt{}}$$

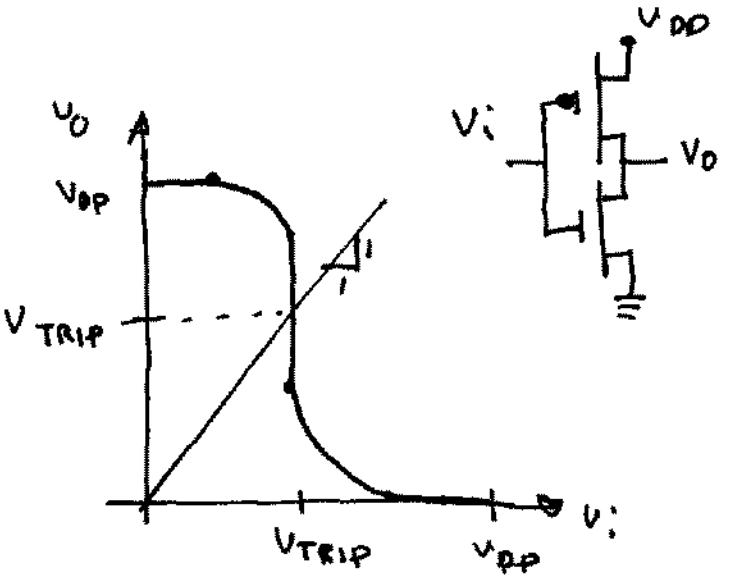
What is V_{TRIP} for the static CMOS Inverter?

In a typical process

$$V_{Tn} \simeq .2V_{DD}$$

$$|V_{Tp}| \simeq .2V_{DD}$$

$$\mu_p \simeq 3^{-1}\mu_n$$



$$\sqrt{\quad} = \sqrt{\frac{1}{3}\frac{W_2 L_1}{W_1 L_2}}$$

$$V_{TRIP} = \frac{.2V_{DD} + (V_{DD} - .2V_{DD})\sqrt{\quad}}{1+\sqrt{\quad}}$$

$$= V_{DD}\left(\frac{.2 + .8\sqrt{\quad}}{1+\sqrt{\quad}}\right)$$

* V_{TRIP} for minimum sized devices:

If $W_1 = W_2 = L_1 = L_2 = L_{min}$

$$V_{TRIP} = V_{DD}\left(\frac{.2 + .8\sqrt{1/3}}{1 + \sqrt{1/3}}\right) = .42 V_{DD}$$

* V_{TRIP} for $W_2/W_1 = \frac{\mu_n}{\mu_p}$

If $W_1 = [illegible] = L_1 = L_2 = L_{min}$

$W_2 = 3W_1$

$$r = \sqrt{\frac{1}{3}\frac{W_2 L_1}{L_2 W_1}} = 1$$

$$V_{TRIP} = V_{DD}\left(\frac{.2 + .8}{1 + 1}\right) = \frac{V_{DD}}{2}$$

– Device sizing substantially affects V_{TRIP}

Device Sizing Strategies

1) Minimum Sized Devices

$V_H = V_{DD}$, $V_L = 0$ 

$V_{TRIP} \simeq .4 V_{DD}$ 

2) $V_{TRIP} = \frac{V_{DD}}{2}$

From previous example, observe that

$$\frac{\mu_p}{\mu_n}\frac{W_2 L_1}{L_2 W_1} = 1$$

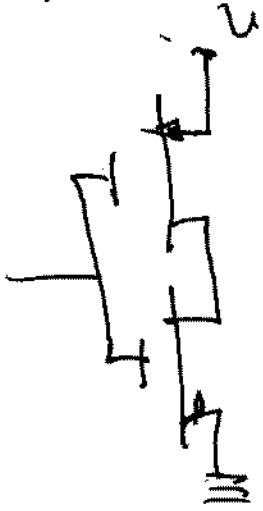
Thus

$$L_1 = L_2 = L_{min}$$
$$W_1 = W_{min}$$
$$W_2 = 3W_{min}$$

3) Equal t_{HL} & t_{LH}

- slow in the timing
- pull up time is slow when minimum sized devices are used

For equal t_{RISE} and t_{FALL}



$$R_{PD} = R_{PU}$$

$$\therefore \quad \frac{L_1}{\mu_n C_{ox} W_1 (V_{DD} - V_{Tn})} = \frac{L_2}{\mu_p C_{ox} W_2 (V_{DD} + V_{Tp})}$$

$$t_{HL} = C_{REF} R_{PD}$$

$$t_{LH} = C_{REF} R_{PU}$$

$$\frac{L_1}{W_1}\frac{W_2}{L_2} = \frac{\mu_n}{\mu_p}\left(\frac{V_{DD} - V_{Tn}}{V_{DD} + V_{Tp}}\right)$$

$$W_2 = W_1 \left(\frac{\mu_n}{\mu_p}\right)\left(\frac{V_{DD} - V_{Tn}}{V_{DD} + V_{Tp}}\right)$$

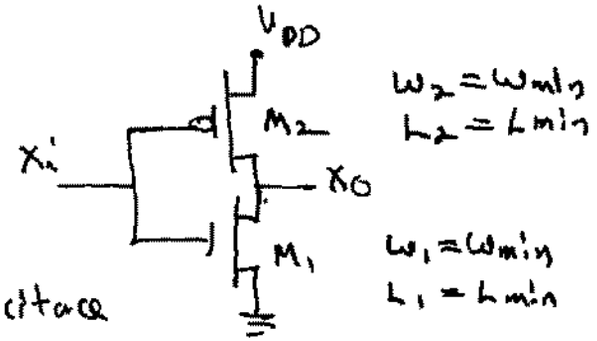
If $V_{Tn} = .2V_{DD}$, $V_{Tp} = -.2V_{DD}$

$$\boxed{W_2 = \left(\frac{\mu_n}{\mu_p}\right) W_1}$$

Note: with these threshold choices, ~~or~~ $V_{TRIP}/2$ sizing criterion is identical to equal rise/fall criteria. ☺

How does the total delay for the minimum sized Inverter compare to that of the equal rise/fall time inverter?

Case I. minimum sized



Define C^* to be the input capacitance to this inverter. $\therefore$

$$C^* = 2 C_{OX} W_{min} L_{min}$$

$$R^*_{pd} = \frac{L_{min}}{\mu_n C_{OX} W_{min} (V_{DD} - V_{Tn})}$$

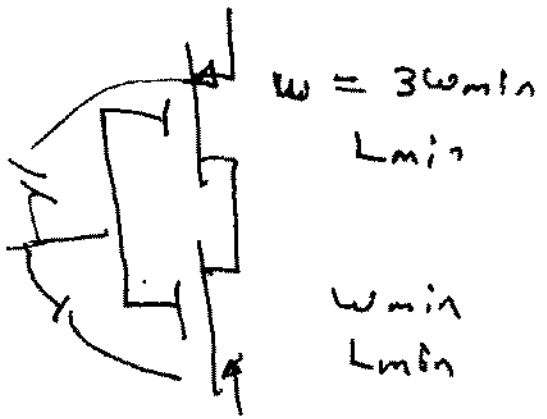
$$R^*_{pu} = 3 R^*_{pd}$$

$\therefore$ $t_{HL} + t_{LH} = R^*_{pd} C^* + R^*_{pu} C^*$

$= R^*_{pd} C^* + 3 R^*_{pd} C^*$

$= 4 R^*_{pd} C^*$

Case 2. Equal Rise & Fall time.



$$C_{REF} = C_{ox} W_{min} L_{min} + C_{ox} 3W_{min} L_{min}$$

$$= 4 C_{ox} W_{min} L_{min}$$

$$t_{HL} = R_{pd} C_{REF}$$

$$t_{HL} + t_{LH} = 2 R_{pd} C_{REF}$$

$$= 2 R_{pd} 4 C_{ox} W_{min} L_{min}$$

$$= 4 R_{pd}^{*} C_{REF}^{*}$$

$\therefore$ speed is identical !

There is no speed improvement with the equal rise/fall time sizing but the total switched capacitance has doubled and the area is modestly larger.