EE 434
Lecture 32

Multiple Input Logic Gates
Review from last time

- For equal rise & fall times, \( \frac{w_p}{w_n} = \frac{M_n}{M_p} \)

- No improvements nor degradation in speed compared to minimum device sizing strategy
- Higher \( C_{ih} \) (by 2x)
  - Higher dynamic power dissipation
  - More area
  - More design complexity
- Equal rise/fall structures widely used.
Multiple Input Gates

Example:

\[ t_{HL} = C_{REF} R_{PD} \quad \text{worst} \]
\[ t_{LH} = C_{REF} (3 R_{PD}) \]
\[ = 9 C_{REF} R_{PD} \]

\[ \text{for } \frac{W}{L} = 3 \]

Note: \( t_{LH} \) is really slow with minimum sizing strategy if the number of inputs is large.
Example (all minimum size)

\[ t_{HL} = C_{REF}(2Rpa) \]

\[ t_{LH} = C_{REF}(3Rpa) \quad \text{worst case} \]

2-input NAND
Multiple Input NAND Gates

\[ R_{pa} = n \quad R_{pa_1} = R_{pa_n} \]
\[ R_{pa_1} = \frac{R_{pa_n}}{n} \]
\[ L_1 = L_{\text{min}} \]
\[ w_1 = n w_{\text{min}} \]

\[ F_I = \frac{3(n+1) w_{\text{min}}}{n} \]
\[ F_I = (3+n) w_{\text{min}} \frac{1}{n} \]
\[ F_I = \frac{3+n}{4} \frac{w_{\text{min}}}{n} \]

\[ R_{pu} = R_{pu_1} \]
\[ L_p = L_{\text{min}} \]
\[ w_p = w_{\text{min}} \quad 3 \]
Sizing for equal rise & fall times (equal to that of n.e. inverter)

**Multiple-input NOR**

- Area gets large
- Layout dependent upon \( n \) size

\[ w = w_{\text{min}} \]
\[ L = L_{\text{min}} \]

\[ C_{\text{in}} = C_{\text{REF}} = \frac{4}{\pi^2 w_{\text{min}} L_{\text{min}}} \]

\[ C_{\text{REF}} = \frac{4}{\pi^2 w_{\text{min}} L_{\text{min}}} \]

\[ R_{\text{pneq}} = \eta \left( 3 R_{\text{pd}} \right) \text{ if minimum sized} \]

\[ R_{\text{in}} = R_{\text{pd}} \]
\[ R_{\text{on}} = \frac{R_{\text{pd}}}{\eta} \]
\[ L = L_{\text{min}} \]
\[ w = 3n w_{\text{min}} \]

\[ F_I = \left( 3n + 1 \right) w_{\text{min}} L_{\text{min}} \text{ CREF} \]

\[ F_I = 3n + 1 \]
NAND: \[ F_I = \left( \frac{3+n}{4} \right) \text{CREF} \]

NOR: \[ F_I = \left( \frac{3n+1}{4} \right) \text{CREF} \]

Observe: Capacitive loading presented by NOR gates much larger than that due to NAND gates if \( n \) is large.
Overdriven (strength relative to a first inverter)

\[ \omega_n = k \omega_{\text{min}} \quad \ell_n = \ell_P = \ell_{\text{min}} \]

\[ w_P = k (3 \omega_{\text{min}}) \]

Widths of all devices are scaled by a factor or \( k \) relative to that of the nonscaled device.
\[ t_{HL} = t_{REF} \left( \frac{C_{LOAD}}{C_{REF}} \right) \]

\[ t_{HL} = \frac{t_{REF}}{k} \left( \frac{C_{LOAD}}{C_{REF}} \right) \]
Example 1

\[ V_i \]

\[ V_o \]

\[ t_{HL_1} \quad t_{LH_2} \quad t_{HL_3} \]

\[ t_{HL} = t_{HL_1} + t_{LH_2} + t_{HL_3} \]

\[ t_{HL_1} = t_{REF} \left( \frac{C_{L_1}}{C_{REF}} \right) = t_{REF} \left( 2 \right) \left( \frac{3+2}{4} \right) = \frac{5}{2} \cdot t_{REF} \]

\[ t_{LH_2} = t_{REF} \frac{C_{L_2}}{2 \cdot C_{REF}} = t_{REF} \left( \frac{1}{2} \right) \]

\[ t_{HL_3} = t_{REF} \left( \frac{C_L}{C_{REF}} \right) \]

\[ t_{HL} = \left( \frac{5}{2} + \frac{1}{2} + \frac{C_L}{C_{REF}} \right) \cdot t_{REF} \]
Calculating Delay in Combinational Logic Circuits — A Summary

1) Partition a delay path of interest into a chain of individual gates, (assume number is $M$).

2) Determine $FI_k$, $OD_k$

\[ t = \sum_{k=1}^{M} t_{dk} \]

where $t$ is the overall propagation delay $(t_{HL} + t_{ LH})$ and $t_{dk}$ is the propagation delay of stage $k$. 
\[ t_{ak} = \frac{t_{REF}}{OD_k} FI_{k+1} \]

where \( FI_k = \frac{C_{ink}}{C_{REF}} \) and \( 2 \leq k \leq M \)

\[ FI_{mti} = \frac{C_{m}}{C_{REF}} \]

\[ t = \left( \sum_{k=1}^{M} \frac{FI_{k+1}}{OD_k} \right) t_{REF} \]