EE 434

Lecture 32

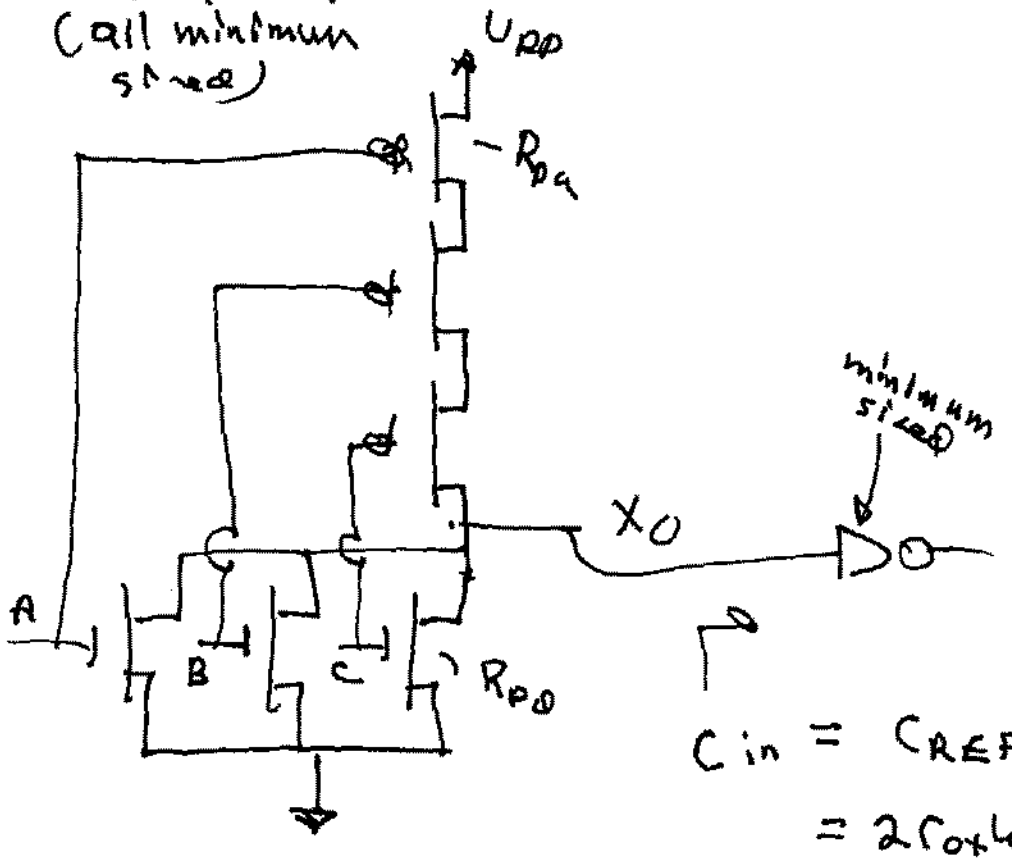
Multiple Input Logic Gates

Review from last time

- for equal rise & fall times, $\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$
- no improvements nor degradations in speed compared to minimum device sizing strategy
- – higher C_{in} (by 2x)
  – higher dynamic power dissipation
  – more area
  – more design complexity
- Equal rise/fall structures widely used.

Multiple Input Gates

Example:



3-input NOR

$C_{in} = C_{REF}$

$= 2 C_{ox} L_{min} W_{min}$

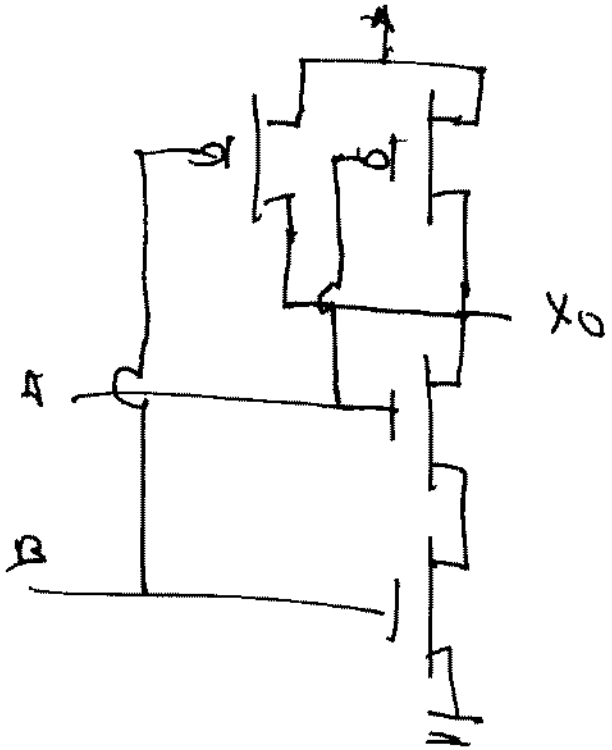
$t_{HL} = C_{REF} R_{pd}$ ← worst case

$t_{LH} = C_{REF}(3 R_{pu})$

$= 9 C_{REF} R_{pd}$ for $\frac{\mu_n}{\mu_p} = 3$

Note: t_{LH} is really slow with minimum sizing strategy if # inputs is large.

Example (all minimum size)



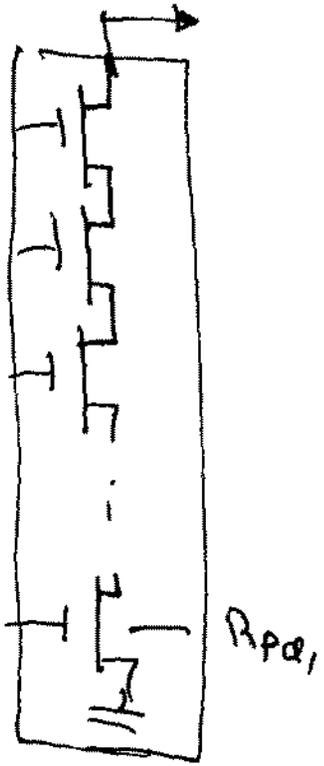
2-input NAND

$t_{HL} = C_{REF}(2R_{PD})$

$t_{LH} = C_{REF}(3R_{PD})$ worst case

Multiple Input NAND Gates

P_Q:

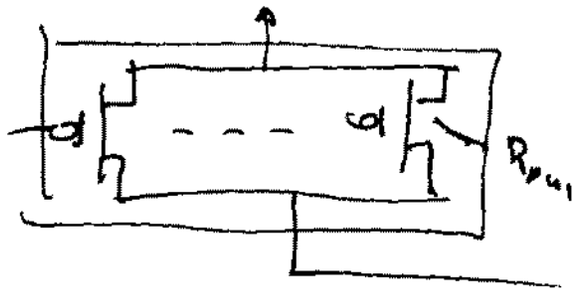


$$R_{pQ} = n\,R_{pQ_1} = R_{pQ_n}$$

$$\therefore\quad R_{pQ_1} = \frac{R_{pQ_n}}{n}$$

$$\therefore\quad L_1 = L_{min}$$

$$W_1 = n\,W_{min}$$



$$R_{pu} = R_{pu_1}$$

$$\therefore\quad L_p = L_{min}$$

$$W_p = W_{min}\,3$$

$$FI = 3C_{ox}W_{min}L_{min} + n\,C_{ox}W_{min}L_{min}$$

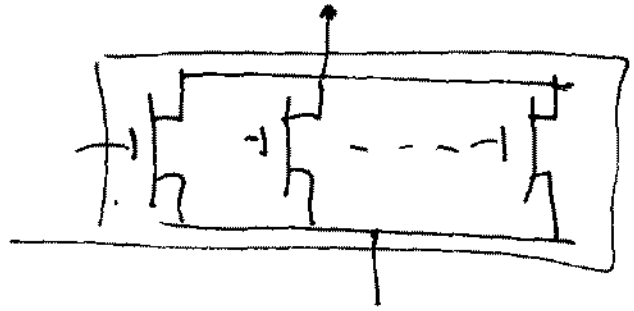
$$FI = (3+n)C_{ox}W_{min}L_{min}$$

$$\boxed{FI = \frac{3+n}{4}\,C_{REF}}$$

Sizing for equal rise & fall times (equal to that of ref. inverter)

multiple-input NOR

PD:



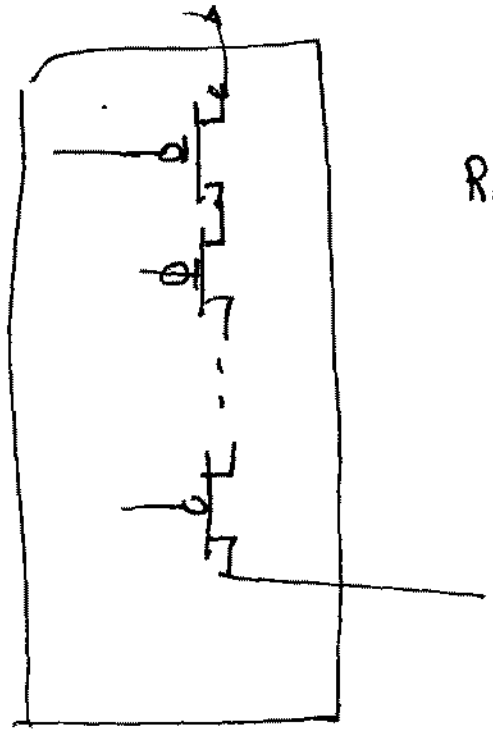
$W = W_{min}$

$L = L_{min}$

$C_{in} = C_{REF} = 4 C_{ox} W_{min} L_{min}$

$C_{REF} = 4 C_{ox} W_{min} L_{min}$

PU:



$R_{pueq} = n\,(3 R_{pd})$ if minimum sized

$n R_{pu} = R_{pd}$

$R_{on} = \frac{R_{pd}}{n}$

$L = L_{min}$

$W = 3n W_{min}$

$FI = (3n W_{min} L_{min} + W_{min} L_{min}) C_{ox}$

$FI = (3n+1) W_{min} L_{min} C_{ox}$

- Fan In increases

$$FI = \frac{3n+1}{4} C_{REF}$$

- Area gets large
- Layout dependent upon n sizing

NAND: $FI = \left(\frac{3+n}{4}\right) C_{REF}$

NOR: $FI = \left(\frac{3n+1}{4}\right) C_{REF}$

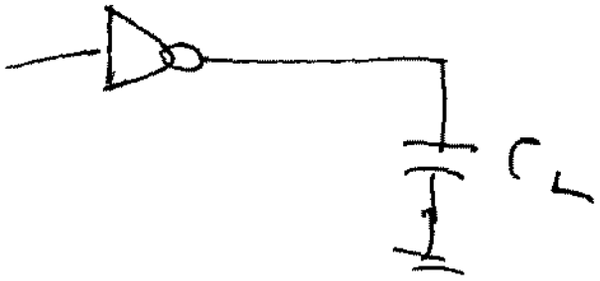
Observe: Capacitative loading presented by NOR gates much larger than that due to NAND gates if n is large

Overdrive (strength relative to a first inverter)

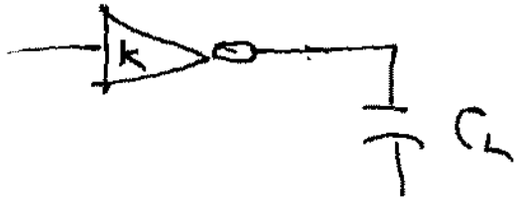
$W_n = K W_{min}$ $\quad L_n = L_p = L_{min}$

$W_p = K(3W_{min})$

widths of all devices are scaled by a factor of K relative to that of the nonscaled device.

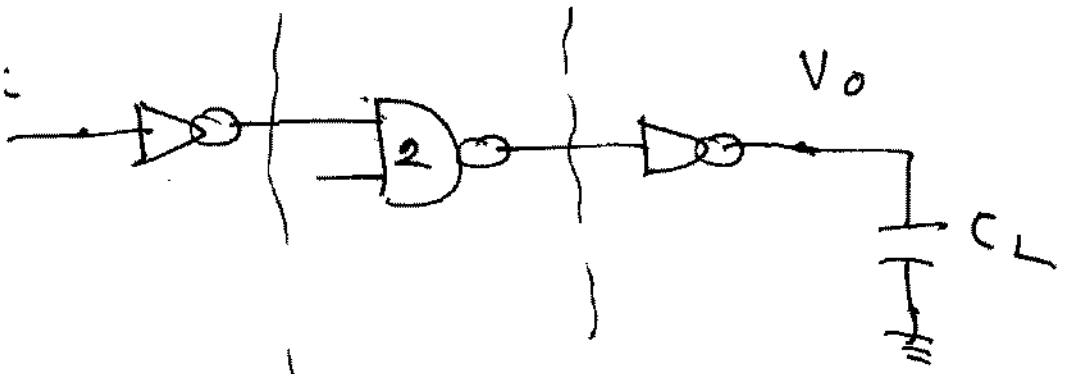


$$t_{HL} = t_{REF}\left(\frac{C_{LOAD}}{C_{REF}}\right)$$



$$t_{HL} = \frac{t_{REF}}{k}\left(\frac{C_{LOAD}}{C_{REF}}\right)$$

Example !



$$t'_{HL} = t_{HL_1} + t_{LH_2} + t_{HL_3}$$

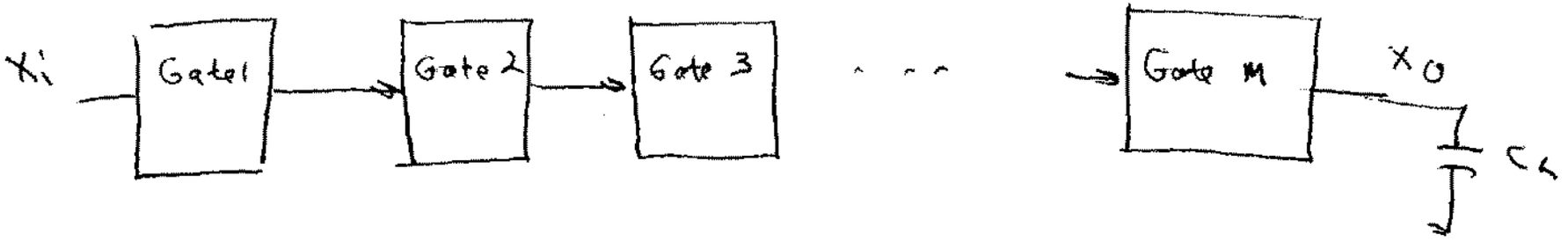
$$t_{HL1} = t_{REF}\left(\frac{C_{L1}}{C_{REF}}\right) = t_{REF}\left(2\right)\left(\frac{3+2}{4}\right) = \frac{5}{2}t_{REF}$$

$$t_{LH2} = \frac{t_{REF}}{2}\frac{C_{L2}}{C_{REF}} = t_{REF}\left(\frac{1}{2}\right)$$

$$t_{HL3} = t_{REF}\left(\frac{C_L}{C_{REF}}\right)$$

$$\therefore \quad t'_{HL} = \left(\frac{5}{2} + \frac{1}{2} + \frac{C_L}{C_{REF}}\right) t_{REF}$$

Calculating Delay in Combinational Logic Circuits – A Summary



1) Partition a delay path of interest into a chain of individual gates, (assume number is M).

2) Determine FI_k, OD_k

$$t = \sum_{k=1}^{M} t_{dk}$$

where t is the overall propagation delay ($t_{HL} + t_{LH}$) and t_{dk} is the propagation delay of stage k

$$t_{ak} = \frac{t_{REF}}{OD_k} \; FI_{k+1}$$

where $FI_k = \frac{C_{ink}}{C_{REF}}$ ~~and~~ $2 \leq k \leq M$

$$FI_{M+1} = \frac{C_L}{C_{REF}}$$

$$\therefore \quad t = \left(\sum_{k=1}^{M} \frac{FI_{k+1}}{OD_k} \right) t_{REF}$$