# EE 434

## Lecture 34

## Other Logic Styles

# Other Logic Design Strategies

Consider an Example! $f = A \oplus B$

- This simple function is one of the small number of "gates" that have two inputs and one output

Gates with 2 inputs, 1 output.

NAND
NOR
AND
OR
XOR
XNOR

| A | B | C |
|---|---|---|
| 0 | 0 | 0, 1 |
| 0 | 1 | 0, 1 |
| 1 | 0 | 0, 1 |
| 1 | 1 | 0, 1 |

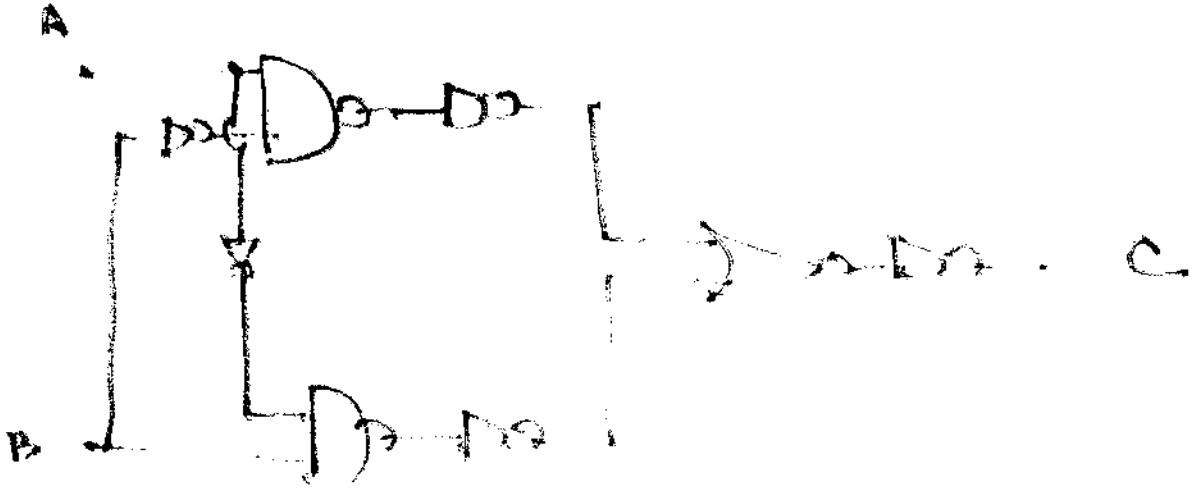
∴ Total # of 2 input, 1 output gates is 16

# 16 - gate

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| C = 0 | AB | $A\bar{B}$ | A | $\bar{A}B$ | B | ~~A+B~~ $A \oplus B$ | A + B |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $\overline{A+B}$ | $\overline{A \oplus B}$ | $\bar{B}$ | $\overline{A\bar{B}}$ | $\bar{A}$ | $\overline{AB}$ | ~~$\overline{A+B}$~~ $\overline{A \cdot B}$ | C = 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

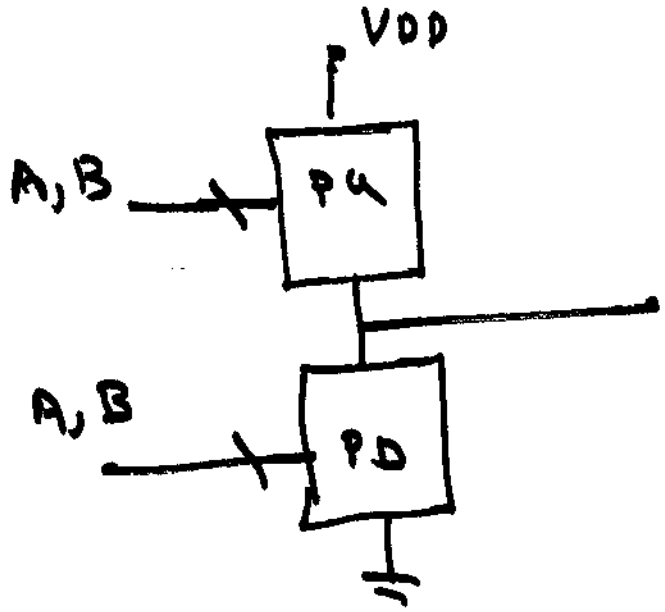
$A \oplus B = A\bar{B} + B\bar{A}$




22 transistors for static CMOS imp.

5 levels of logic

$$C = A \oplus B = A\bar{B} + B\bar{A}$$




- PU network & PD network never both conducting
- PU or PD network is conducting

for pd network, consider

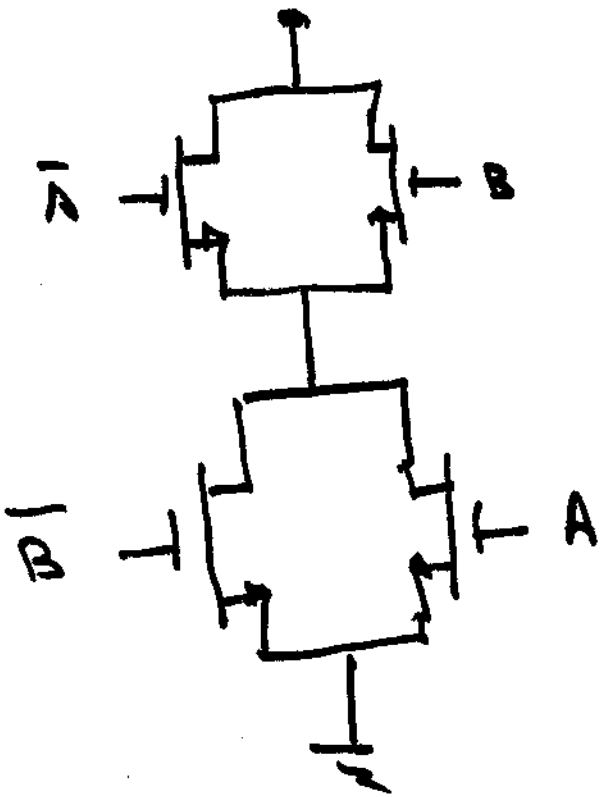
$$\bar{C} = \overline{A\bar{B} + B\bar{A}}$$

$$= \overline{A\bar{B}} \cdot \overline{B\bar{A}}$$

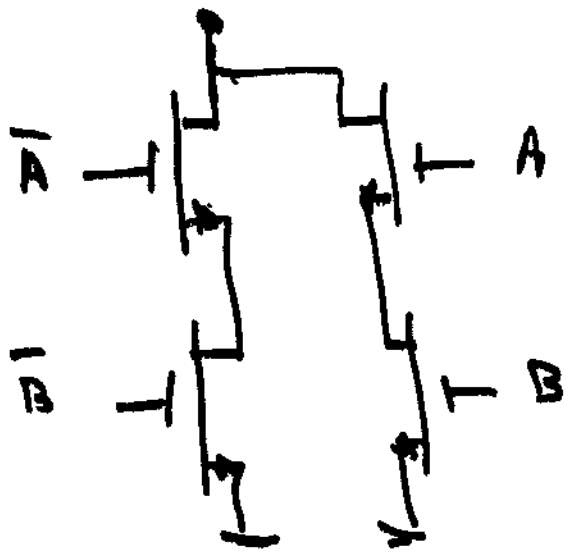
$$= (\bar{A} + B) \cdot (\bar{B} + A)$$

$$\bar{C} = (\bar{A}+B)\cdot(\bar{B}+A) = \bar{A}\bar{B} + \bar{A}A + B\bar{B} + AB$$

$$= \bar{A}\bar{B} + AB$$




8 transistors




8 transistors

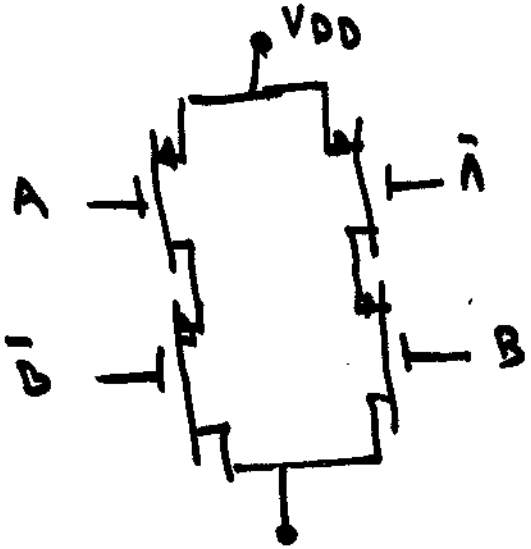
4 trans. for pd function

4 trans for variable comp. function.

$C = \bar{A}B + A\bar{B}$

for p-chanel devices

$C = A\bar{B} + \bar{A}B$




8 transistors

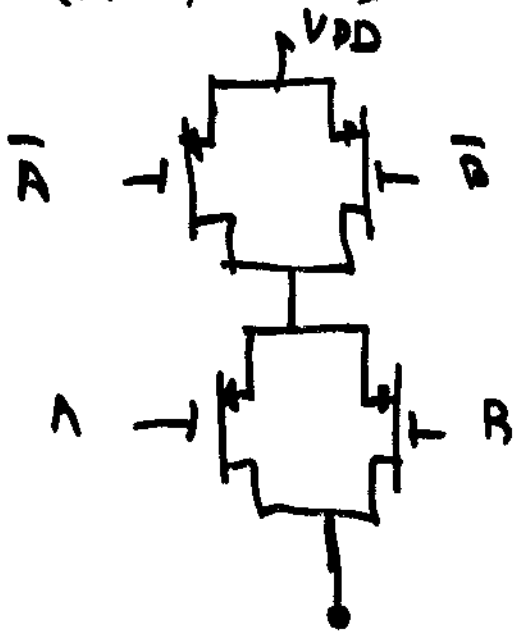
4 trans for pu

4 trans for ver. comp

$A\bar{B} + \bar{A}B + A\bar{A} + B\bar{B} =$

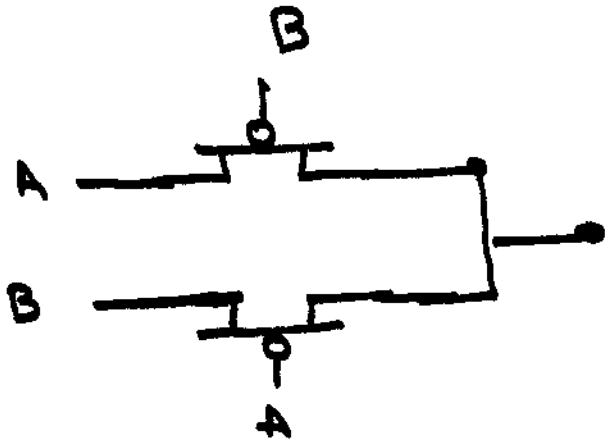
$\bar{A}(A+B) + \bar{B}(A+B) =$

$(\bar{A}+\bar{B})\cdot(A+B)$



Another Alternative.

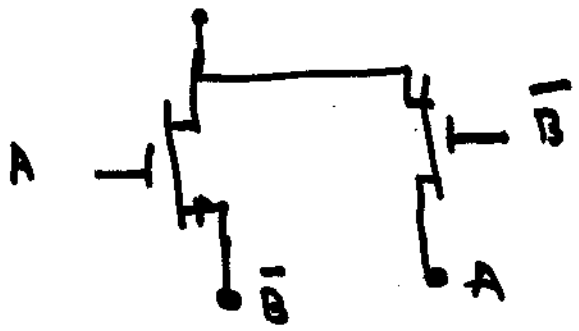
Pu network : $A\bar{B} + B\bar{A}$



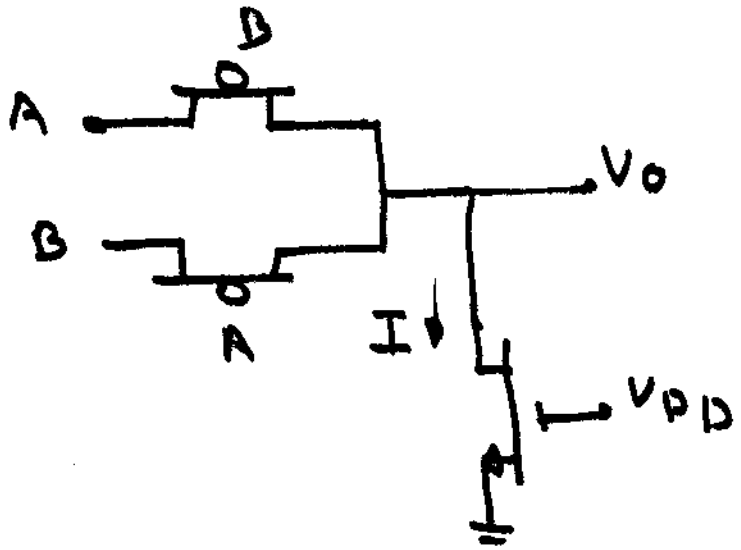

# transistors : 2

Another Pull-Down Network.

$$\overline{C} = \overline{A}\,\overline{B} + AB$$




4 - transistors



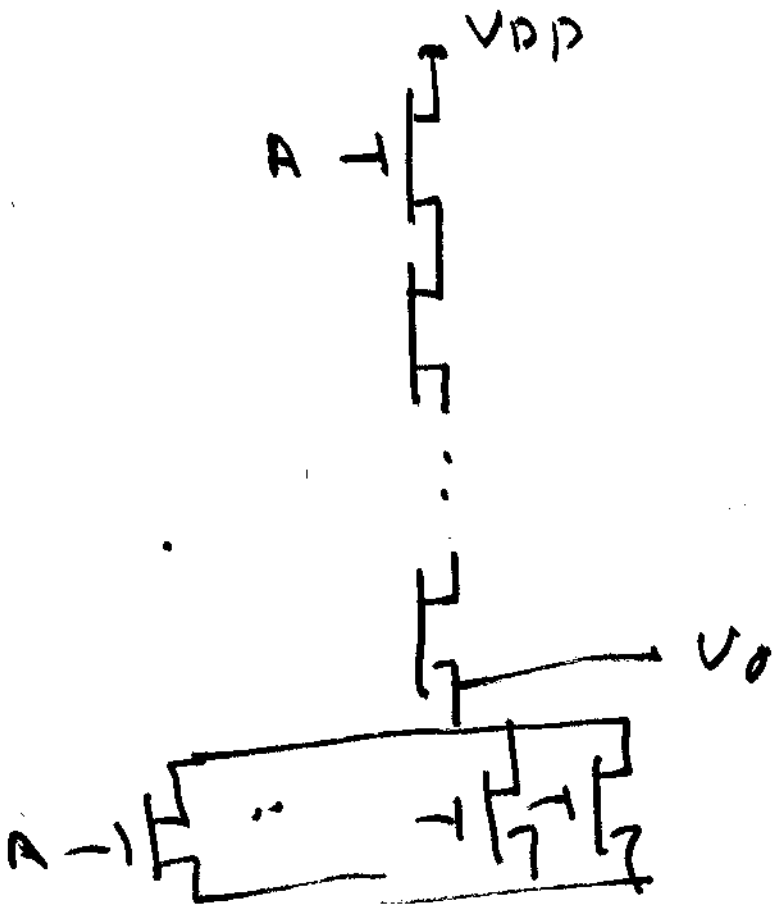

- 3-transistor implementation

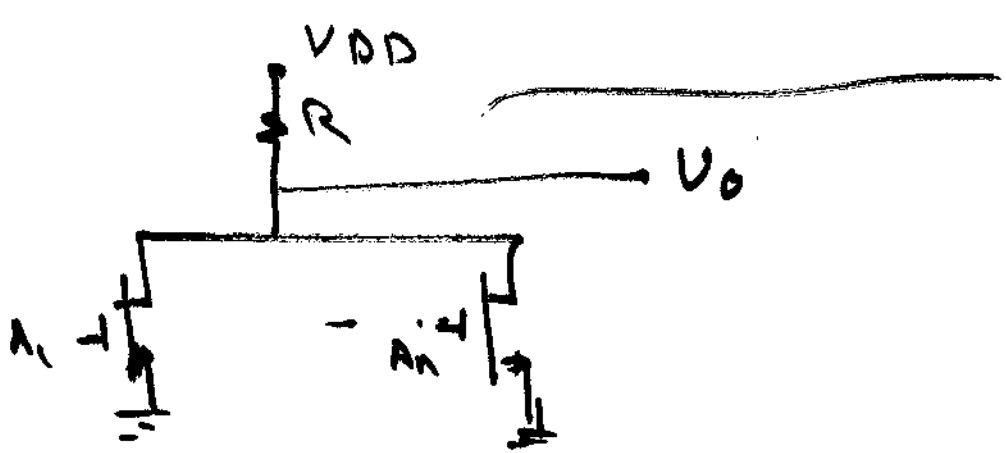
- when $V_o$ is high
  - a) $V_o$ is not quite $D_{DD}$
  - b) $P_{STATIC} \approx V_{DD} I$

- when $V_o$ is low
  - $V_o$ is zero
  - $P_{STATIC} = 0$

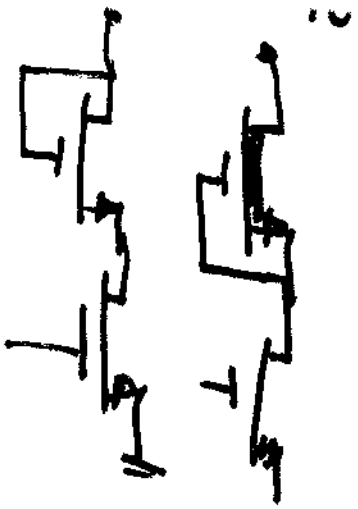
Often the necessity of implementing a function in SOP form when many input variables are present exists often necessary to implement a function in POS form where there are many input variables.

Consider the multiple-input NOR gate.:









Pseudo-NMOS Logic

- ratioed logic
- $P_{STATIC} = \begin{cases} 0 & \text{when } V_o \text{ high} \\ V_{DD} \cdot I & \text{when } V_o \text{ low} \end{cases}$

# Styles of Logic

- Standard CMOS
- Complex Logic Gates
- Pass Transistor Logic
- Pseudo NMOS
- Dynamic or Domino Logic