

EE 434

Lecture 35

Other Logic Design Styles  
(Logical Effort)

## Review from last time

- Dynamic power dissipation dominant in most useful CMOS Logic
  - Dependent upon  $f$ ,  $C_L$ ,  $V_{DD}$
- Alternate Logic Styles often result in considerable improvements in performance in some applications
- Standard CMOS is still the dominant logic of choice

# Logical Effort

Recall:  $t = t_{\text{eff}} \sum_{i=1}^n \frac{FI_{i+1}}{OD_i}$

WH:  $t = \sum_{i=1}^n g_i h_i$

$g$  is the logical effort  
 $h$  is the electrical effort

$g$ : ratio of input capac. of gate to input cap. of inverter that can deliver the same output current

$h$ : ratio of load capacitance to input capacitance

Using either approach will give the same results!

## Other Logic Styles

- Static CMOS
- Complex Logic Gates
- Pass Transistor Logic
- Pseudo NMOS
- Dynamic Logic Styles

## Static CMOS:

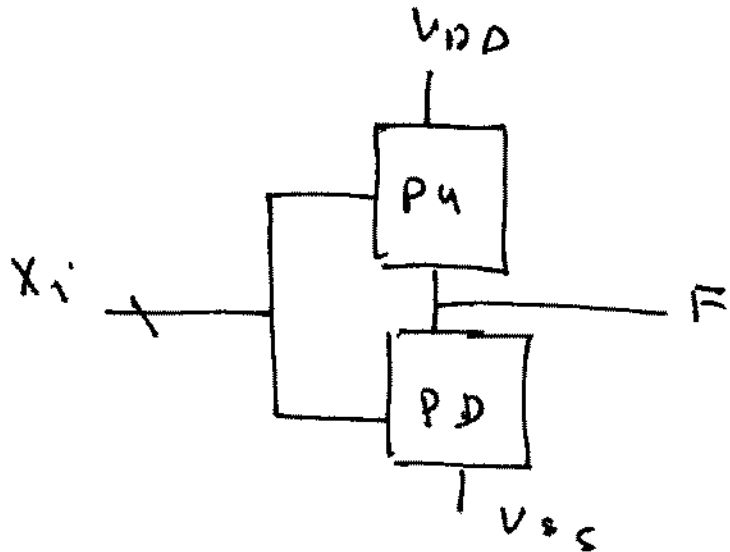
- $V_H = V_{DD}$  ,  $V_L = V_{SS}$

- Static power dissipation = 0

= Created around a P<sub>n</sub>, P<sub>D</sub> network concept

(same Boolean info. carried in P<sub>n</sub> as in P<sub>D</sub> network)

## Complex Logic Gates



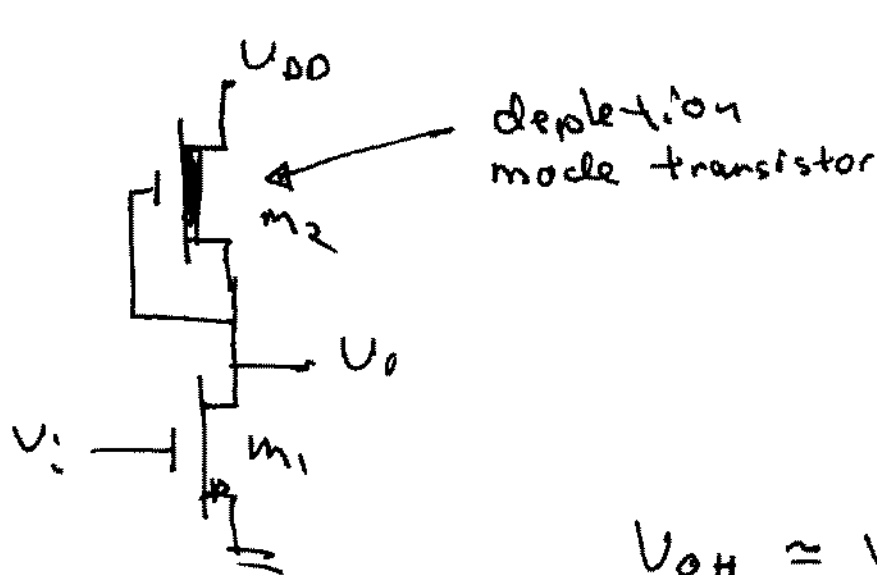
- allowed more complicated logic functions in  $P_n$  &  $P_p$  networks

## Review

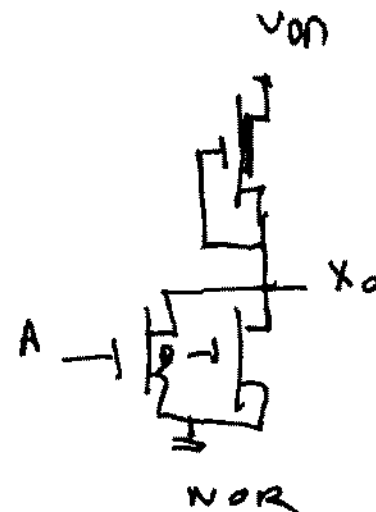
- Realize  $\bar{F}$  with n-channel devices in  $P_p$  network  
F with p-channel devices in  $P_n$  network
- Dramatic Reduction in device count
- # Levels of logic is often reduced (to 2)

# - nmos Logic (pmos)

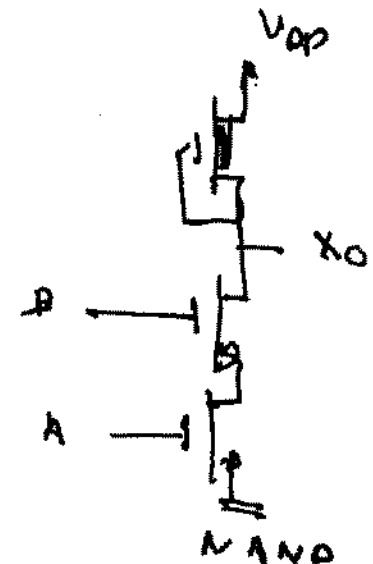
dominant MOS Logic family until ~ 1985



NMOS



NOR



NAND

$$V_{OH} \approx V_{DD}$$

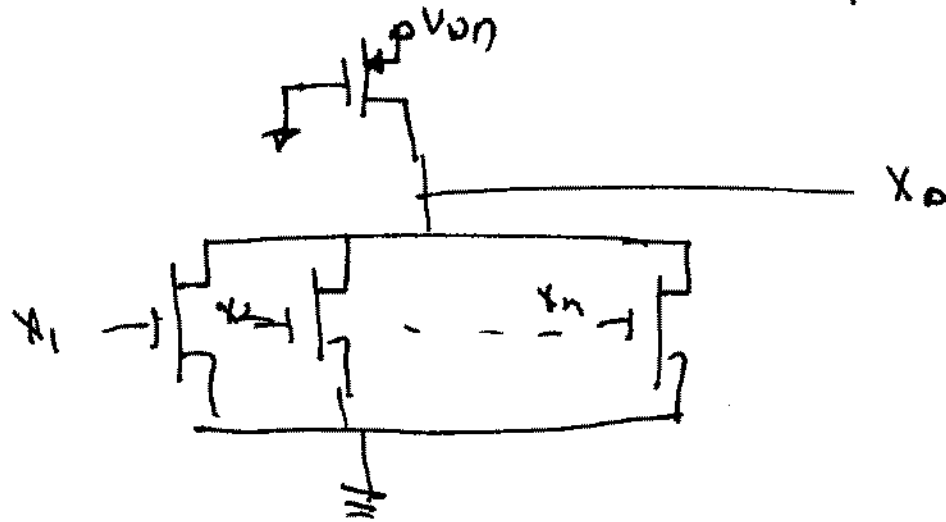
$V_{OL}$  - depends upon sizing of  $M_1$  &  $M_2$

" - " static power dissipation is not 0 when  $V_o = V_L$

- " + "
- less transistors
  - less interconnect traffic
  - eliminate need for wells (area wells is big)
  - cost of adding wells is also large

## - Pseudo NMOS

multiple-input NOR gates.

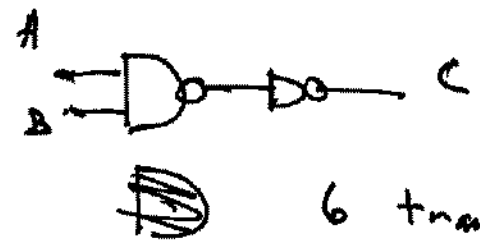


applicable primarily when a large number of inputs on a NOR gate are required!



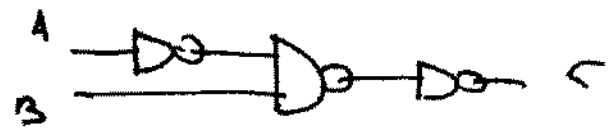
# Pass Transistor Logic

Example!  $A \cdot B$   $\frac{\text{static}}{\text{cmos}}$

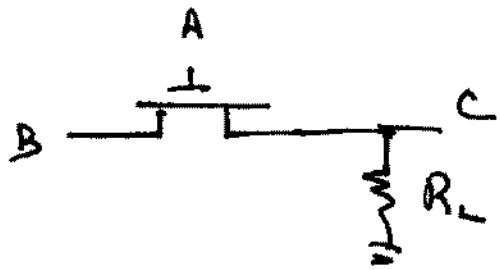


6 transistors  
2 levels of logic

$\bar{A} \cdot B$



8 transistors  
3 levels of logic



1 transistor solution (+ resistor)