EE 434
Lecture 35
Other Logic Design Styles
(Logical Effort)
Review from last time

- Dynamic power dissipation
dominant in most useful
CMOS logic
  - Dependent upon $f$, $C_L$, $V_{DD}$

- Alternate logic styles often
result in considerable improvements
in performance in some applications

- Standard CMOS is still the
dominant logic of choice
Logical Effort

Recall: \( L = \log \sum_{i=1}^{n} \frac{FL_{i+1}}{0D_i} \)

Why: \( L = \sum_{i=1}^{n} gh_i \)

\( g \) is the logical effort
\( h \) is the electrical effort

\( g \): ratio of input capacitance of gate
to input capacitance of inverter
that can deliver the same output current

\( h \): ratio of load capacitance to
input capacitance

Using either approach will give the same results!
Other Logic Styles

- Static CMOS
- Complex Logic Gates
- Pass Transistor Logic
- Pseudo NMOS
- Dynamic Logic Styles
Static CMOS:

- $V_H = V_{DD}$, $V_L = V_{SS}$

- Static power dissipation = 0

- Created around a $P4$, $P4$ network concept

(same Boolean info. carried in $P4$ as in $P0$ network)
Complex Logic Gates

- Allowed more complicated logic functions in $P_n$ and $P_D$ networks

Review

- Realize $F$ with $n$-channel devices in $P_D$ network
- Realize $F$ with $p$-channel devices in $P_n$ network

- Dramatic reduction in device count
- # Levels of logic is often reduced (to 2)
nMOS Logic (pMOS)

dominant MOS logic family until ~ 1985

\[ V_{OH} = V_{DD} \]
\[ V_{OL} = \text{depends upon sizing of } M_1 \times M_2 \]

static power dissipation is not 0 when \( V_{OL} = V_{HH} \)

- less transistors
- less interconnect traffic
- eliminates need for wells (open wells is big)
- cost of adding wells is also large
- Pseudo NMOS

multiple input NOR gates.

Applicable primarily when a large number of inputs on a NOR gate are required!
Pass Transistor Logic

Example: \( A \cdot B \) to \( C \)

\[ A \cdot B \]

\( \overline{A} \cdot B \)

\[ A \]

\[ B \]

\[ C \]

6 transistors
2 levels of logic

8 transistors
3 levels of logic

1 transistor solution (+ resistor)