EE 434

Lecture 40

Array Logic

Programmable Logic Arrays (PLA)

Gate Arrays & Seas of Gates

} mask Programmable

Field Programmable Gate Arrays (FPGA) } Field Programmable

Array Logic Features

- Systematic Design Approach
- Very Quick Turn Around
- Small or no mask costs for personalization
- Late in Design Cycle Changes
- Updates or Revisions at low cost

} +

- Not competitive with fully custom
  - Cost
  - Speed
  - Power Dissipation (Dynamic

} "-"

Migration from Arra

Recall: Any Boolean Combinational Logic Function can be expressed in SOP canonical form

Ex: $F = A\bar{B} + \bar{A}BC + AB\bar{D} + \ldots$

If multiple input gates available, these functions can be implemented in 2 levels of logic ☺

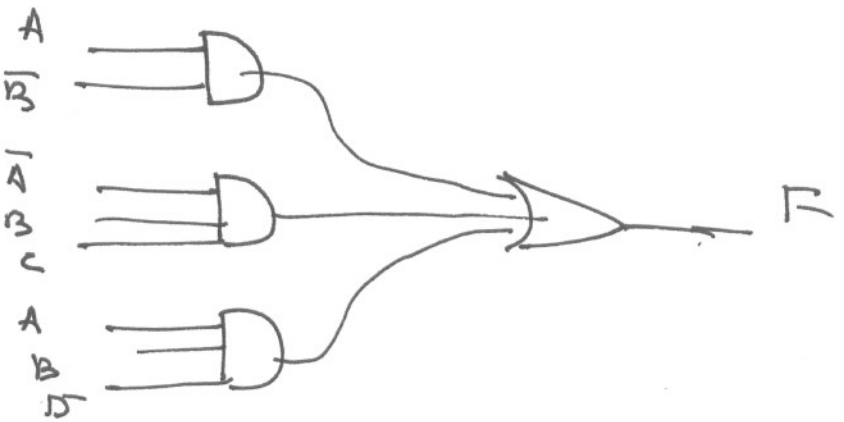
But - need AND and OR gates (not attractive)

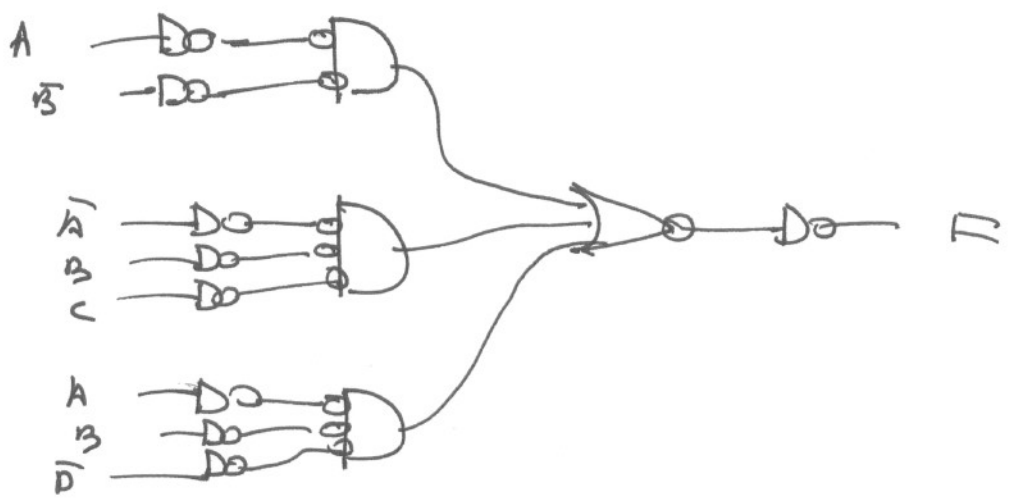
Observe $A \cdot B = \overline{\overline{A \cdot B}} = \overline{A} + \overline{B}$

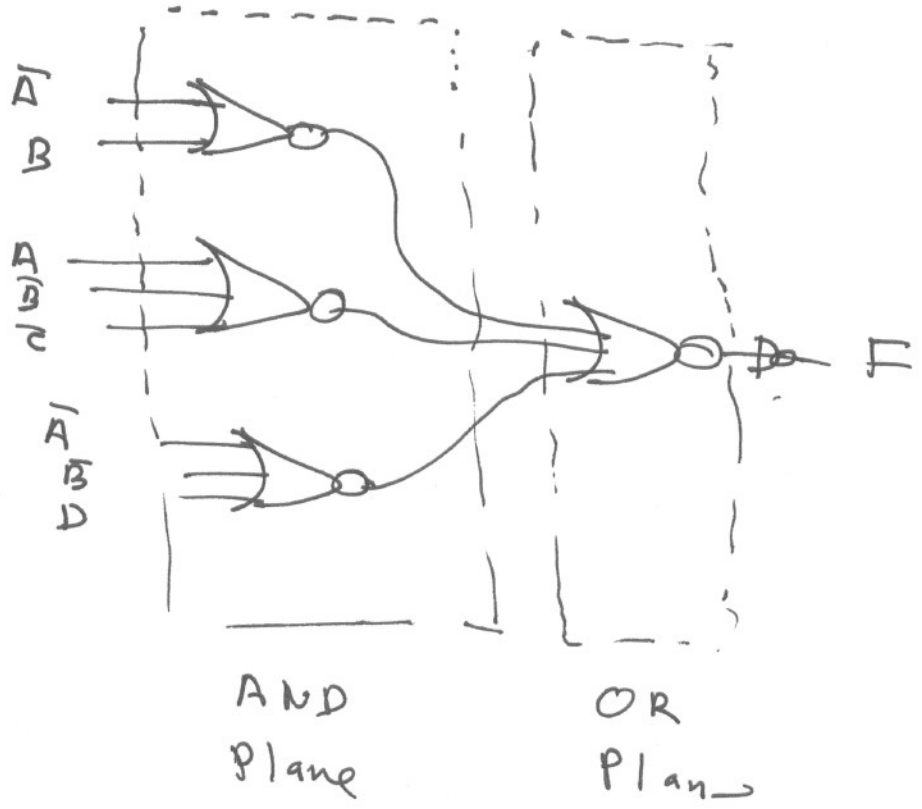
Observe

requires single inverter on final output

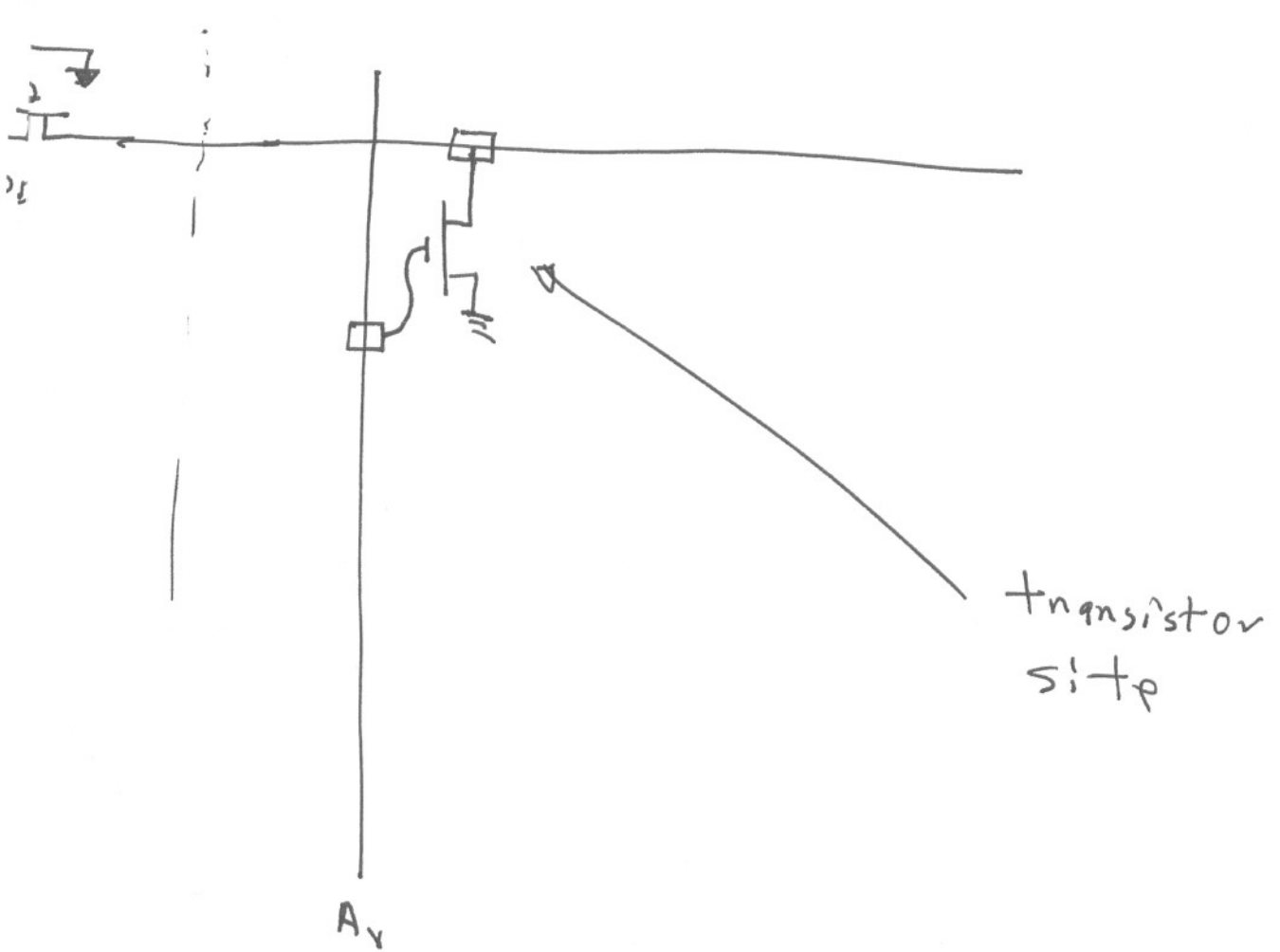
$F = A\bar{B} + A\bar{B}C + AB\bar{D}$







NOR Gate
Implementation of
Standard
SOP function


transistor
site
A_x

- Pseudo - NMOS Logic

— all sites are included.

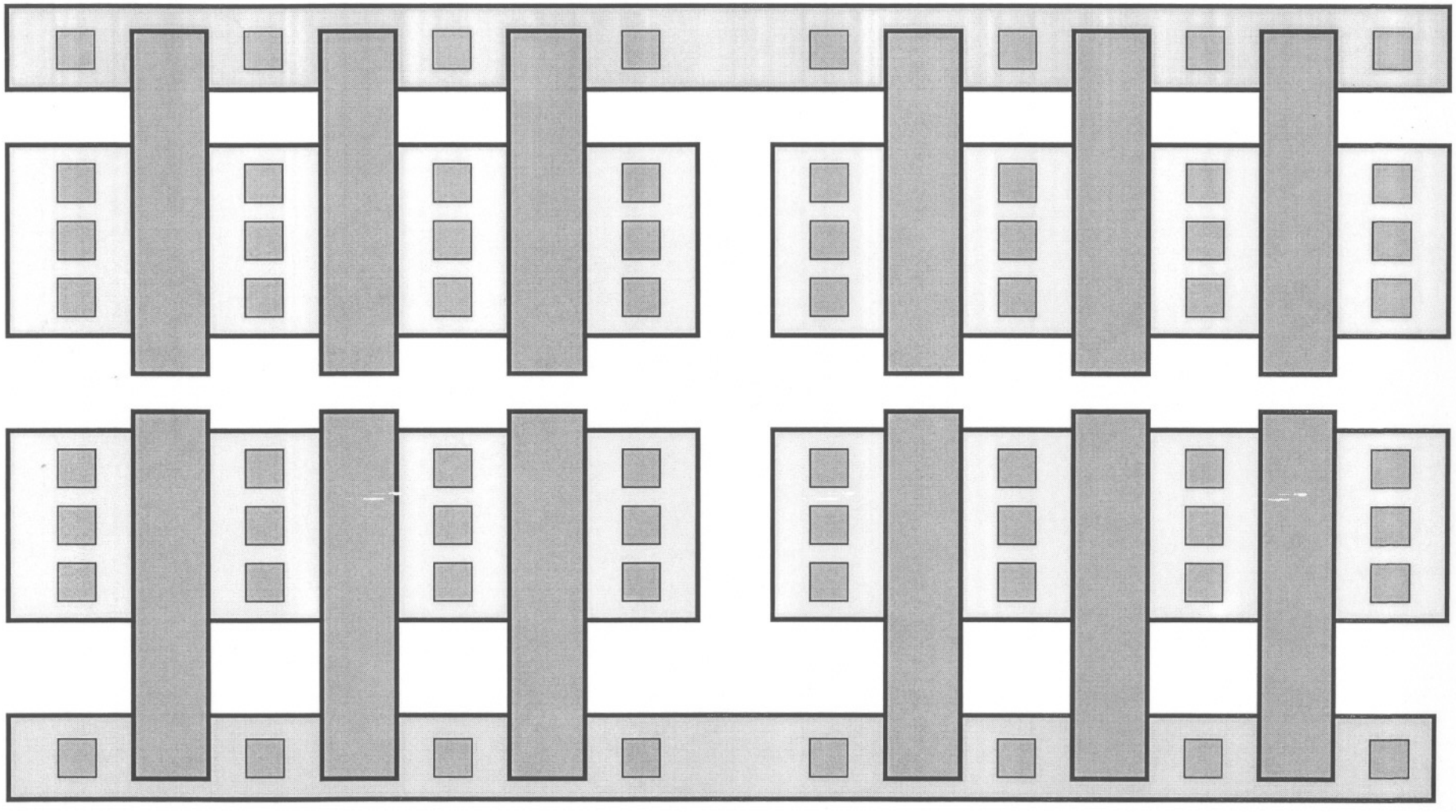
— Requires only one or two masks

— If interconnects are at a high level, requires only a few proc. steps

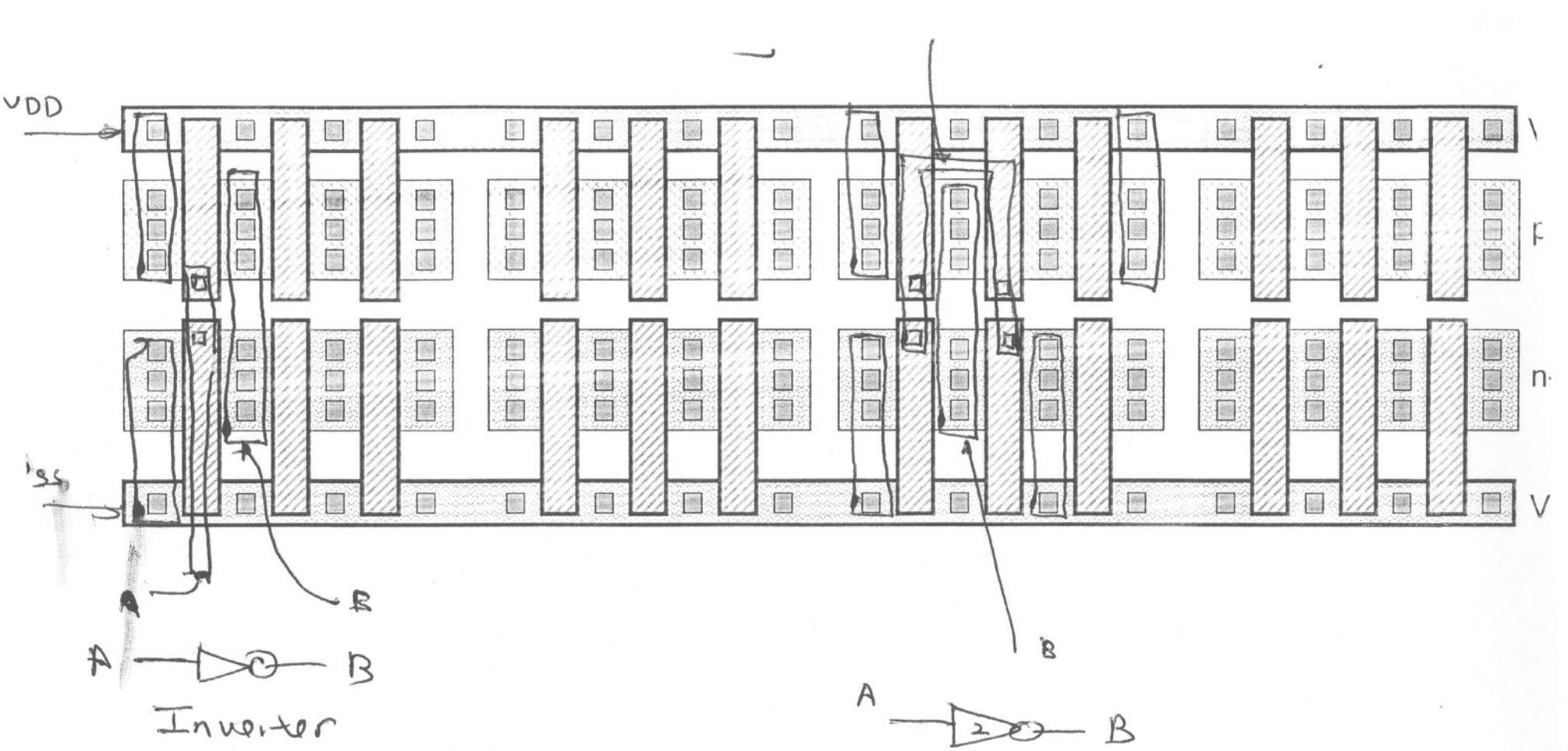
— Compatible with any Bulk CMOS proc

— Some area and power penalties

Gate Arrays and Seas of Gates



- Pattern may be repeated many times
- Compatible with essentially all CMOS processes


VDD
A
B
A
B
Inverter
B
A
2
B