EE 434
Lecture 40
Array Logic
Programmable Logic Arrays (PLA)

Gate Arrays & Seas of Gates

Field Programmable Gate Arrays (FPGA)

mask
programmable

Field Programmable
Array Logic Features

- Systematic Design Approach
- Very Quick Turn Around
- Small or no mask costs for personalization
- Late in Design Cycle Changes
- Updates or Revisions at low cost

- Not competitive with fully custom
  - Cost
  - Speed
  - Power Dissipation (Dynamic)
  - Migration from Array to Custom
Recall: Any Boolean Combinational Logic Function can be expressed in SOP canonical form.

Ex: \[ F = AB\overline{B} + \overline{A}BC + ABD + \ldots \]

If multiple input gates available, these functions can be implemented in 2 levels of logic 😊

But - need AND and OR gates (not attractive)
Observe \[ A \cdot B = \overline{A \cdot B} = \overline{A} + \overline{B} \]

Observe

\[
\begin{array}{c}
A \\
B
\end{array}
\]
\[
\begin{array}{c}
\rightarrow \\
\rightarrow
\end{array}
\]
\[
\begin{array}{c}
\overline{A} \\
\overline{B}
\end{array}
\]
\[
\rightarrow \\
F
\]

requires single inverter on final output
\[ f = AB + ABCD + AB^2D \]
NOR Gate
Implementation of Standard SOP Function
- Pseudo-NMOS Logic
- All sites are included.
- Requires only one or two masks
- If interconnects are at a high level, requires only a few proc. steps
- Compatible with any bulk CNOS proc.
- Some area and power penalties
Gate Arrays and Seas of Gates
- Pattern may be repeated many times
- Compatible with essentially all CMOS processes