EE 434

Lecture 41

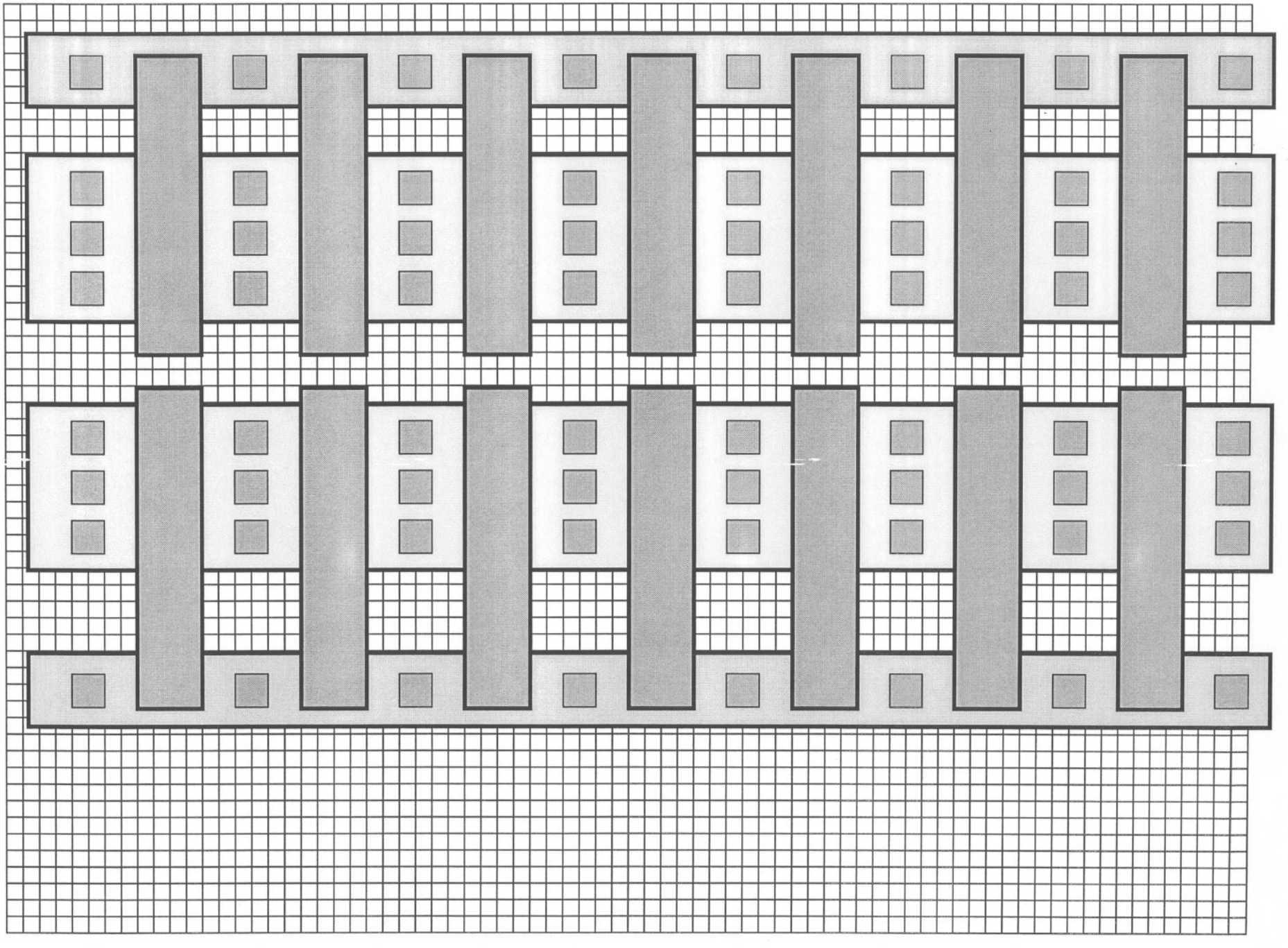
Array Logic

- Sea of Gates
- Mask Programmable ROM
- FPGA

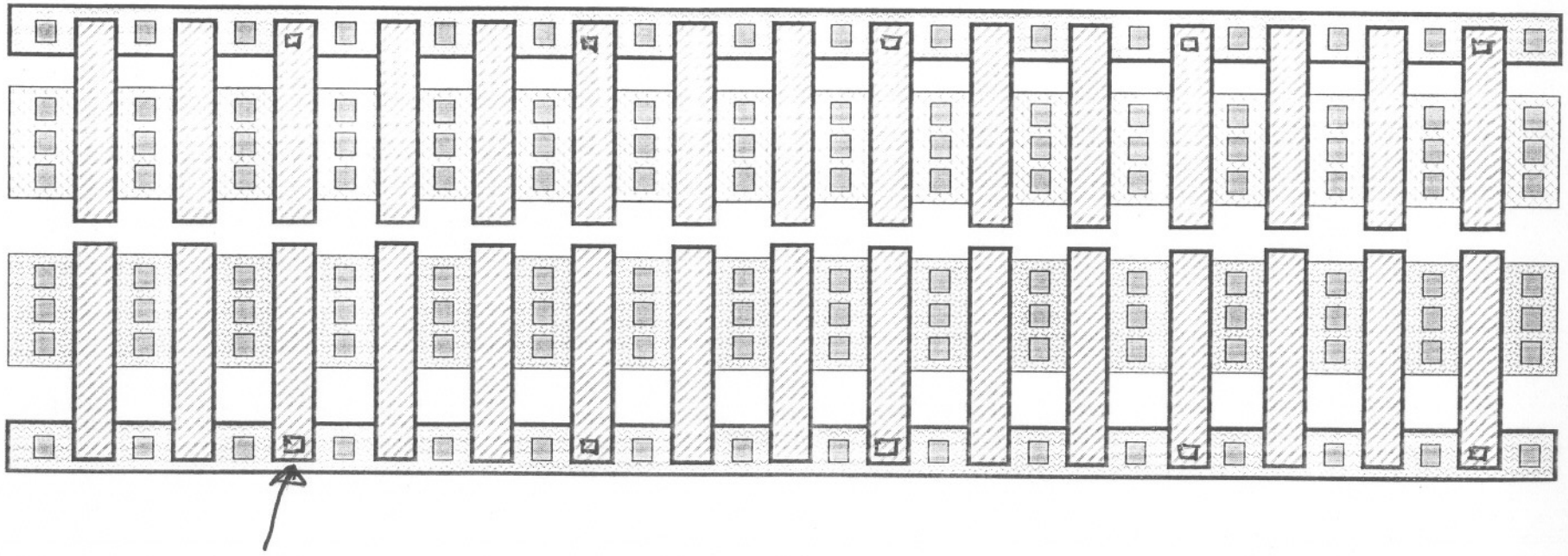

V
p
n
V
V_O
V_{DD}
A
B

- If more inputs are needed
  can use multiple cells
- waste is common
  - both within a cell
  - within the array

Basic Sea of Gates Structure

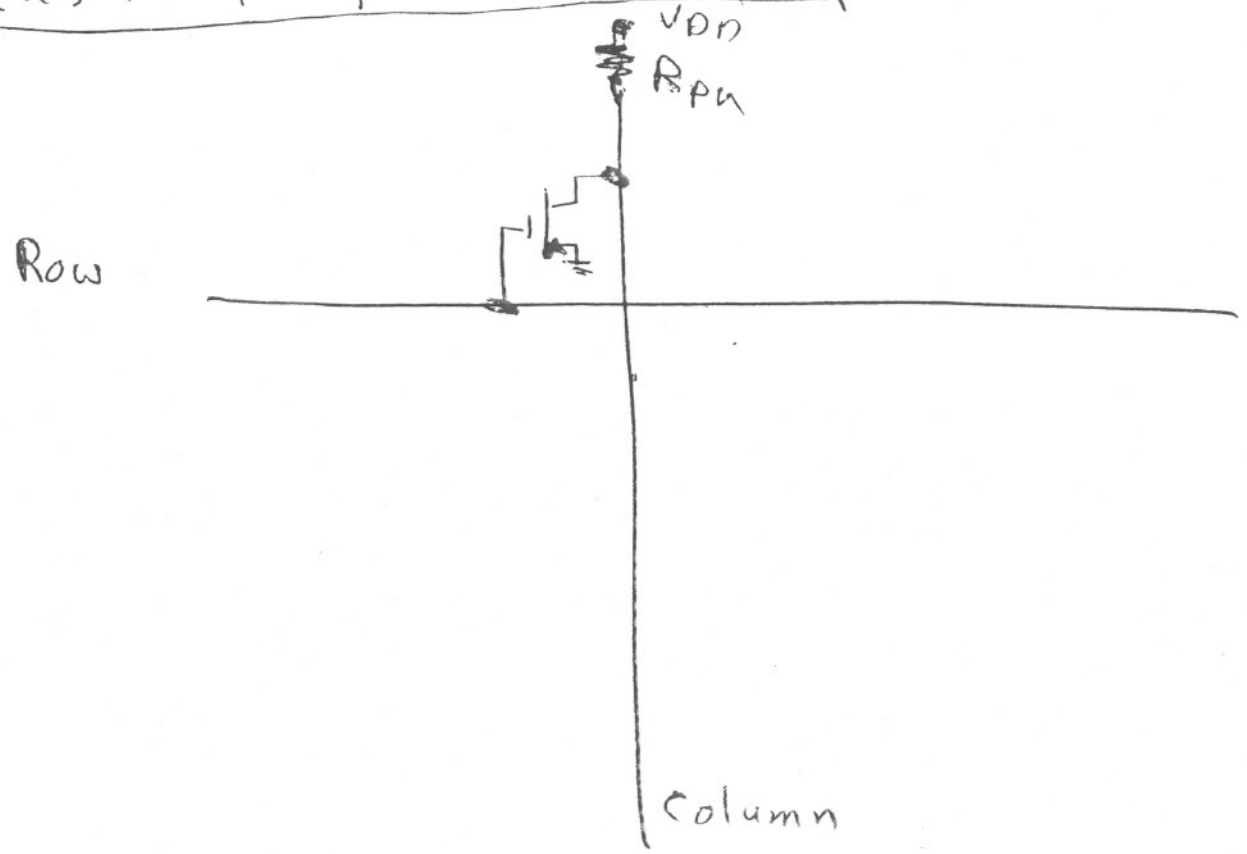


Sea of Gates Partitioning to Realize Array of Small Gates



- Simply need to add contacts to partition array
- Logic Implemented in same way as Gate Array
- May be less wasted sites since partitions can be used to create desired size of gates

Mask Programmable ROM



- single transistor for each bit ☺
- Read Only ☹
- transistor site present at <u>all</u> intersections

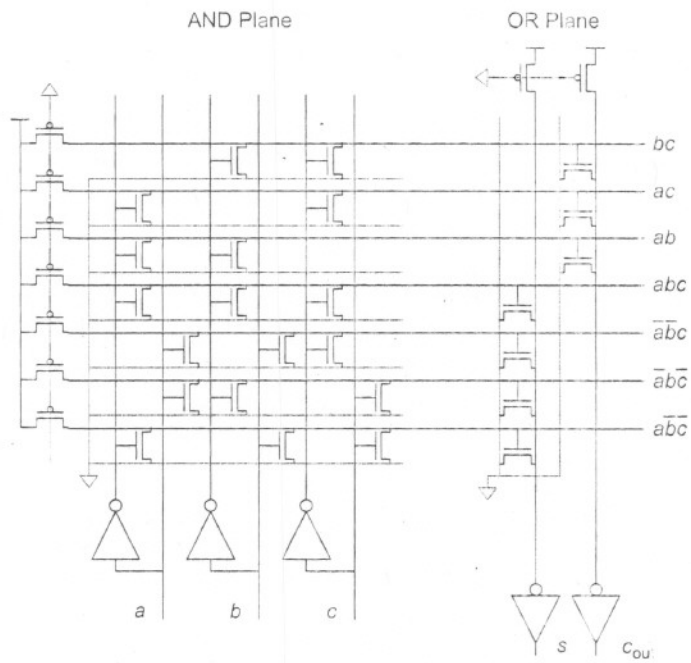


FIG 11.57 Pseudo-nMOS PLA schematic

To Read, take Row L high and presel column outputs to Sense amp.

- cap. on column lines is large and can cause cell contents to be over-written!
- To circumvent this problem, precharge column lines to V_{TRIP}

Field Programmable Gate Arrays

Major Players :

Xilinx
Altera } comparable in size

Actel — much smaller

- Some are one-time programmable
- Some can be repeatedly reprogrammed

Memory in FPGAs

1) SRAM / EPROM support or E^2PROM support

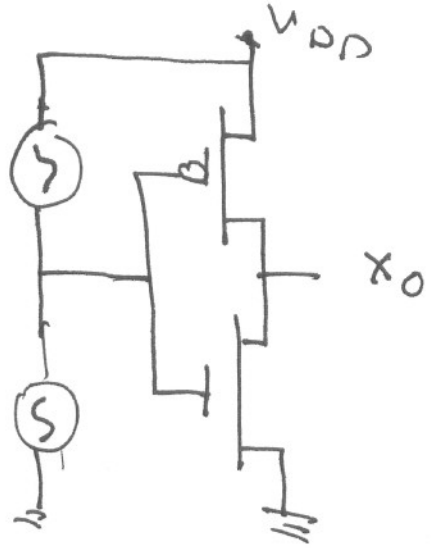
2) EPROM
or E^2PROM

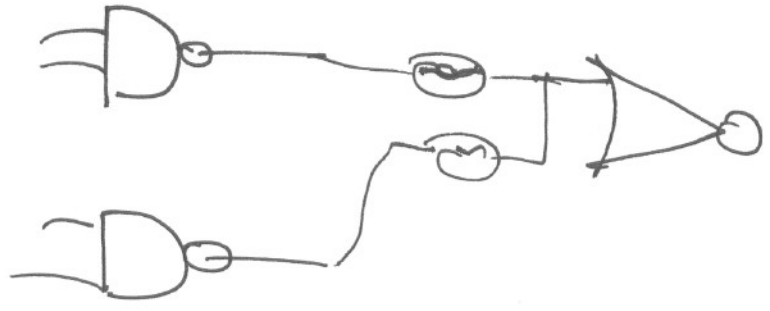
3) Anti-fuses

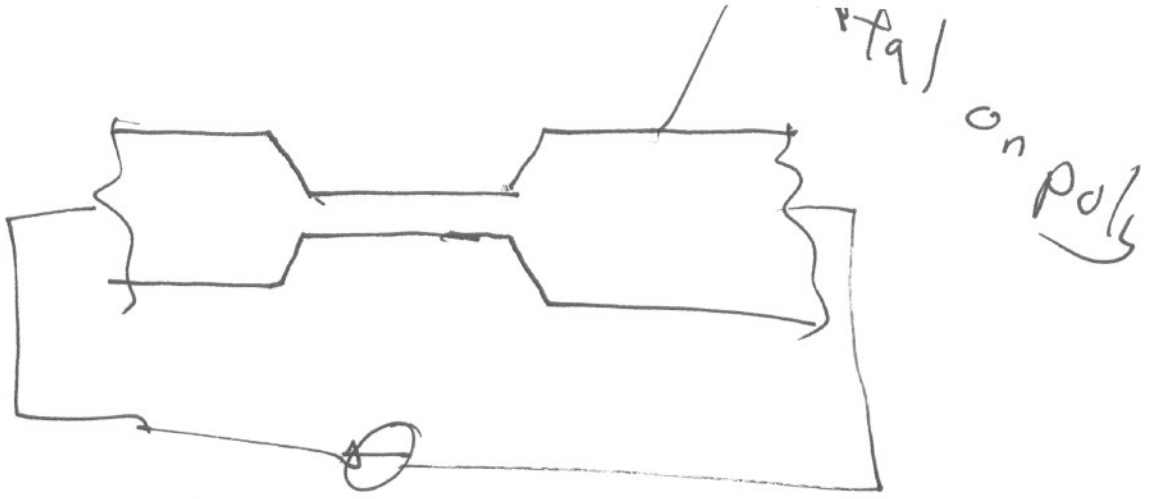
4) Fuses (Least Popular)

Must be able to interconnect "gates"
and program the gates

Fuse :







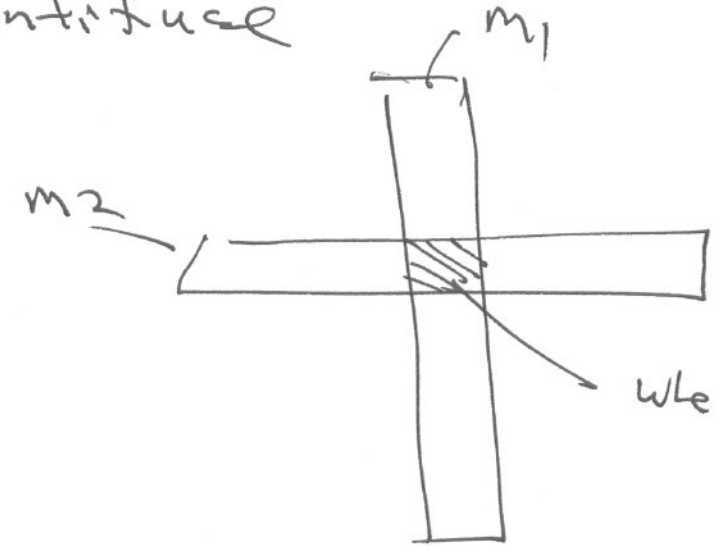
If transistors are used to route the current, how do we keep the transistors from burning out?

→ size width & interconnect appropriately

Limitations

1) Transistors for prog. current are too large
2) one-time use
3) damages material above & has regrowth

Antifuse



- widely used at Altera

Limitations

1) Single-tile programmable
2) Specialized processing step