

EE 434

Lecture 43

Sequential Logic

Most useful circuits include a combination of combinational & sequential logic blocks

Observation:

- Multiple-input NAND or NOR gates are sufficient to build any combinational logic function
- Any clocked flip flop or storage element will be sufficient to add the sequential logic functionality to any system.

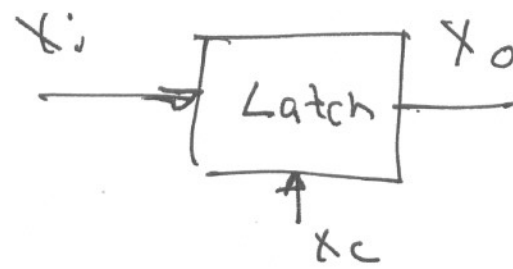
# Memory Circuits / Elements

1) Latch

2) Flip Flop

3) Memory Cell

Latches ;



Terminology

Transparency :

Input to Latch appears immediately on the latched output.

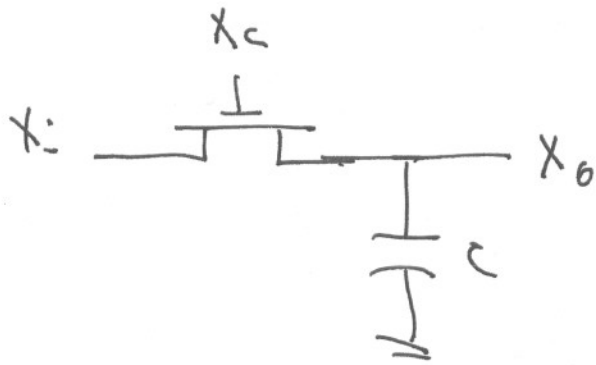
Opaque :

Input to the Latch does not appear at the output while in the Opaque State

Edge Triggered :

Input to the latch at a control transition determines when the input is transferred to the latch output

Example:



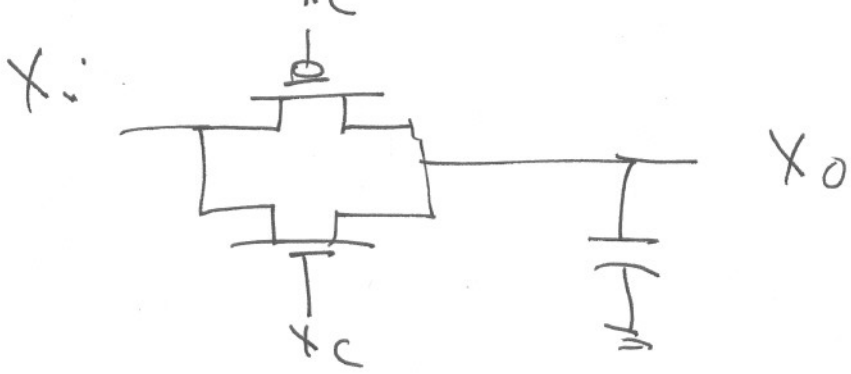
when  $X_c$  is high,  
output tracks input

when  $X_c$  is low,  
latch is opaque

- very simple
- negative edge triggered.

Limitations:

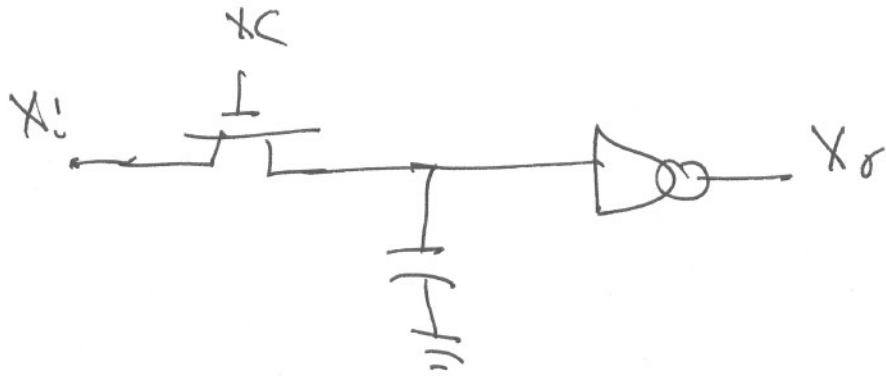
- $X_o$  can get no closer to  $V_{DD}$  than  $V_{TH}$
- leakage of charge will occur when  $X_c$  is low
- any loads placed on  $X_o$  will further degrade signal



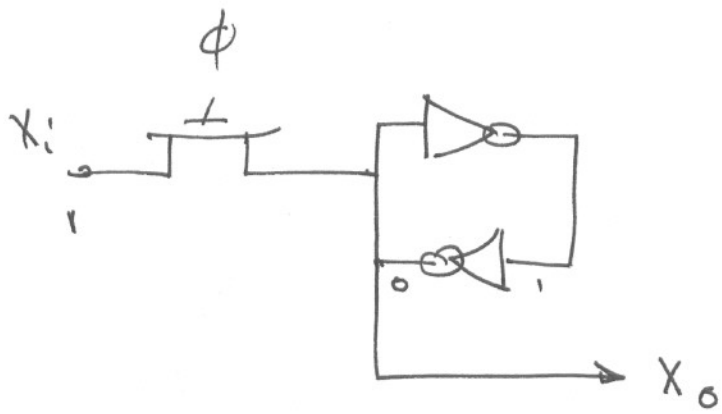
→ rail to rail output

→ leakage & loading problem

→ more complexity



→ removes loading problem

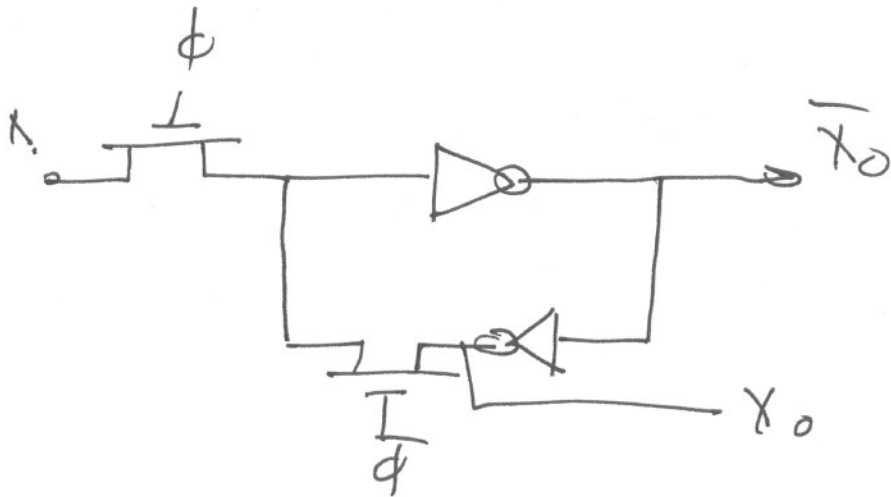


- removes the leakage problem.

- volatile

- load challenge

load transistor must be stronger than the FB inverter.



6-transistor solution ~

# Flip Flops

S-R

D

T

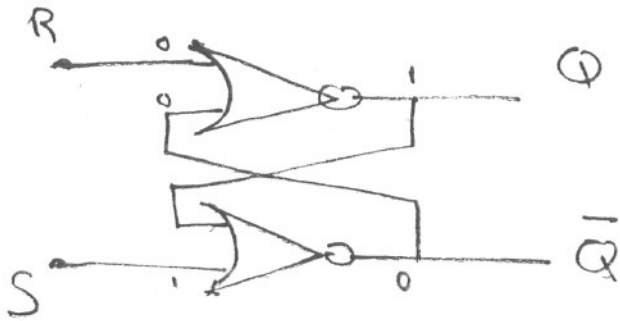
J-K



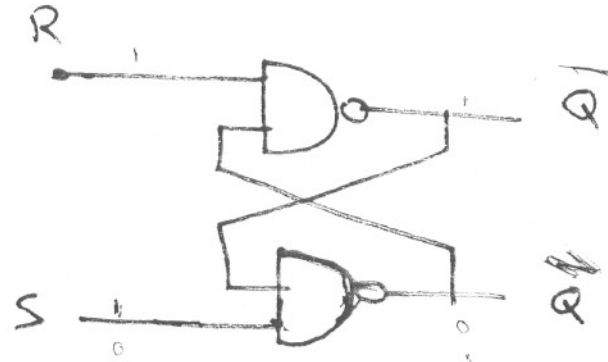
Master/Slave Version



# S-R flip flop



Two cross-coupled  
NOR gates



Two cross-coupled  
NAND gates

R & S can not be high at the same time

R & S can not be low at the same time

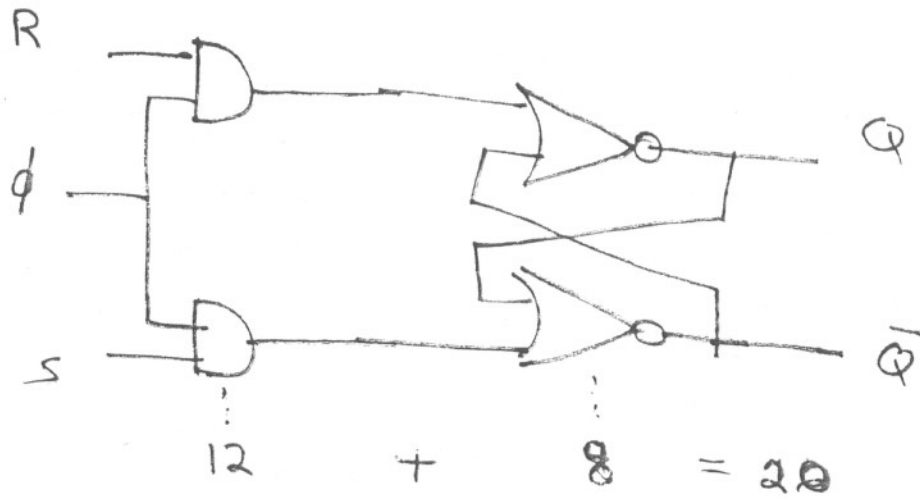
If they are ever both simultaneously

high, the state of the FF when

both go low will be indeterminate

1 level of logic }  
transistors } ☺

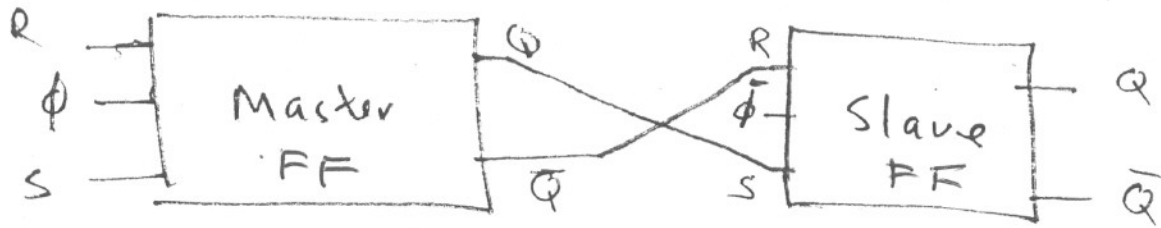
To obtain a clocked S-R flip flop



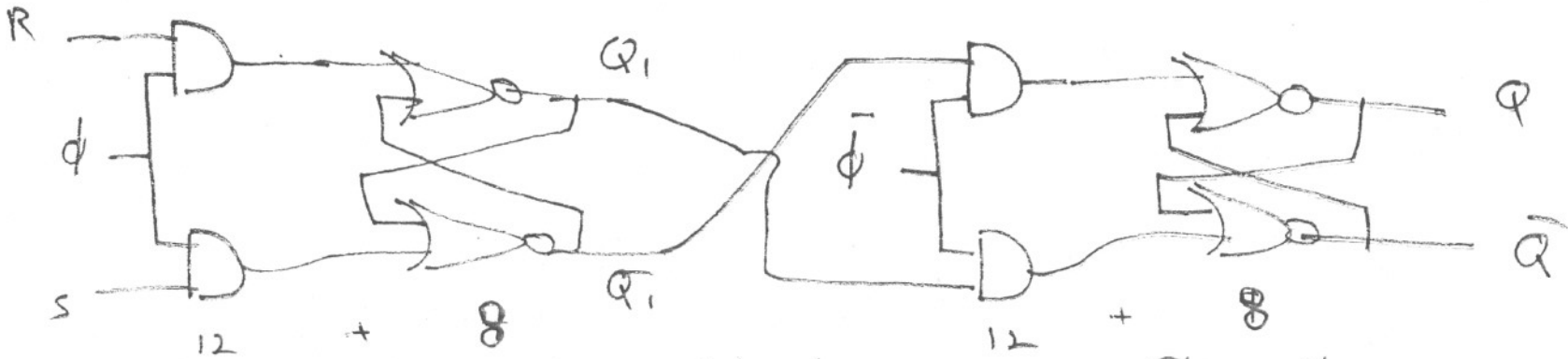
- output will not change when  $\phi$  is low
- Output is immediate when  $\phi$  is high

20 transistors  
3 levels of logic





Master Slave Flip Flop



Master-Slave Clocked S-R flip flop  
triggered on negative edge  $\phi$

40 transistors  
6 levels of logic



- output is not immediate on either  $\phi$  or  $\phi$
- avoid "shoot-through" when  $\phi$  goes from L to H by

or to sure  $\phi$  goes low before  $\phi$  high

