LE 434
Lecture 44

Sequential Logic Circuits

Memory Structures
Review from last time:

Master-Slave Flip Flop

Master-Slave Clocked S-R Flip Flop triggered on negative edge $\phi$

<table>
<thead>
<tr>
<th>40 transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 levels of logic</td>
</tr>
</tbody>
</table>

Transistor count is High!
Levels of logic is High!
Clocked S-R Flip Flop with Pass Transistor Logic

for MS Flip flop

<table>
<thead>
<tr>
<th>4 levels of logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 transistors</td>
</tr>
</tbody>
</table>

- Uses Pass Transistor Logic for input control
- Substantial reduction in device count for edge-triggered MS S-R flip flop
- Still several levels of logic and quite a few transistors
D flip flop (clocked, edge-triggered M/S)

Positive edge sampled

12 transistors
6 levels of logic

Note: multiple logic styles, significant reduction in device count!
Dynamic Shift Register

Bit Cell Boundary
- 6 transistor SR
- "Dynamic"
- Complimentary nonoverlap clock

Question: How are SR & TR generated?
Modification of SR for Static Hold
Bidirectional Dynamic SR

- If TL and TR were both high.
  SL and SR were both low.

- Then the data in the SR can be held as long as power is available.

- Can be used as a Stack.
Slight modifications of this SR provides:

a) Bidirectional shifting
b) Serial to Parallel Conversion
c) Parallel to Serial Conversion
d) Static Hold
Modified Shift Register

- Parallel to Serial Conversion and Serial to
  - Parallel Conversion controlled with X
- Low Device Count
- can be put in static hold state
Typical Memory Structure

Row Decoder

Addres

Sense Amp

Column Decoder

MEM Cell

Memory Array
- Memory Array often Square irrespective of the number of output bits desired

- Same basic concept used for various memory types

- Pseudo NMOS often used for row and column decoders

- Sense amp improves speed for saturating MEM cells and is essential for non-saturating MEM cells

- Pre-charge of columns often used to improve speed and reduce problems of over-writing data stored in MEM cells
To write, put data on Ck & \overline{Ck} and take RowL high.

If data to be written differs from what is in memory, contention will exist on Ck & \overline{Ck}.
Must size OD or Ck & \overline{Ck} to have them dominate.