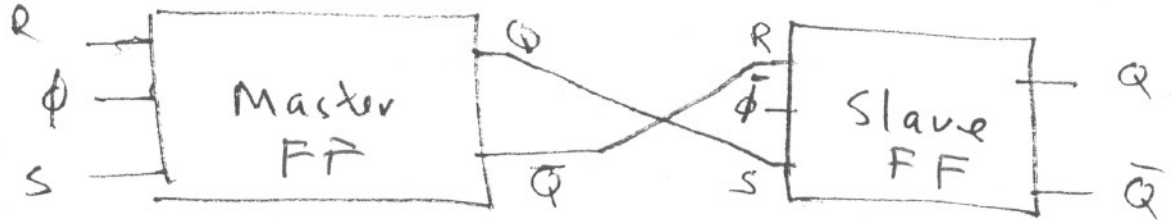
EE 434

Lecture 44

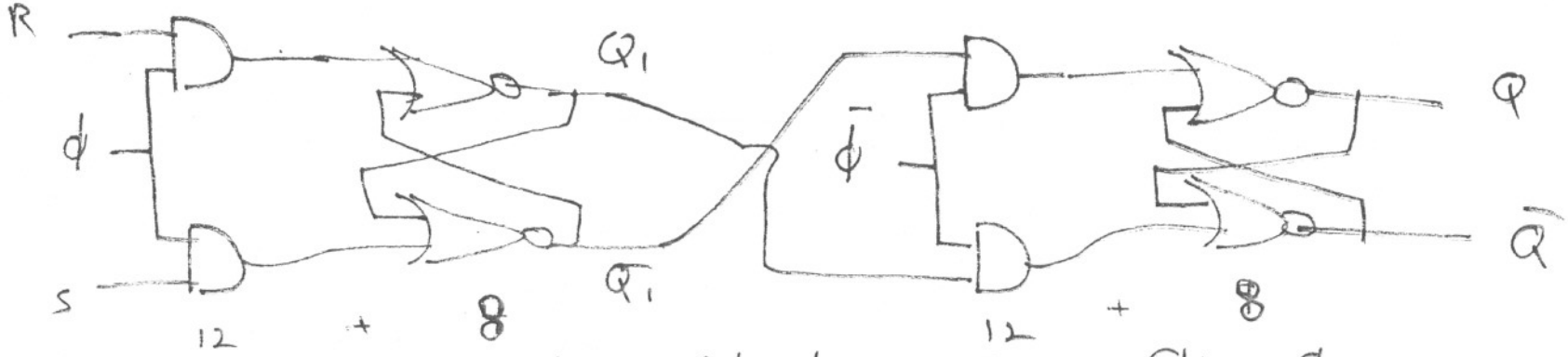
Sequential Logic Circuits

Memory Structures

Review from last time



Master Slave Flip Flop

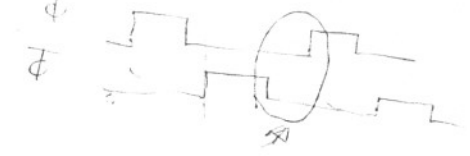


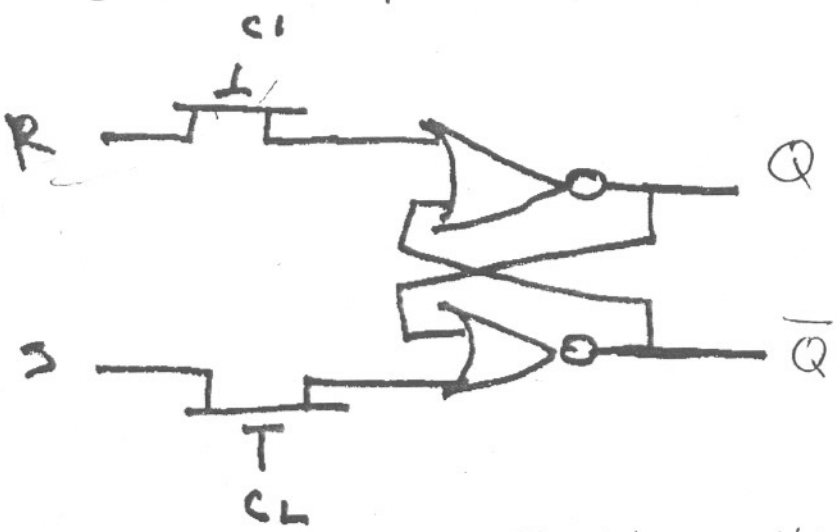
Master-Slave Clocked S-R flip flop
triggered on negative edge ϕ

40	transistors
6	levels of logic

Transistor count is High!
Levels of Logic is High!

- output is not immediate on either ϕ or $\bar{\phi}$
- avoid shoot-through when $\bar{\phi}$ goes from LOW by





2 levels of Logic
10 transistors

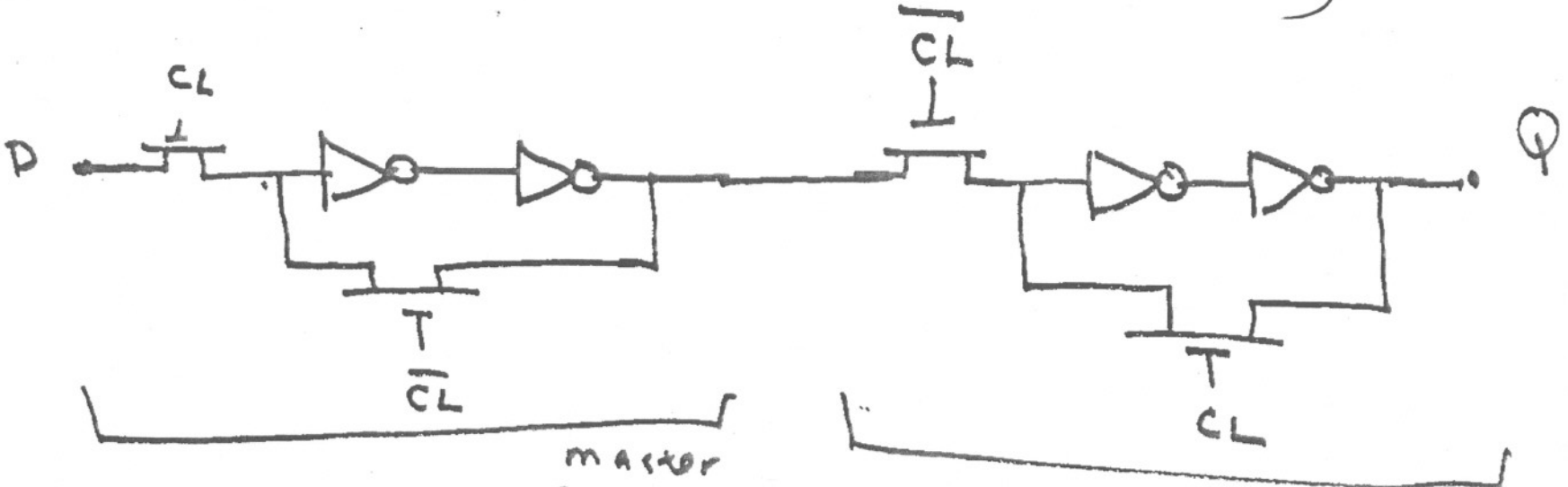
Clocked S-R Flip Flop with Pass Transistor Logic

for MS flip flop

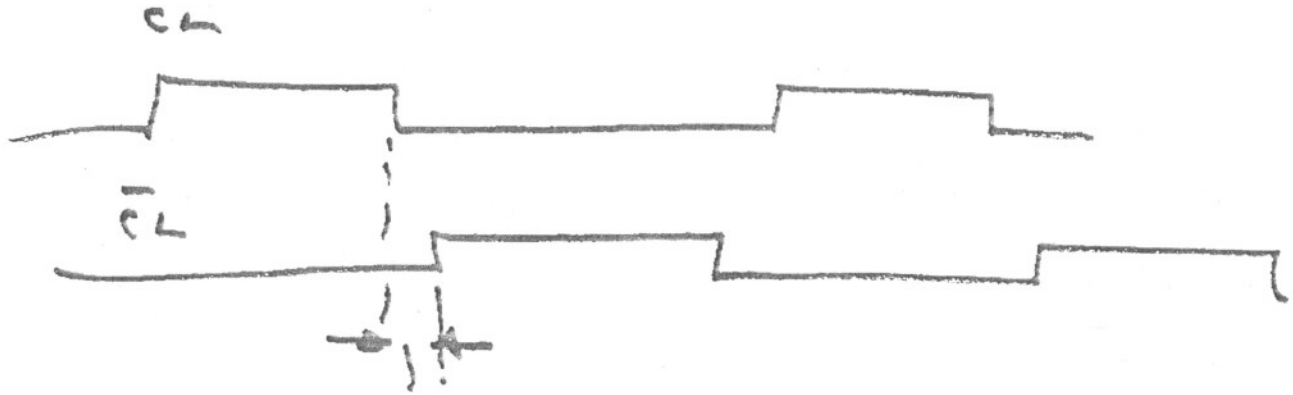
4 levels of logic
20 transistors

- Uses Pass Transistor Logic for input control
- Substantial reduction in device count for edge-triggered MS S-R flip flop
- Still several levels of logic and quite a few transistors.

D flip flop (clocked, edge-triggered M/S)



Negative edge sampled



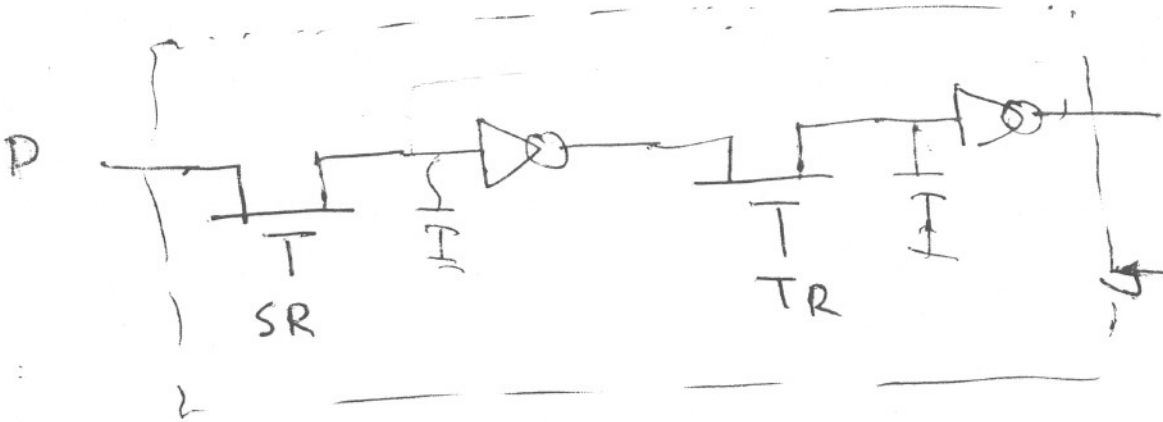
12 transistors

6 levels of logic

Note: - multiple logic styles

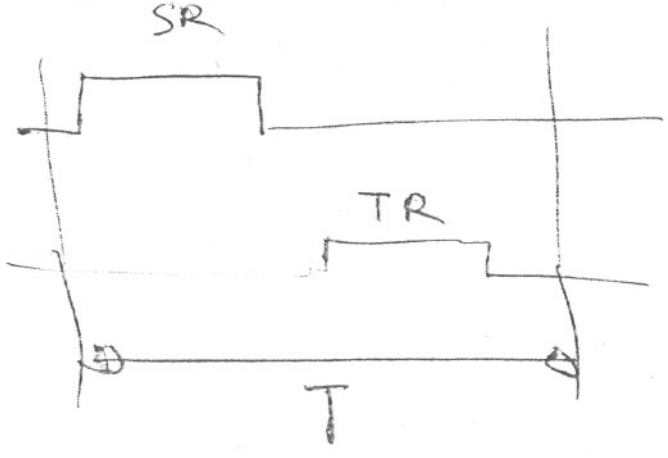
- significant reduction in device count!

Dynamic Shift Register



Bit Cell Boundary

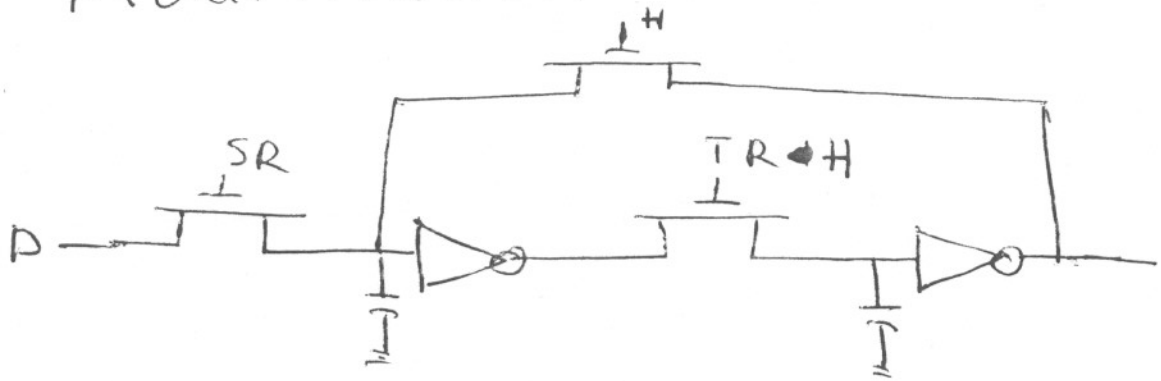
- 6 transistor SR



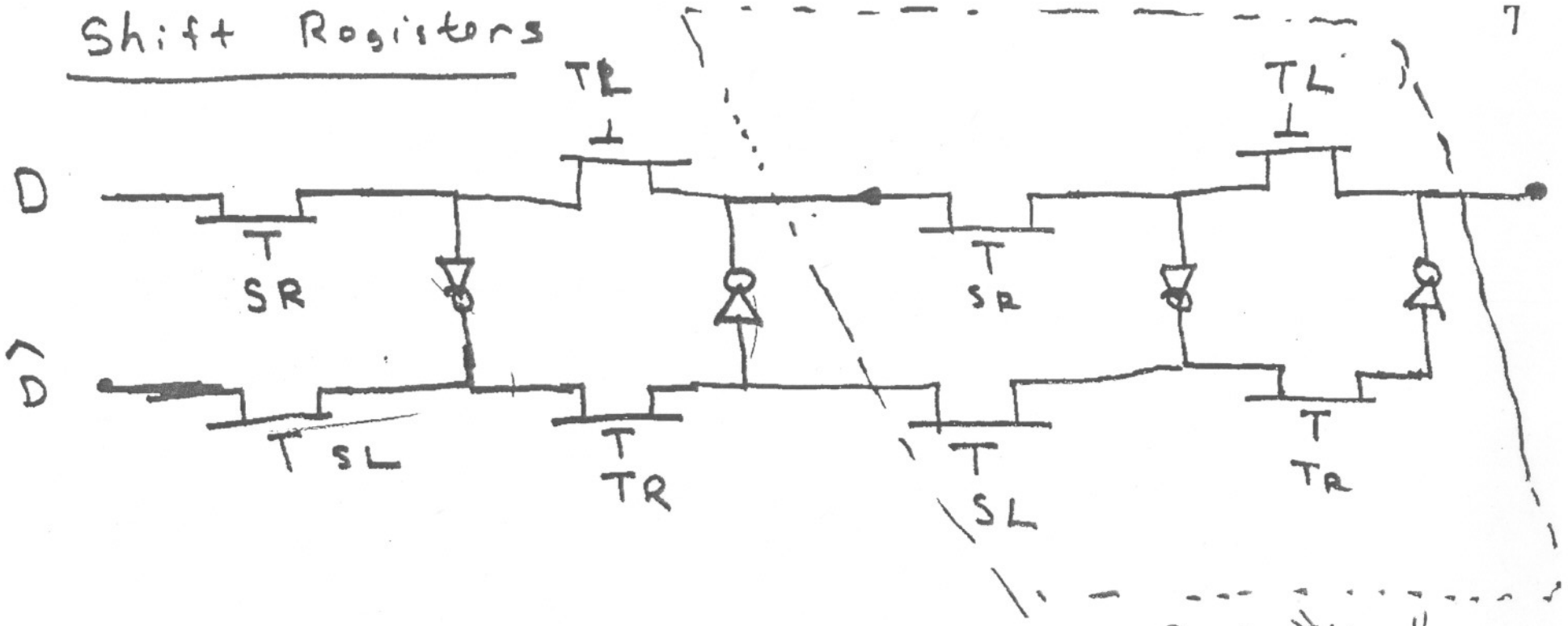
- "Dynamic"
- Complimentary nonoverlap clock

Question: How are SR & TR generated.
from Student

Modification of SR for Static Hold



Shift Registers



Basic "Slice" of SR

Bidirectional Dynamic SR

- If TL & TR were both high
  SL & SR were both low
- Then the data in the SR can be held as long as power is available.
- Can be used as a stack

Slight modifications of this SR provides

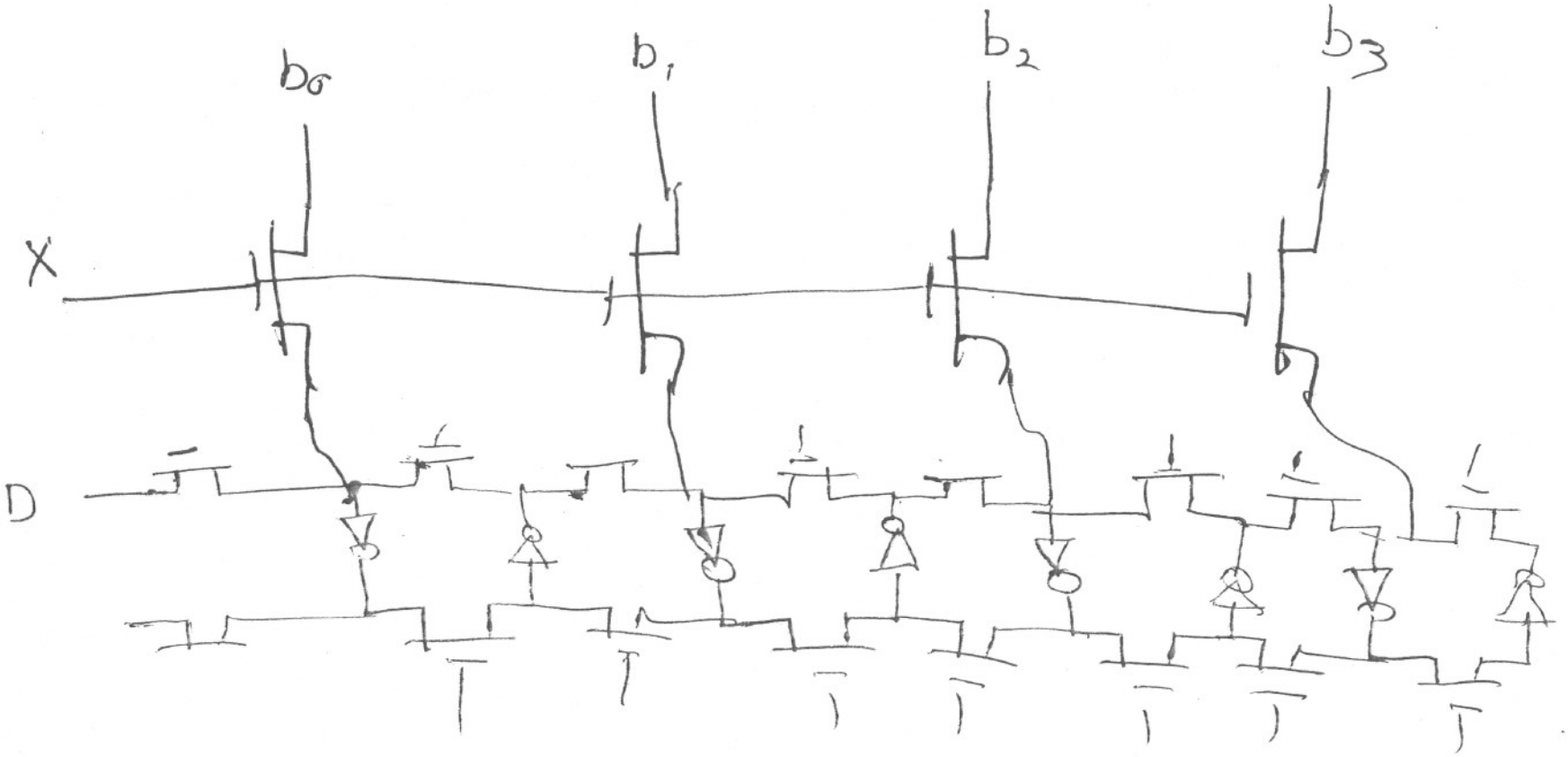
a) Bidirectional shifting

b) Serial to Parallel conversion

c) Parallel to Serial conversion

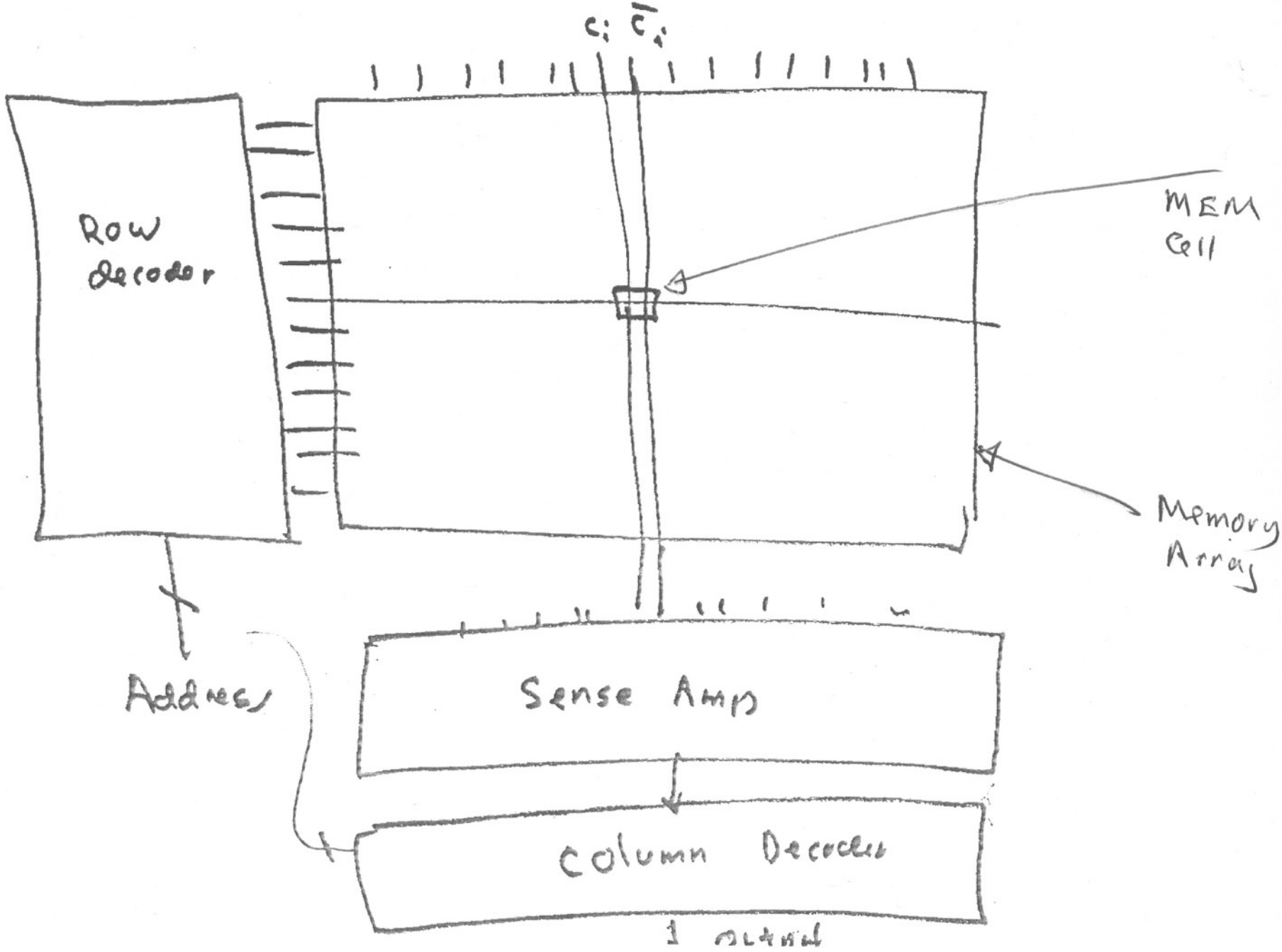
d) Static Hold

Modified Shift Register

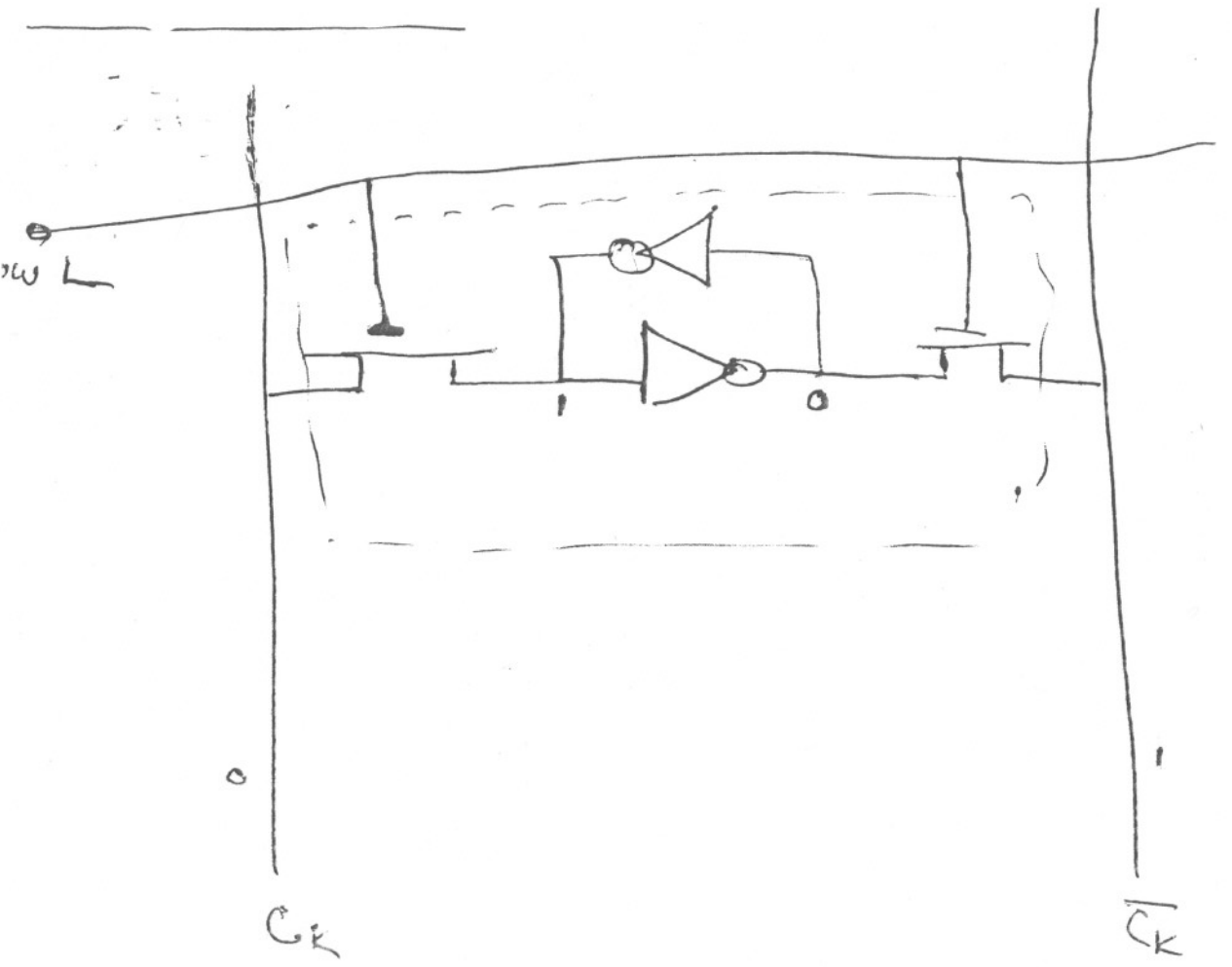


- Parallel to Serial Conversion and Serial to Parallel Conversion controlled with X
- Low Device Count
- can be put in static hold State

Typical Memory Structure



- Memory Array often Square irrespective of the number of output bits desired
- Same basic concept used for various memory types
- Pseudo NMOS often used for row and column decoders
- Sense amp improves speed for saturating MEM cells and is essential for non-saturating MEM cells
- Pre-charge of columns often used to improve speed and ~~di~~ reduce problems of over-writing data stored in MEM cells



6 - transistors

To write, put data on C_K & $\overline{C_K}$ and take Row L high

If data to be written differs from what is in memory, contention will exist on C_K & $\overline{C_K}$ must size OD of C_K & $\overline{C_K}$ to have them dominate