CHAPTER
5

BASIC INTEGRATED CIRCUIT BUILDING BLOCKS

5.0 INTRODUCTION

This chapter introduces various integrated circuit building blocks, which form the first step in integrated circuit design. Figures 5.0-1 and 5.0-2 illustrate the circuit diagrams of a BJT op amp and a CMOS op amp. Although such circuits will not be covered until Chapter 6, they are useful in illustrating how the various building blocks are combined to form more complex circuits. There are two important observations to make concerning these two figures. The first is that circuit design is remarkably similar for different technologies. The architecture of both op amps is identical although the performance may not be identical. This fact will permit circuit design ideas developed in one technology to be applicable to a new technology. The second observation is that some components in each op amp perform more than one function. For example, Q3 (M3) serves as an active resistor load but also serves as part of a current mirror. This characteristic of circuits makes it difficult to distinguish the function of a component in a circuit.

In this chapter, some of the building blocks of Figs. 5.0-1 and 5.0-2 will be discussed. These blocks include switches (not shown on Figs. 5.0-1 or 5.0-2), active resistors, current sinks and sources, current mirrors, and voltage and current references. These blocks, along with passive resistors and capacitors, will form the lowest level of the design hierarchy. The next level of hierarchy takes the blocks of this chapter and implements more complex circuits such as amplifiers or comparators. Chapters 6 and 7 address analog and digital circuits, respectively, implemented from the building blocks of this chapter. Chapters 8 and 9 address
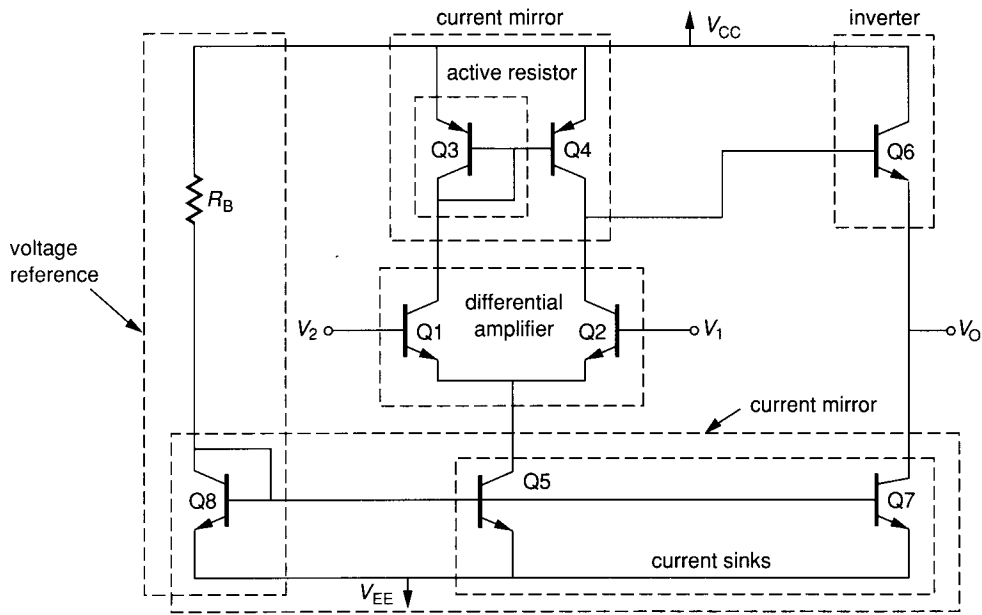
FIGURE 5.0-1
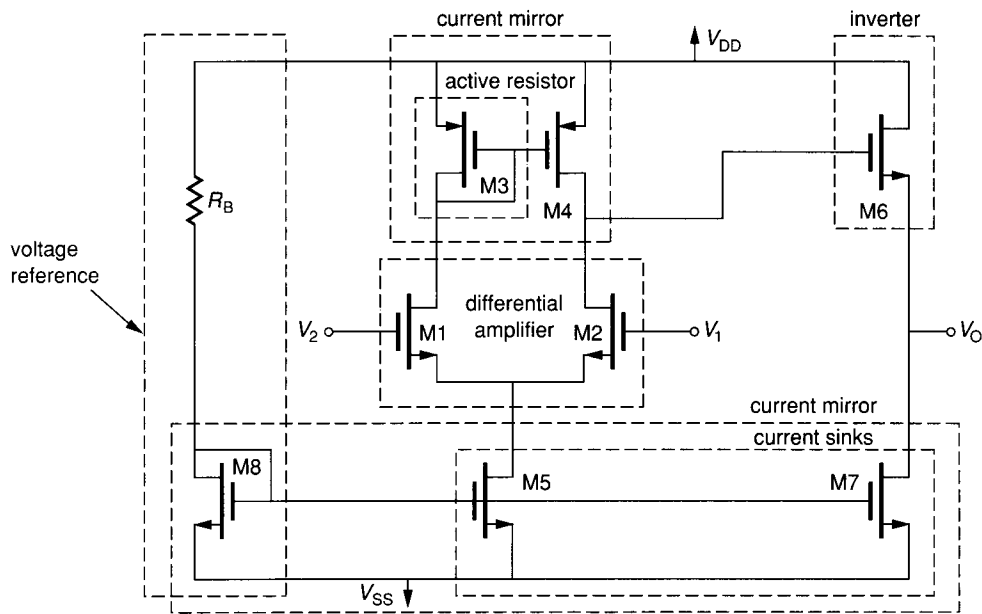BJT op amp illustrating the various components.

FIGURE 5.0-2
CMOS op amp illustrating the various components.

TABLE 5.0-1
Design hierarchy of Chapters 5 through 9

Design hierarchy	Analog design	Digital design
Systems	Chapter 8	Chapter 9
Basic circuits	Chapter 6	Chapter 7
Building blocks	Chapter 5	—

the use of these analog and digital circuits to perform analog and digital signal processing functions, respectively. The hierarchical relationships of this material are illustrated in Table 5.0-1.

Throughout this chapter, several key concepts are introduced. These concepts include both techniques and principles. How to use both positive and negative feedback in order to improve some aspect of the performance of the building blocks will be shown. The important principle of matched devices that is key to integrated circuit design will be presented and illustrated. Techniques such as how to make a mismatch analysis or how to attain the zero sensitivity of a circuit to some parameter will be described. These principles and techniques should be understood by the reader since they are invariant and applicable regardless of the technology. The summary will include a review of these important principles and techniques.

5.1 SWITCHES

Although the switch is not one of the components illustrated in Fig. 5.0-1 or Fig. 5.0-2, it will be considered first because of its simplicity and importance. The switch finds many applications in integrated circuit design. In analog circuits, the switch is used to implement such useful functions as the switched simulation of a resistor in Sec. 5.2. The switch is also useful for multiplexing, modulation, autozeroing and a number of other applications. The switch is used as a transmission gate in digital circuits and adds a dimension of flexibility not found in standard logic circuits. The objective of this section is to study the characteristics of switches that are compatible with integrated circuits.

Figure 5.1-1a illustrates a model of the ideal voltage-controlled switch. Terminals A and B represent the switch terminals, and terminal C is the controlling terminal. Ideally, the voltage at V_C has two states. In one state, the switch is open (off) and in the other state the switch is closed (on). In the on state, the ideal switch presents a short circuit between terminals A and B. In the off state, the ideal switch presents an open circuit between terminals A and B.

Unfortunately, practical switch implementations only approximate the model given in Fig. 5.1-1a. Figure 5.1-1b is a model of the switch that includes some of the more important nonideal characteristics. R_{ON} is a resistance that represents the small but finite resistance between terminals A and B when the switch is on. R_{OFF} represents the large but not infinite resistance between terminals A and B when the switch is off. In many applications it will be desirable to have R_{ON} as small as possible and R_{OFF} as large as possible.
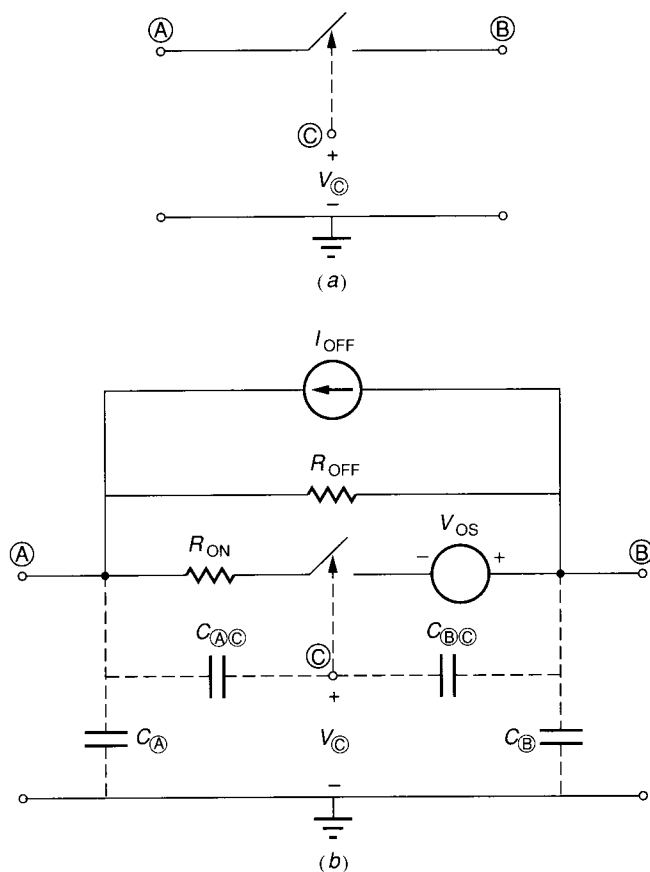
FIGURE 5.1-1
Models of the switch: (a) Ideal, (b) Nonideal.

Another practical characteristic of the switch is given by V_{OS} and I_{OFF} shown in Fig. 5.1-1b. The voltage that exists between terminals Ⓐ and Ⓑ when the switch is on but the current through it is zero is approximately the offset voltage and is modeled by an independent voltage source of V_{OS}. Similarly, the current that flows between terminals Ⓐ and Ⓑ when the switch is off but the voltage across the switch terminals is zero is approximately the offset current and is modeled by an independent current source of I_{OFF}. The polarities of the offset current and voltage are not known and have arbitrarily been assigned in Fig. 5.1-1b.

Figure 5.1-1b also shows some of the parasitic capacitances that exist between the various switch terminals and to ground. $C_{ⒶⒸ}$ and $C_{ⒷⒸ}$ will be particularly important when considering the influence of the controlling voltage on the switch performance. There are many other nonideal characteristics of the switch such as linearity, commutation time, noise, etc. that are not modeled by Fig. 5.1-1b.

The graphical characterization of a switch shown in Fig. 5.1-2 is useful in determining how well the switch can be implemented by a bipolar or MOS
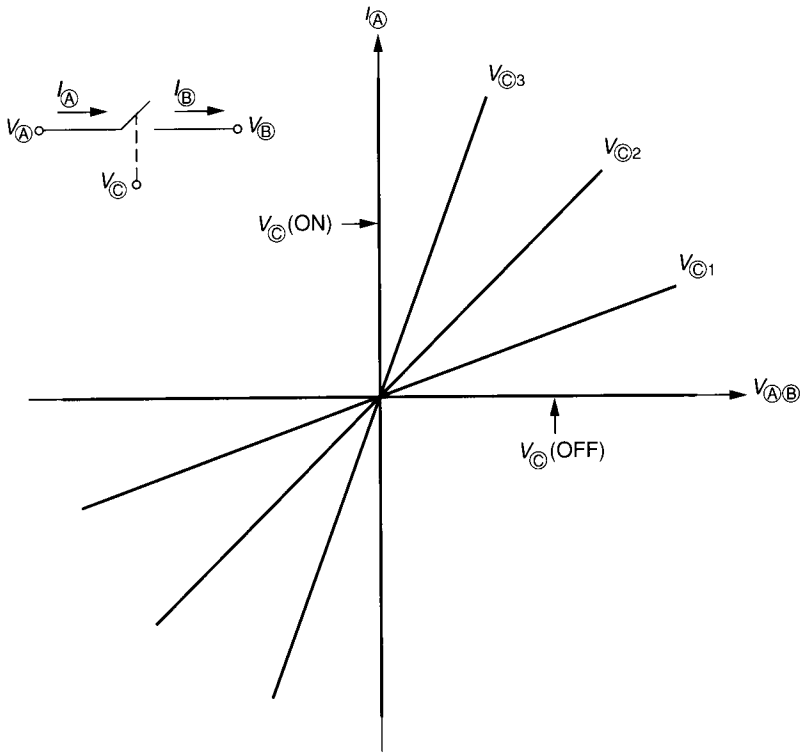
FIGURE 5.1-2
Graphical characteristics of a controlled switch.

transistor. $V_{\textcircled{A}\textcircled{B}} = V_{\textcircled{A}} - V_{\textcircled{B}}$ is the voltage across the switch, and $I_{\textcircled{A}}$ is the current into the terminal $\textcircled{A}$ and $I_{\textcircled{B}}$ the current out of terminal $\textcircled{B}$ of the switch. When $V_{\textcircled{C}} = V_{\textcircled{C}}(ON)$, ideally $V_{\textcircled{A}\textcircled{B}} = 0$ and $I_{\textcircled{A}}(I_{\textcircled{B}})$ can have any value. In the on state, the ideal switch is a short circuit. When $V_{\textcircled{C}} = V_{\textcircled{C}}$ (OFF), $I_{\textcircled{A}} = I_{\textcircled{B}} = 0$ and $V_{\textcircled{A}\textcircled{B}}$ can have any value and is identical to an open circuit. $V_{\textcircled{C}1}$, $V_{\textcircled{C}2}$, and $V_{\textcircled{C}3}$ are values of $V_{\textcircled{C}}$ that cause the switch to be between its on and off states. Normally $V_{\textcircled{C}}(OFF) < V_{\textcircled{C}1} < V_{\textcircled{C}2} < V_{\textcircled{C}3} < V_{\textcircled{C}}$ (ON).

Now consider the bipolar transistor as an implementation of the switch as shown in Fig. 5.1-3a, where $V_{\textcircled{A}\textcircled{B}} = V_{CE}$, $I_{\textcircled{A}} = I_C$, and $V_{\textcircled{C}} = V_B$. The right-hand side of these equalities refers to the transistor, whereas the left-hand side refers to the switch in Fig. 5.1-1 or 5.1-2. Typical BJT characteristics are shown in Fig. 5.1-3b with $V_{\textcircled{B}} = 0(V_E = 0)$. Several shortcomings of the BJT switch realization are immediately apparent in Fig. 5.1-3b. The first is that the origin of the characteristics for $I_{\textcircled{A}} = 0$ is not zero. Thus V_{OS} of Fig. 5.1-1 is approximately 16 mV. The second is the nonlinearity of the various curves for a constant $V_{\textcircled{C}}$. This would severely limit the dynamic range of the switch. Lastly, the switch characteristics are not symmetrical in the first and third quadrants. Another problem, which is not apparent from Fig. 5.1-3b, is that the BJT requires
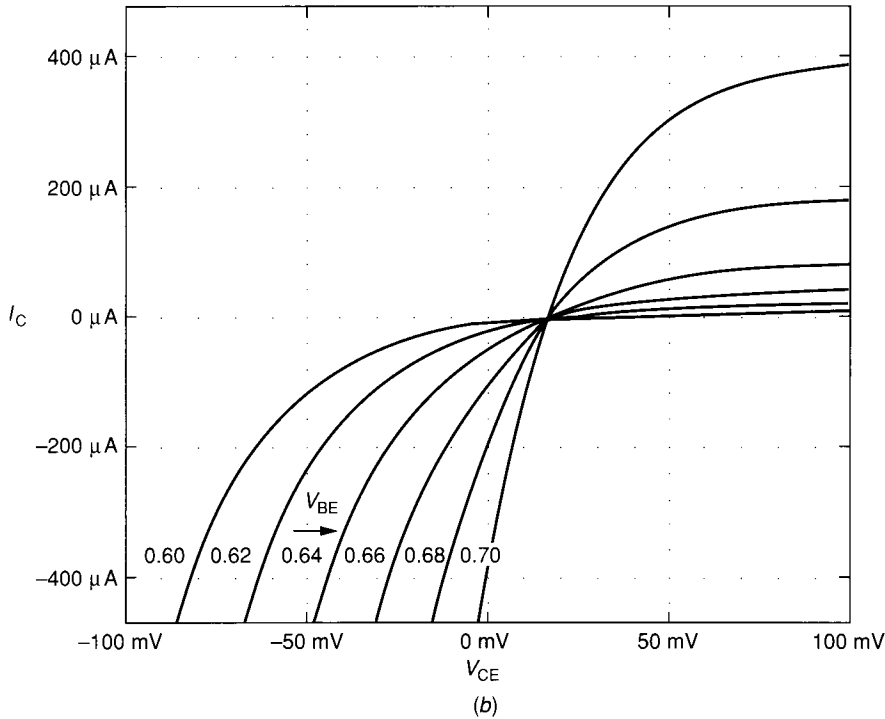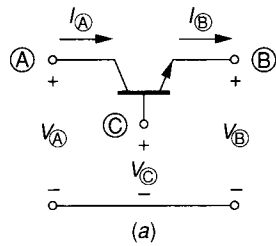
FIGURE 5.1-3

(a) Bipolar transistor as a switch, (b) Graphical characteristics of a where $V_{\text{(A)(B)}} = V_{\text{CE}}$, $I_{\text{(A)}} = I_{\text{C}}$, and $V_{\text{(C)}} = V_{\text{B}}$. Note that $V_{\text{E}} = 0$.

a small current flowing in the controlling terminal, causing the current flowing in terminal A to be different from that flowing out of terminal B.

Figure 5.1-4b shows the graphical characteristics of the MOS transistor of Fig. 5.1-4a, where $V_{\text{(A)(B)}} = V_{\text{DS}}$, $I_{\text{(A)}} = I_{\text{D}}$, and $V_{\text{(C)}} = V_{\text{G}}$. Again, the right-hand side of these inequalities refers to the MOS transistor while the left-hand side refers to the switch in Fig. 5.1-1 or 5.1-2. Comparison of Figs. 5.1-2, 5.1-3b, and 5.1-4b strongly suggests that the MOS transistor is a much better switch realization.

Figure 5.1-5 shows a MOS transistor that will be used as a switch. It will be important to consider the influence of the bulk voltage on the switch operation. The performance of this realization can be determined by comparing
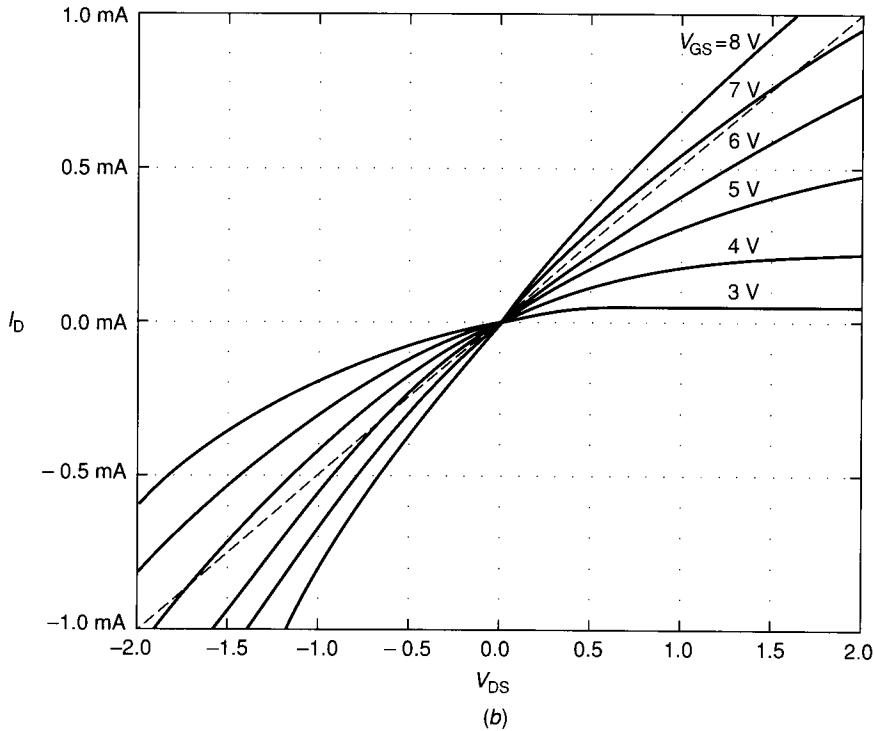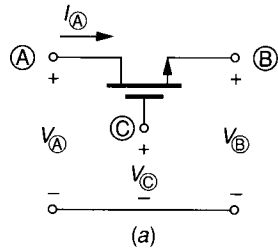
(a)

(b)

FIGURE 5.1-4

(a) MOS transistor as a switch, (b) Graphical characteristics of a where $V_{\text{Ⓐ}\text{Ⓑ}} = V_{\text{DS}}$, $I_{\text{Ⓐ}} = I_{\text{D}}$, and $V_{\text{C}} = V_{\text{G}}$. Note that $V_{\text{S}} = 0$.

Fig. 5.1-1b with the large signal model for the MOS transistor. We see that terminals Ⓐ or Ⓑ can either be the drain or source of the MOS transistor. The on resistance is seen to consist of the series combination of R_{D}, R_{S}, and whatever channel resistance exists. An expression for the on channel resistance can be found as follows. In the on state of the switch, the voltage across the switch should be small, and V_{GS} should be large. Therefore, the MOS device is assumed to be in the ohmic region. Furthermore, let us assume that the channel length modulation effects can be ignored. From Sec. 3.1, the drain current is given by

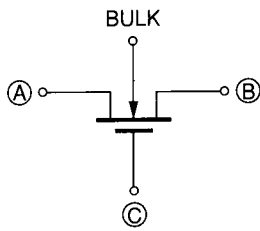$$I_{\text{D}} = \frac{K'W}{2L}[2(V_{\text{GS}} - V_{\text{T}})V_{\text{DS}} - V_{\text{DS}}^2] \qquad (5.1\text{-}1)$$

BULK

Ⓐ o——[ ]——o Ⓑ

Ⓒ

FIGURE 5.1-5
MOS transistor used as a switch.

if V_{DS} is less than $V_{GS} - V_T$ but greater than zero. (V_{GS} becomes V_{GD} if V_{DS} is negative.) Assuming that there is no offset voltage, the large signal channel resistance when $V_{GS} > V_T$ is

$$R_{ON} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{(K'W/L)(V_{GS} - V_T - V_{DS})} \qquad (5.1\text{-}2)$$

Figure 5.1-6 illustrates Eq. 5.1-2 for very small values of V_{DS}. When $V_{GS} < V_T$ and $V_{DS} = 0$, R_{ON} is infinite. For large V_{DS}, the curves of Fig. 5.1-6 will start to decrease in slope (see Fig. 3.1-2) for increasing V_{DS}. A plot of R_{ON} as a function of V_{GS}/V_T is shown in Fig. 5.1-7 for small V_{DS} using the parameters indicated for various values of W/L. A lower value of R_{ON} is achieved for larger values of W/L.

When the switch is off, V_{GS} is less than or equal to V_T and the transistor is always in the cutoff region. R_{OFF} is ideally infinite. A typical value is in the range of 10^{12} Ω. Because of this large value, the leakage current from drain and source to substrate is a more important parameter than R_{OFF}. This leakage current is a combination of the subthreshold current, the surface leakage current, and the package leakage current. Typically this leakage current is in the 10 pA range at room temperature and doubles for every 10°C increase. The resistances
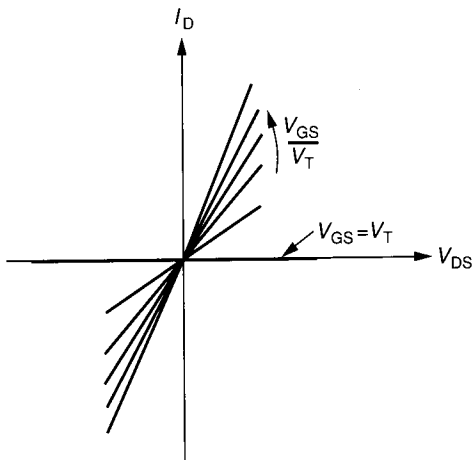
I_D

$\frac{V_{GS}}{V_T}$

$V_{GS} = V_T$

V_{DS}

FIGURE 5.1-6
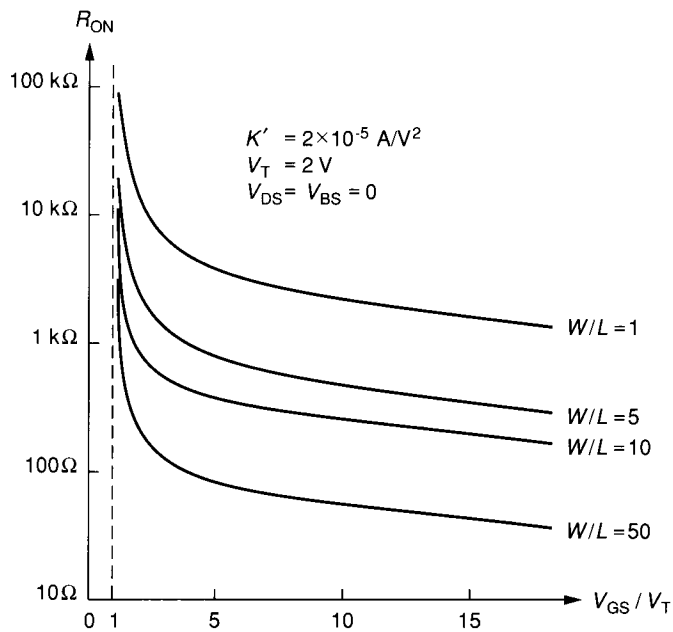Illustration of the on state of a switch. V_{GS}/V_T is increasing in equal increments.

FIGURE 5.1-7

Illustration of the R_{ON} characteristics of an MOS transistor with W/L as a parameter.

representing this leakage current are called $R_{\textcircled{A}}$ and $R_{\textcircled{B}}$ and are connected from $\textcircled{A}$ and $\textcircled{B}$ to ground in Fig. 5.1-1 and are on the order of 10^{10} Ω. Unfortunately, $R_{\textcircled{A}}$ and $R_{\textcircled{B}}$ prevent the designer from achieving R_{OFF} of 10^{12} Ω.

The offset voltage of the MOS device is zero and does not influence the switch performance. The capacitors C_A, C_B, C_{AC}, and C_{BC} of Fig. 5.1-1b correspond directly to the capacitors C_{BD}, C_{BS}, C_{GD}, and C_{GS} of the MOS transistor of Fig. 5.1-4a. The maximum commutation rate of the MOS switch is determined primarily by the capacitors of Fig. 5.1-1b and the external resistances. Commutation rates for CMOS switches of 20 MHz are typical depending upon the load capacitance.

One important aspect of the switch is the range of voltages on the switch terminals compared to the control voltage. In the n-channel MOS transistor we see that the gate voltage must be considerably larger than either the drain or source voltage to insure that the MOS transistor is on. Typically the bulk is taken to the most negative potential for the n-channel MOS switch. The problem can be illustrated as follows. Suppose that the on voltage of the gate is the positive power supply V_{DD}. With the bulk connected to ground this should keep the MOS switch on until the signal on the switch terminals (which should be approximately identical at the source and drain) approaches $V_{DD} - V_T$. As the signal approaches $V_{DD} - V_T$, the switch begins to turn off. This often introduces an undesired nonlinear distortion in the transmission of analog signals. Typical voltages used for an n-channel MOS switch are shown in Fig. 5.1-8, where the switch is connected between two circuits and the power supplies are ± 5 V.
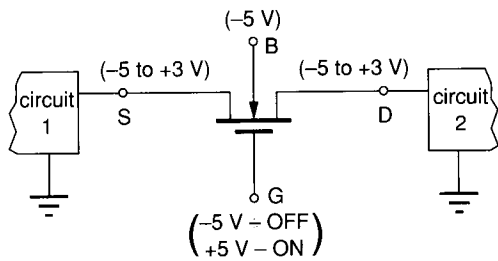
FIGURE 5.1-8
Application of an n-channel MOS transistor as a switch with typical terminal voltages indicated.

To illustrate the influence of the switches on the circuit, consider the use of a switch to charge an integrated capacitor, as shown in Fig. 5.1-9. M1 is a MOS transistor used as a switch, and ϕ_1 is called the clock. The on resistance of the switches can become important during the charge transfer phase of this circuit. For example, when ϕ_1 goes high, M1 connects C_1 to the voltage source V_{in}. The equivalent circuit at this time is shown in Fig. 5.1-10. It is seen that C_1 will charge to V_{in} with the time constant of $R_{ON}C_1$. For successful operation $R_{ON}C_1 \ll T$, where T is the time ϕ_1 is high. The value of R_{ON} is not constant during the charging of C_1 because the value of V_{GS} decreases as the capacitor charges. The assumption that R_{ON} is constant avoids the solution of nonlinear differential equations necessary for the exact solution.

The maximum acceptable value of R_{ON} will determine required values for W and L of M1. Typical values of C_1 are less than 20 pF because the area required to implement larger capacitors would be too large to be practical. If the time ϕ_1 is high is $T = 10 \,\mu s$ and $C_1 = 20$ pF, then R_{ON} must be less than 0.5 MΩ. Since small capacitors are used, switches with a large R_{ON} can still perform satisfactorily. As a result, the MOS devices used for switching typically use minimum geometries. For a clock of 10 V, the MOS device of Fig. 5.1-7 with $W = L$ and $V_{in} = 5$ V gives R_{ON} of approximately 6 kΩ, which is sufficiently small to transfer the charge in the desired time. The minimum size switches will also help to reduce parasitic capacitances.
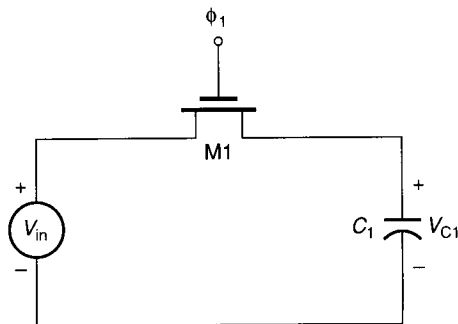

FIGURE 5.1-9
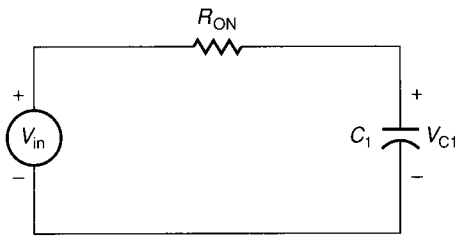An application of a MOS switch.

FIGURE 5.1-10
Model for the on state of the switch in Fig. 5.1-9.

The off state of the switch has little influence upon the performance of the circuit in Fig. 5.1-9 except for the leakage current. Figure 5.1-11 shows two cases where the leakage current can create serious problems. Figure 5.1-11a is a sample-and-hold circuit. If C_H is not large enough, then in the hold mode, where the MOS switch is off, the leakage current can charge or discharge C_H by a significant amount. Figure 5.1-11b shows an integrator. The leakage current can cause the circuit to integrate in a continuous mode, which can lead to large values of dc offset unless there is an external feedback path from V_{OUT} back to the inverting input of the operational amplifier. This feedback must contain resistors and may go through other dc circuits before returning to the input. If the
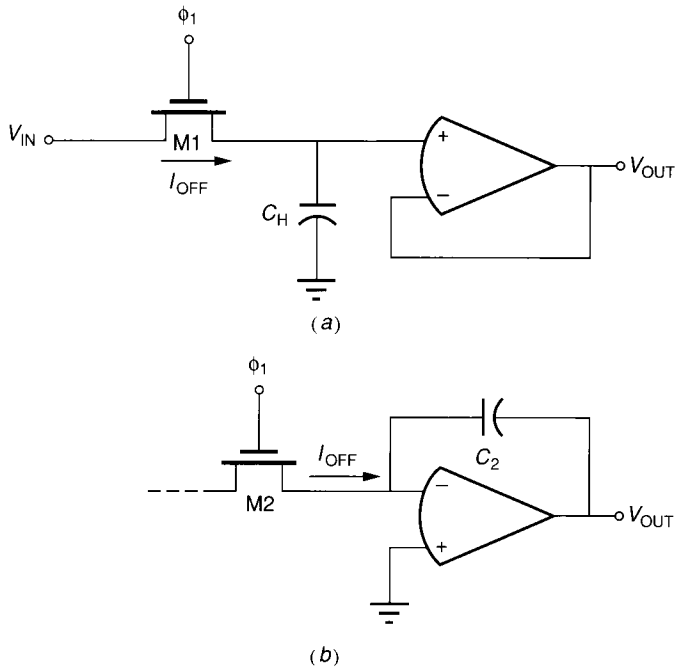

(a)

(b)

FIGURE 5.1-11
Examples of the influence of I_{OFF}: (a) Sample-and-hold circuit, (b) Integrator. Switch is off in both cases.

gate voltage of an MOS switch is equal to or less than the lowest source/drain potential, I_{OFF} is negligible.

One of the most serious limitations of switches is the clock feedthrough that can occur between the switch control signal and the switch terminals. This coupling occurs through the parasitic capacitors of the switch, namely C_{AC} and C_{BC} of Fig. 5.1-1b. Figure 5.1-12 shows the parasitic capacitances associated with the MOS switch of Fig. 5.1-9. Since the clock (gate) signal must make very large transitions, this signal can easily couple to the source and drain through C_{GS} or C_{GD}, respectively. The effects of clock feedthrough can be observed in Fig. 5.1-13 by following the sequence of events occurring when ϕ_1 is high. Assume that C_{GS} and C_{GD} are 2 fF, $C_1 = 1$ pF, $V_{in} = 5$ V and V_{C1} is initially zero. The clock waveform is shown in Fig. 5.1-13 and has finite rise and fall times for purposes of explanation. Following the convention that the lowest potential determines the source of an MOS transistor, the source will be the side connected to the capacitor. During the time t_0 to t_1 the switch is off and the clock feeds through C_{GD} and C_{GS}. The feedthrough via C_{GD} has no effect because of the voltage source V_{in}. However, the feedthrough via C_{GS} will change the voltage across C_1. Assuming the switch turns on at t_1 and connects C_1 to V_{in}, any further feedthrough has no effect, again because the voltage source V_{in} is connected to C_1. The problem occurs when the switch turns off. From t_3 to t_4 the switch is still on so that any feedthrough is unimportant. However, from t_4 to t_5 the switch is off, and feedthrough occurs from the clock to C_1. As a result, the voltage across V_{C1} is decreased below V_{in} by an amount ΔV_{C1}, given as

$$\Delta V_{C1} = (\frac{C_{GS}}{C_1 + C_{GS}})(V_{in} + V_T) \approx 0.002V_{in} \qquad (5.1\text{-}3)$$

If V_{in} is 5 V, then a feedthrough of -10 mV to C_1 occurs during the ϕ_1 phase period. This feedthrough results in an offset, which can be a very serious problem. Furthermore, the offset is dependent upon the signal level, which will cause a nonlinear offset. In general, the feedthrough will be dependent upon the switch configuration, the size of the switch, and the size of the capacitors in the circuit.

The situation concerning feedthrough is often not as bad as implied. For example, once C_1 has been charged to V_{in} (minus ΔV_{C1}) it will typically be
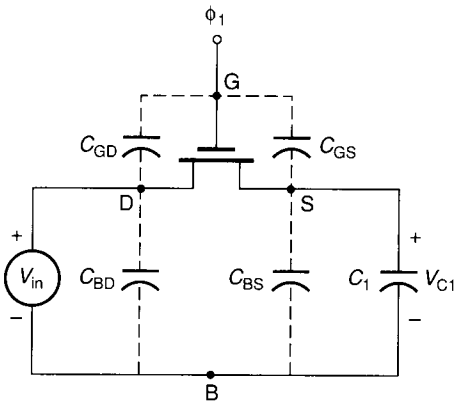
FIGURE 5.1-12
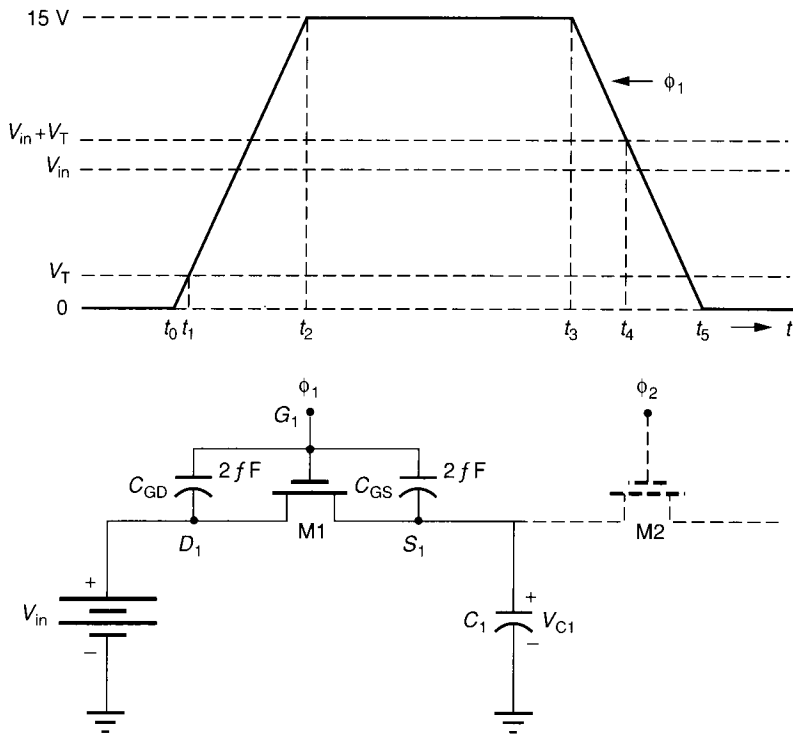Illustration of the parasitics associated with the switch of Fig. 5.1-9.

FIGURE 5.1-13
Illustration of switch feedthrough and the ϕ_1 waveform.

connected by some other switch (M2 in Fig. 5.1-13) to some other circuit. As M2 turns from off to on, there will be a positive feedthrough from ϕ_2 on to C_1 via the parasitic capacitance of M2. If the source of M2 is the terminal connected to C_1, then the net feedthrough should approximately cancel if M1 and M2 are identical. The problem is that the potential of the right-hand side of M2 is usually ground, making that side the drain and causing the positive feedthrough to be

$$\Delta V_{C1}(\text{due to M2}) = (\frac{C_{GD}}{C_{GD} + C_1})V_T \qquad (5.1\text{-}4)$$

which is less than that of Eq. 5.1-3 if $V_{in} \neq 0$.

It is possible to partially cancel some of the feedthrough effects using the technique illustrated in Fig. 5.1-14. Here a dummy MOS transistor, MD, with source and drain both attached to the signal line and the gate attached to the
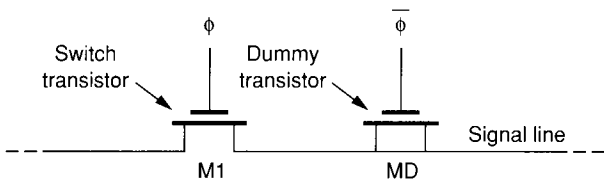

FIGURE 5.1-14
The use of a dummy transistor to cancel clock feedthrough.

inverse clock, is used to apply an opposing clock feedthrough due to M1. The area of MD can be designed to provide minimum clock feedthrough. Unfortunately, this method never completely removes the feedthrough, and in some cases may worsen it. Also, it is necessary to generate an inverted clock, which is applied to the dummy switch. In some cases, the dummy switch is a transistor with the gate attached to the source of M1, and the source and drain of the dummy switch connected to the inverse clock. This avoids charge pumping of the substrate, which can defeat the purpose of the dummy switch. Clock feedthrough can be reduced by using the largest circuit capacitors possible, using minimum geometry switches, and keeping the clock swings as small as possible. Typically, these solutions will create problems in other areas, requiring a compromise to be made.

Some of the problems associated with single-channel MOS switches can be avoided with the CMOS switch shown in Fig. 5.1-15. Using CMOS technology, a switch is usually constructed by paralleling p-channel and n-channel enhancement transistors; therefore, when ϕ is low ($\overline{\phi}$ is high) both transistors are off, creating an effective open circuit. When ϕ is high ($\overline{\phi}$ is low) both transistors are on, giving a low-impedance state. The on resistance of the CMOS switch can be lower than 1 kΩ while the off leakage current is in the 1 pA range. The bulk potentials of the p-channel (V_{BP}) and the n-channel devices (V_{BN}) are taken to the highest and lowest potentials, respectively. It is also possible to apply the clocks to the bulks of the MOS devices to improve their switching characteristics.

The CMOS switch has two advantages over the single-channel MOS switch. The first advantage is that the dynamic analog signal range in the on state is greatly increased. The second is that since the n-channel and p-channel devices are in parallel and require opposing clock signals, the feedthrough due to the clock will be diminished through cancellation.

The increased signal amplitude of the analog signal can be seen to be a direct result of using complementary devices. When one of the transistors is being turned off because of a large analog signal on the drain and source, this large analog signal will be causing the other transistor to be fully on. As a consequence, both transistors of Fig. 5.1-15 are on for analog signal amplitudes less than the clock
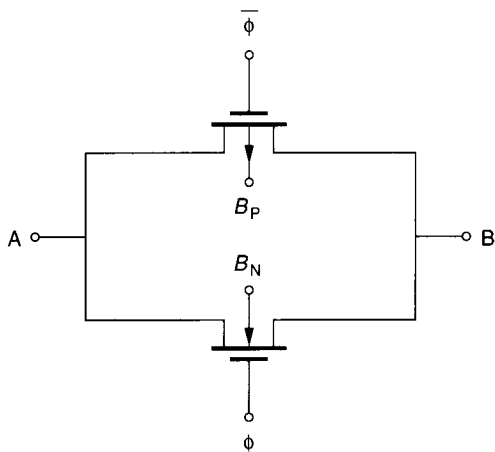

FIGURE 5.1-15
A CMOS switch.

magnitude, and at least one of the transistors is on for analog signal amplitudes equal to the magnitude of the clock signal.

The feedthrough cancellation of the CMOS switch in Fig. 5.1-15 is not complete for two reasons. One is that the feedthrough capacitances of the n-channel device are not necessarily equal to the feedthrough capacitances of the p-channel device. The second reason is that the turn-on delay of each type of transistor is not equal, and so the channel conductances do not necessarily track each other during turn-on and turn-off.

CMOS switches are generally used in place of single-channel switches when the technology permits. Although the CMOS switches have larger parasitics than single-channel switches, these parasitics can be minimized through the use of circuit techniques that will be illustrated in Chapter 8. The clock circuitry for CMOS switches is more complex because of the requirement for a complementary clock. The configuration of Fig. 5.1-15 is often called a transmission gate.

One must be careful in using switches where the power supply voltages are small. If $| V_{DD} - V_{SS} |$ is less than 5 V, it will become necessary to use a CMOS technology with twin wells so that the bulk potentials can be switched as shown in Fig. 5.1-16 in order to achieve low values of on resistance. It is
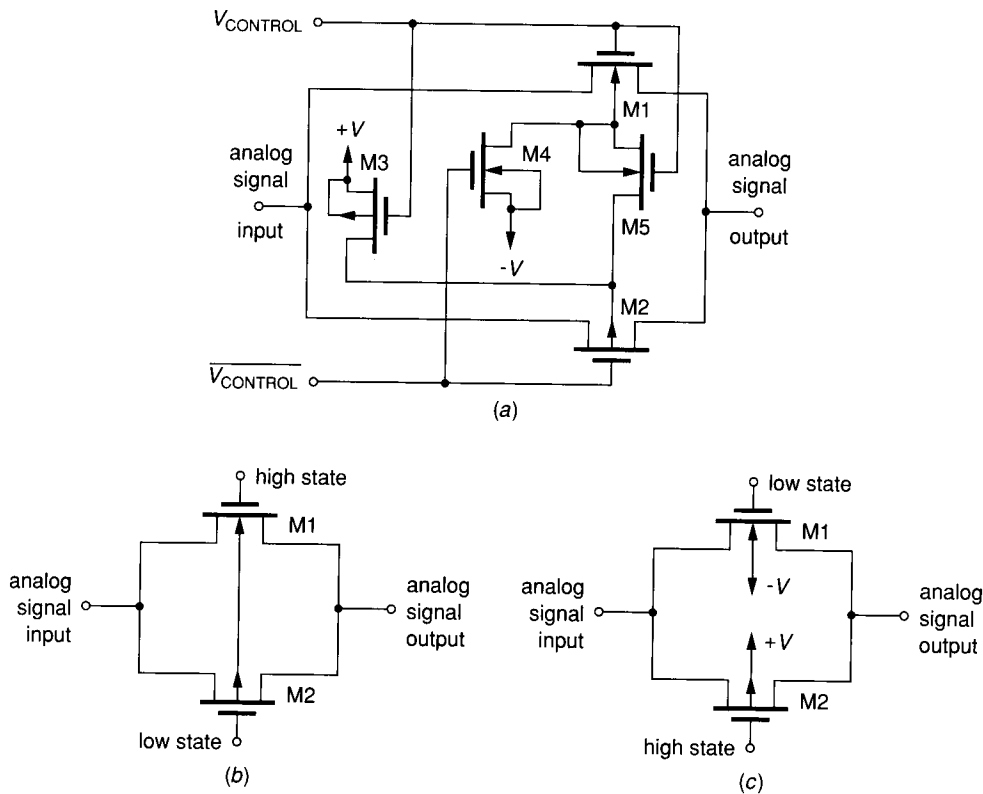

FIGURE 5.1-16
A twin-well CMOS switch with control circuitry: (a) Circuit, (b) On state, (c) Off state.

assumed that $V_{CONTROL}$ and $\overline{V_{CONTROL}}$ are generated from the clock waveform. When $V_{CONTROL}$ is high, the transmission gate is on. The equivalent circuit in this condition is shown in Fig. 5.1-16b. Here we see that the n-channel gate is taken to the high state and the p-channel gate is in the low state. Also the substrates have been connected together by means of the switches M3, M4, and M5. M3 and M4 are off while M5 is on. This helps to keep the switch on resistance from being a function of the analog signal potential. When $V_{CONTROL}$ is low, the transmission gate is off and has the equivalent circuit shown in Fig. 5.1-16c. The bulks of the n- and p-channel device terminals have been taken to $-V$ and $+V$, respectively, since M3 and M4 are on and M5 is off. This insures that the off state will be maintained since V_{BS} is strongly reverse-biased and causes a large V_T.

If $| V_{DD} - V_{SS} |$ is less than 4 V, switches can only be used if a clock signal of 5 V or higher can be obtained. One can either apply external clocks or use a voltage doubler to provide an on-chip voltage which is higher than $| V_{DD} - V_{SS} |$.

In this section we have seen that the MOS transistor makes a good switch realization for integrated circuits. They require small area, dissipate very little power, and provide reasonable values of R_{ON} and R_{OFF} for most applications. This section has also illustrated the importance of the terminal voltages on the behavior of the MOS transistor. The incorporation of a good realization of a switch into the basic building blocks will produce some interesting and useful circuits and systems which will be studied in the following material.

5.2 ACTIVE RESISTORS

In Chapters 2 and 3, the implementation of a resistance and a capacitance by IC technologies was discussed. The passive components including resistors and capacitors are very important in analog signal processing. Typically the gain of an amplifier is determined by ratios of resistors or capacitors while the time constant of a filter is determined by the product of resistors and capacitors. Thus, the performance of many analog systems can be directly related to their resistive and capacitive passive components.

The capacitor can be implemented as a parallel plate configuration of a conductor-insulator-conductor sandwich. The MOS capacitance uses the thin oxide of the MOS process as the insulator while the conductors (plates) can be metal, polysilicon, or a heavily doped semiconductor. The conductor-insulator-conductor capacitor was found to be a near ideal component, having only the problems of size and parasitics. For reasonable area usage the value of the conductor-insulator-conductor capacitor is limited to the 10–20 pF range. Fortunately, in many applications the influence of the parasitics can be eliminated. Another possible implementation of the capacitor is the pn junction capacitance. This capacitance exhibits a strong voltage dependence, which limits its usefulness.

Compared to capacitors, the resistors implemented by IC technologies were found to be lacking in several areas of performance. The typical sheet resistance was sufficiently small that large values of resistors required large areas. The higher value of resistance attained with pinched resistors suffered nonlinearity. In

addition, the tolerance of the resistors, their temperature coefficient, and their voltage coefficient were all poorer than those of the capacitor. Of course, modifications to the standard IC technology can result in better resistor implementation. However, the objective of this section is to investigate ways of emulating a resistor without having the inherent disadvantages using standard IC technologies.

We shall discuss two ways of implementing resistors that have found use in integrated circuit design. The first method is to use active devices, such as those introduced in Sec. 3.4, and the second method is to use switched capacitors. The first method has the advantage of minimizing the area required for resistors, and the second has the advantage of a resistor whose accuracy is dependent upon the frequency of a clock and a capacitor. It will be shown that the RC time constant accuracy of circuits using a switched capacitor resistor simulation is equivalent to the relative accuracy of the capacitor, which is quite good.

There are two distinct applications of resistors that are important. These applications are dc resistors and ac resistors. The dc resistor is typically used to provide a dc voltage drop given a dc current. The ac resistor provides an ac voltage drop given an ac current. Figure 5.2-1 illustrates the difference, although in many cases the resistor is used simultaneously as both an ac and dc resistor. As a dc resistor, Fig. 5.2-1 shows that a dc voltage drop of V_Q is produced for a dc current of I_Q. As an ac resistor, Fig. 5.2-1 shows that an ac voltage of ΔV_Q is produced for an ac current of ΔI_Q. The use of an active element to implement a dc resistor will be considered first.

Ignoring the substrate terminal for the moment, the MOS and BJT transistors are three-terminal devices. Through proper connection of these three terminals,
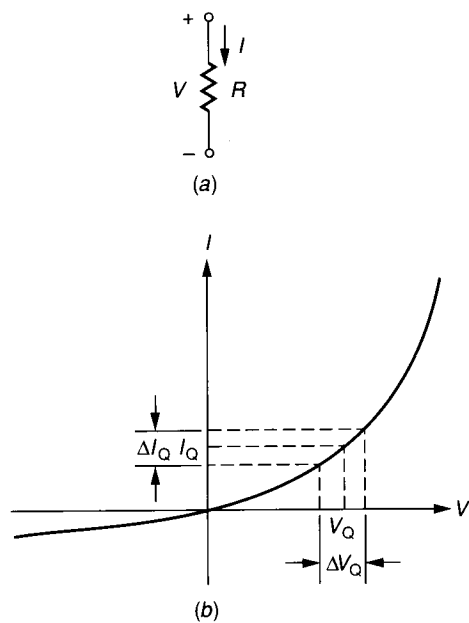

FIGURE 5.2-1
The distinction between a dc and an ac resistor. (a) Resistor, (b) I-V characteristics.

the active device becomes a two-terminal resistor called an *active resistor*. The active resistor can be used in place of a polysilicon or diffused resistor to produce a dc voltage drop and/or provide a small signal resistance that is linear over a small range. There are many cases where the area required to obtain a small signal resistance is more important than the linearity. A small MOS or BJT device can simulate a resistor in much less area than is required with an equivalent polysilicon or diffused resistor.

The active resistor can be implemented by simply connecting the gate of an n- or p-channel enhancement MOS device to the drain, as shown in Fig. 5.2-2*a* and *b*. For the n-channel device, the source should be placed at the most negative power supply voltage, V_{SS}, if possible, to eliminate the bulk effect. The source of the p-channel device should be taken to the most positive voltage for the same reason. Since V_{GS} is now equal to V_{DS}, the transconductance curve (I_D vs. V_{GS}) of the MOS transistor shown in Fig. 5.2-2*c* characterizes the large signal behavior of the active resistor. This curve is valid for both the n- and p-channel enhancement transistors for the polarities shown. It is seen that the resistance is not linear, which was anticipated. In many circumstances, the signal swing is very small, and in these cases the active resistor works very well. Since the connection of the gate to the drain guarantees operation in the saturation region for $V > V_T$, the I–V characteristics can be written as

$$I = I_D = \frac{K'W}{2L}\left[(V_{GS} - V_T)^2\right]$$ (5.2-1)

or

$$V = V_{GS} = V_{DS} = V_T + \left(\frac{2I_D L}{K'W}\right)^{1/2}$$ (5.2-2)

where

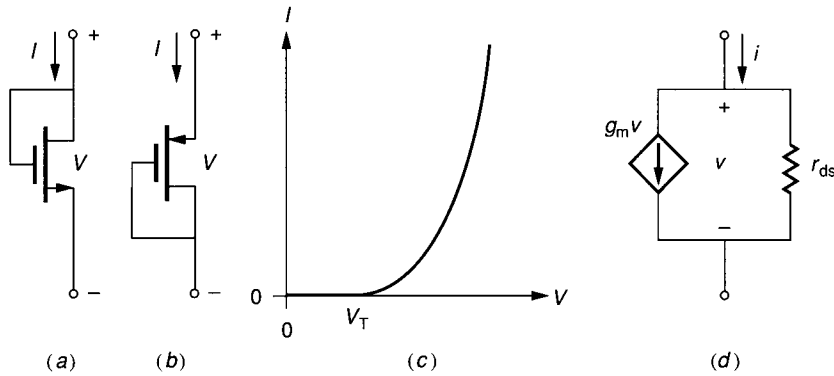$$K' = \mu_o C_{ox}$$ (5.2-3)

FIGURE 5.2-2
(*a*) n-channel enhancement active resistor, (*b*) p-channel enhancement active resistor, (*c*) Voltage–current characteristics of the MOS active resistor, (*d*) Small signal model of *a* or *b*.

If either V or I is defined, then the other variable can be found by using Eq. 5.2-1 or Eq. 5.2-2.

Connecting the gate to the drain means that V_{DS} controls I_D, and therefore the channel transconductance becomes a channel conductance. The small signal conductance can be found by differentiating Eq. 5.2-1 with respect to V, resulting in

$$g = \frac{\partial I}{\partial V} \cong \left(\frac{2I\, K'W}{L} \right)^{1/2} = \frac{K'W}{L}(V - V_T) \qquad (5.2\text{-}4)$$

Another method of finding the small signal conductance is to use the small signal model of the MOS transistor of Fig. 3.1-14. The small signal model of the active resistor valid for either the n- or the p-channel active resistor is shown in Fig. 5.2-2d where $r_{ds} = 1/g_{ds}$. Assuming $v_{bs} = 0$, it is easily seen that the small signal conductance of these circuits is

$$g = \frac{1 + g_m r_{ds}}{r_{ds}} \cong g_m \qquad (5.2\text{-}5)$$

where $g_m r_{ds}$ is greater than unity. The influence of an ac bulk voltage can be incorporated into Eq. 5.2-5 using the same model (see Prob. 5.8). In either case, we note how the value of g depends upon the dc values of V and I (refer back to Table 3.1-3 in Chapter 3 for the dependence of g_m and r_{ds} upon V and I).

The bipolar junction transistor can be used to form an active resistor in the same manner as for the MOS transistor. The circuit of Fig. 5.2-3 is topologically identical to the MOS circuit of Fig. 5.2-2. When operating in the forward active region, it follows from Eq. 3.3-10 that the I–V characteristics of the BJT active resistor can be expressed as

$$I \cong I_s \exp(V/V_t) \qquad (5.2\text{-}6)$$
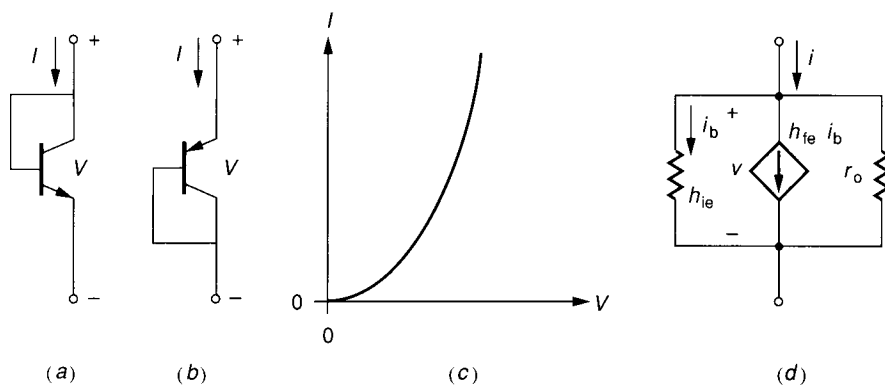

FIGURE 5.2-3

(a) npn BJT active resistor, (b) pnp BJT active resistor, (c) Voltage-current characteristics of the BJT active resistor, (d) Small signal model for the BJT active resistor.

or

$$V = V_t \ln \left[\frac{I}{I_s} \right] \tag{5.2-7}$$

where

I_s = reverse saturation current of the emitter base junction
$V_t = (kT)/q = 0.026$ V at room temperature

The small signal conductance of the BJT active resistor can be found by differentiating Eq. 5.2-6 with respect to V ($= V_{BE}$) to get

$$g = \frac{\partial I}{\partial V} = \frac{|I|}{V_t} \tag{5.2-8}$$

The small signal model of Fig. 5.2-3d, derived from Fig. 3.3-8, can also be used to more accurately calculate the small signal conductance and gives

$$g = h_{oe} + \frac{1 + h_{fe}}{h_{ie}} \tag{5.2-9}$$

These small signal model parameters have been defined in Table 3.3-4 of Chapter 3. The dependence of g upon the dc values of the BJT active resistor are indicated by Table 3.3-4.

Active resistors can be used to produce a dc voltage or to provide a small signal resistance. An example illustrating the application of the active resistor to provide a dc voltage follows.

Example 5.2-1. Voltage division using active resistors. Figure 5.2-4 shows the use of an n-channel MOS active resistor and a p-channel MOS active resistor to provide a dc voltage, V_{out}. Find a W/L ratio for M1 and M2 that give V_{out} of 1 V if $V_{DD} = 5$ V, $V_{SS} = -5$ V and $I = 50\ \mu$A. Assume that $V_{TN} = +0.75$ V, $V_{TP} = -0.75$ V, $K'_N = 2.4 \times 10^{-5}$ A/V^2 and $K'_P = 0.8 \times 10^{-5}$ A/V^2.

Solutions. Both bulks are connected to their respective sources so that the body effect has no influence. Also since $V_{DG} = 0$, both transistors are saturated. Since the currents through both transistors must be the same and V_{DS1} and V_{DS2} are defined, we can solve for the W/L ratios of M1 and M2 using Eq. 5.2-1 as 0.15 and 1.18, respectively.
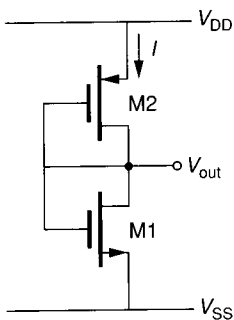

FIGURE 5.2-4
Use of active resistors to achieve voltage division.

BJT active resistors can be used to divide voltages in the same manner as illustrated in the example; however, the voltages across the BJT are limited to less than 1 V.

The use of active resistors to develop large dc voltages requires large currents or W/L ratios that are much less than unity. This can be circumvented by cascading devices as shown in Fig. 5.2-5. The voltages V_1, V_2 and V_3 are given by Eq. 5.2-2, where I is from a known current source. If the voltages are specified, then the W/L ratio of each device can be determined from Eq. 5.2-2 if the bulk–source voltage is taken into consideration. If the W/L ratios are given, then the voltages V_1 through V_3 can be calculated starting with V_1. Using more than one device to drop the voltage will result in W/L ratios closer to unity and smaller dc currents.

Example 5.2-2. Replacement of one active resistor by two. An n-channel MOS active resistor is used to produce a dc voltage drop of 5 V from a 25 μA current. Assuming that the bulk–source effects can be neglected, (*a*) find the W/L ratio of a single active resistor, and (*b*) find the W/L ratio of two identical n-channel active resistors in series replacing the single active resistor of (*a*). Assume that the MOS parameters of Example 5.2-1 are valid in this example. Compare the gate area required for both cases.

Solution. For case (*a*) we get $W/L = 1/8.7$. If we assume that W has a unit length, then the gate area required is 8.7 square units. For case (*b*) we find that the W/L of one of the transistors is $1/1.47$. If $W = 1$, then $L = 1.47$ with a gate area of 1.47, two identical active resistors would require 2.94 square units. A savings in gate area of almost 3 to 1 results in case (*b*) compared to case (*a*). The source and drain area would reduce this ratio.
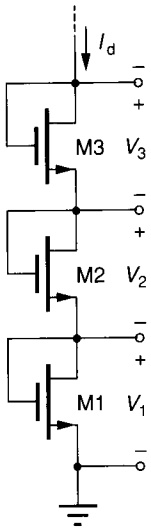

FIGURE 5.2-5
Use of cascaded devices to create large voltage drops.

The second application of a resistor is to provide an ac voltage (or current) for a given ac current (or voltage). In this presentation, the dc current will be zero. For a zero dc current, the active resistors of Figs. 5.2-2 and 5.2-3 are not satisfactory because the value of resistance approaches infinity. The switches of Figs. 5.1-3 and 5.1-4 make a much better realization of an ac resistor with the MOS switch being nearly linear and having no dc offset. By controlling the value of voltage between the gate and source, one can get a linear ac resistance for values ΔV up to 1 V.

> **Example 5.2-3. A MOS switch as an ac resistor.** Assume that the circuit of Fig. 5.1-4a is to be used to implement an ac resistor of 2000 Ω and that the device parameters are $V_T = 0.75$ V, $K'_N = 24\,\mu\text{A/V}^2$, $\gamma_N = 0.8\,\text{V}^{1/2}$, $\lambda = 0.01\,\text{V}^{-1}$, and $\phi = 0.6$ V. If $W = 50\,\mu$, $L = 10\,\mu$, $V_{DS} = 0$, and $V_{BS} = -5$ V, find the value of V_{GS} ($= V_C$).
>
> **Solution.** The threshold voltage due to $V_{BS} = -5$ V is 2.023 V. Equating 2000 Ω to Eq. 5.1-2 of Sec. 5.1 gives a value of $V_{GS} = 6.19$ V. The dotted line in Fig. 5.1-4b corresponds to a resistance of 2000 Ω. Figure 5.1-4b shows that the 2000 Ω resistor is closely approximated by this value of V_{GS}.

The linearity of the ac resistor in the example is limited for negative values of V_{DS} by the effects of V_{BS} and for positive values of V_{DS} by V_{DS} itself. The bulk influences the linearity by causing V_T to change. The drain–source voltage influences the linearity by leaving the ohmic region and entering the saturation region. Techniques for eliminating both of these effects will now be considered.

Figure 5.2-6 shows how to eliminate the influence of V_{DS} upon the ac resistor realization.[1] The principle employed is to use two identical devices biased
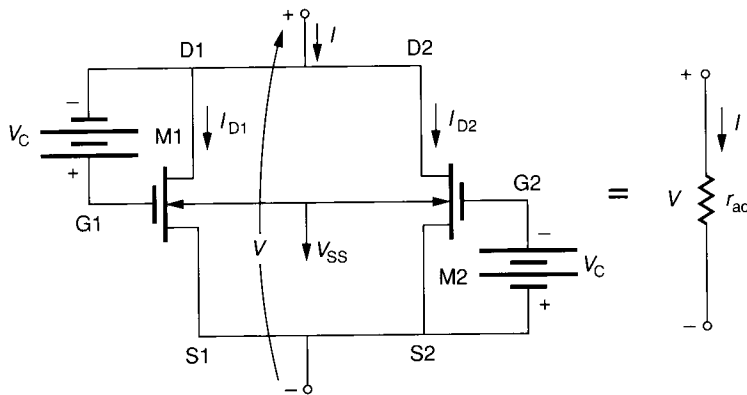

FIGURE 5.2-6
Configuration to eliminate the effects of V_{DS} in the ac resistor implementation of Figure 5.1-4a.

so that the influences of V_{DS} cancel. Using Eq. 3 of Table 3.1-1 to obtain expressions for I_{D1} and I_{D2} gives

$$
\begin{aligned}
I_{D1} &= K_N' \left(\frac{W_1}{L_1} \right) \left[(V_{GS1} - V_{T1}) V_{DS1} - \frac{V_{DS1}^2}{2} \right] \\
&= K_N' \left(\frac{W_1}{L_1} \right) \left[(V_{DS1} + V_C - V_{T1}) V_{DS1} - \frac{V_{DS1}^2}{2} \right] \qquad (5.2\text{-}10) \\
&= K_N' \left(\frac{W_1}{L_1} \right) \left[\frac{V_{DS1}^2}{2} + (V_C - V_{T1}) V_{DS1} \right]
\end{aligned}
$$

and

$$
\begin{aligned}
I_{D2} &= K_N' \left(\frac{W_2}{L_2} \right) \left[(V_{GS2} - V_{T2}) V_{DS2} - \frac{V_{DS2}^2}{2} \right] \\
&= K_N' \left(\frac{W_2}{L_2} \right) \left[(V_C - V_{T2}) V_{DS2} - \frac{V_{DS2}^2}{2} \right]
\end{aligned}
\qquad (5.2\text{-}11)
$$

Noting that $V_{DS1} = V_{DS2} = V$ and assuming matched transistors allows the current I to be expressed as

$$
I = I_{D1} + I_{D2} = \frac{2K_N' W}{L} (V_C - V_T) V_{DS} \qquad (5.2\text{-}12)
$$

Thus the value of ac resistance found by differentiating Eq. 5.2-12 with respect to I is

$$
r_{ac} = \frac{\partial V_{DS}}{\partial I} = \frac{1}{2K_N'(W/L)(V_C - V_T)} \qquad (5.2\text{-}13)
$$

In the development of Eq. 5.2-13, it has been assumed that the transistors remain in the ohmic region or that V_{DS} is less than $V_{GS} - V_T$. This assumption places the following constraint on the value of V for Eq. 5.2-13 to be valid.

$$
V < (V_C - V_T) \qquad (5.2\text{-}14)
$$

Therefore, a larger value of V_C will lead to a larger range of V. While the linearity range has been increased, the dependence upon V_{BS} through V_T is still present and must be eliminated to achieve a wide linearity range.

In many applications, resistors are used differentially in pairs. In these cases it is possible to achieve an increase in linearity and to eventually even cancel the bulk effects. A method of canceling the effects of V_{DS} will be discussed first. Figure 5.2-7a shows a pair of ac resistors used in a differential configuration.[2] Note that a differential signal (V_1) is applied to the left-hand side of the resistors
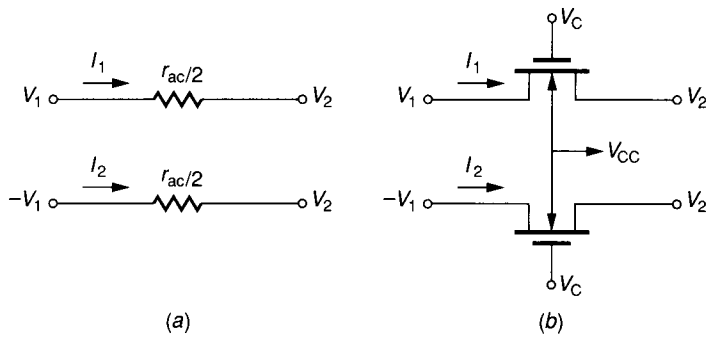
FIGURE 5.2-7

(a) Differential ac resistor configuration, (b) Single-MOS implementation of a.

while the right-hand side is at the same potential (although not physically connected). Again Eq. 3 of Table 3.1-1 can be used to write

$$I_1 = \frac{K_N'W}{L}\left[(V_C - V_2 - V_T)(V_1 - V_2) - \frac{1}{2}(V_1 - V_2)^2\right] \qquad (5.2\text{-}15)$$

and

$$-I_2 = \frac{K_N'W}{L}\left[(V_C + V_1 - V_T)(V_2 + V_1) - \frac{1}{2}(V_2 + V_1)^2\right] \qquad (5.2\text{-}16)$$

Adding Eqs. 5.2-15 and 5.2-16 gives

$$I_1 - I_2 = \frac{K_N'W}{L}(V_C - V_T)2V_1 \qquad (5.2\text{-}17)$$

Defining r_{ac} as

$$r_{ac} = \frac{2V_1}{I_1 - I_2} \qquad (5.2\text{-}18)$$

gives

$$r_{ac} = \frac{1}{(K_N'W/L)(V_C - V_T)} \qquad (5.2\text{-}19)$$

Therefore, Fig. 5.2-7a simulates a resistor r_{ac} which is independent of V_1 or V_2 as long as

$$|V_1 - V_2| = V < V_C - V_T \qquad (5.2\text{-}20)$$

Figures 5.2-8a and b show the I–V characteristics of the resistors of Figs. 5.2-6 and 5.2-7b using n-channel transistors having $W = 50\,\mu$, $L = 10\,\mu$ and model parameters of $V_T = 0.75$ V, $K_N' = 24\,\mu\text{A/V}^2$, $\gamma_N = 0.8\ \text{V}^{1/2}$, $\lambda_N = 0.01\ \text{V}^{-1}$, and $\phi_N = 0.6$ V. The characteristics of Fig. 5.2-8a and b are almost identical and considerably more linear than Fig. 5.1-4b. For large values of V_C, the linearity range increases, as predicted by Eq. 5.2-20.
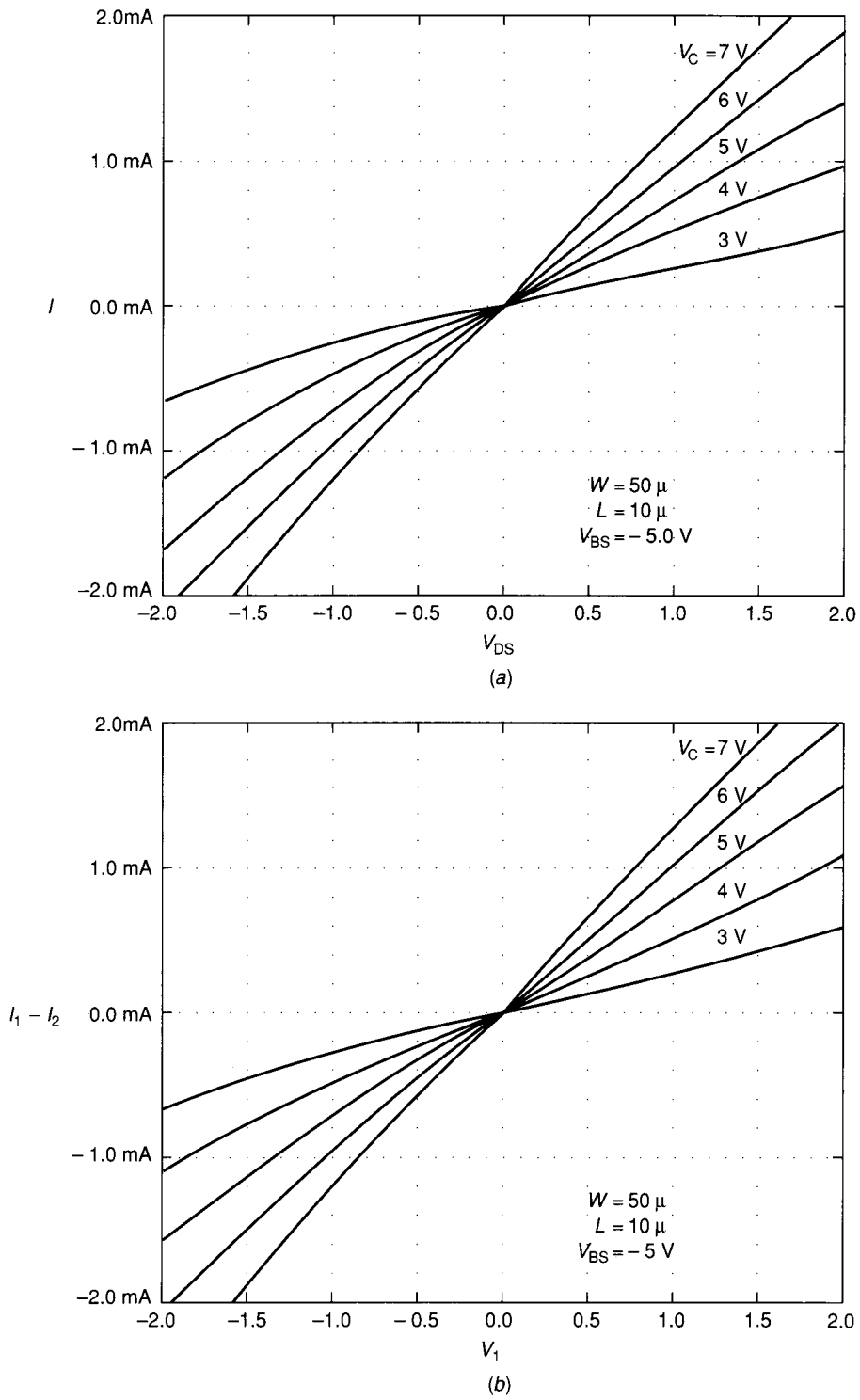
FIGURE 5.2-8
I–V characteristics of: (*a*) Parallel MOS resistor, (*b*) A single-MOS differential resistor. (Note that the actual voltage across Fig. 5.2-7 is $2V_1$.)

311

A double-MOS, differential configuration, shown in Fig. 5.2-9a, not only linearizes the ac resistor but removes the influence of the bulk-source voltage.[2] The relationship for the ac resistance can be obtained by assuming all of the devices are matched and in the ohmic region. Using Eq. 3 of Table 3.1-1 to solve for I_1 and I_2 results in the following.

$$I_1 = I_{D1} + I_{D3} = \frac{K_N'W}{L}\left[(V_{C1} - V_3 - V_T)(V_1 - V_3) - \frac{1}{2}(V_1 - V_3)^2\right]$$

$$+ \frac{K_N'W}{L}\left[(V_{C2} - V_3 - V_T)(V_2 - V_3) - \frac{1}{2}(V_2 - V_3)^2\right]$$

$$(5.2\text{-}21)$$

and

$$I_2 = I_{D2} + I_{D4} = \frac{K_N'W}{L}\left[(V_{C2} - V_3 - V_T)(V_1 - V_3) - \frac{1}{2}(V_1 - V_3)^2\right]$$

$$+ \frac{K_N'W}{L}\left[(V_{C1} - V_3 - V_T)(V_2 - V_3) - \frac{1}{2}(V_2 - V_3)^2\right]$$

$$(5.2\text{-}22)$$

Using Eqs. 5.2-21 and 5.2-22 to find $I_1 - I_2$ gives

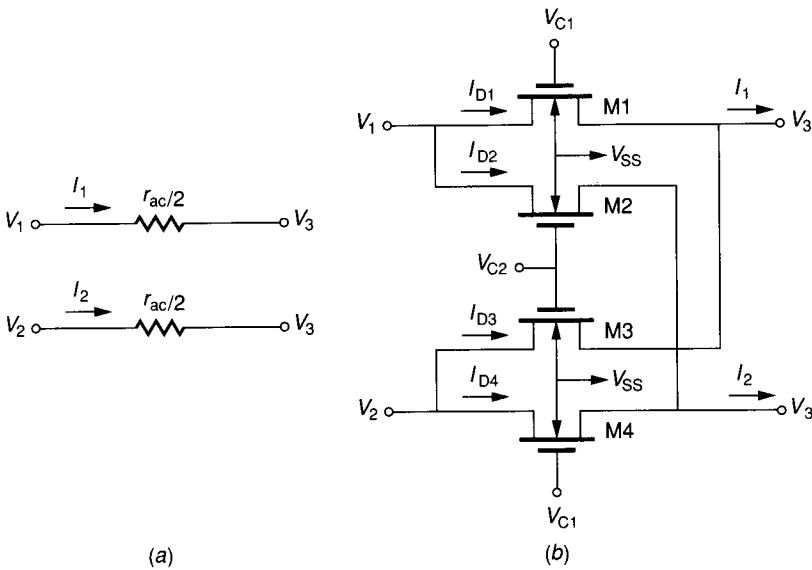$$I_1 - I_2 = \frac{K_N'W}{L}(V_{C1} - V_{C2})(V_1 - V_2) \qquad (5.2\text{-}23)$$

FIGURE 5.2-9
(a) Differential ac resistor configuration, (b) Double-MOS implementation of a.

r_{ac} can be found as

$$r_{ac} = \frac{V_1 - V_2}{I_1 - I_2} = \frac{1}{(K_N' W/L)(V_{C1} - V_{C2})} \qquad (5.2\text{-}24)$$

Because all devices have been assumed to be in the ohmic region, Eq. 5.2-24 only holds when

$$V_1, V_2 \leq \min [V_{C1} - V_T, V_{C2} - V_T] \qquad (5.2\text{-}25)$$

Figure 5.2-10 is a simulation of Fig. 5.2-9b when $V_{C1} = 7$ V, $V_3 = 0$, $V_{BS} = -5$ V and using the same device parameters as have been used for Figs. 5.1-4 and 5.2-7. It is of interest to compare the ac resistor realizations of Figs. 5.1-4, 5.2-6, 5.2-7b and 5.2-9b. Of all the realizations, the double-MOSFET differential resistor of Fig. 5.2-9b is superior in linearity. However, the double-MOSFET differential resistor is really a transresistance in that the voltages and currents are at different terminals. This restricts the double-MOSFET differential resistance to transresistance applications that are found in differential-in, differential-out op amps. The parallel MOS resistor of Fig. 5.2-6 and the single-MOSFET differential resistor of Fig. 5.2-7b are true resistor realizations that have approximately the same linearity. However, the parallel MOS resistor is a true floating resistor realization while the single MOSFET differential resistor must have a differential signal with reference
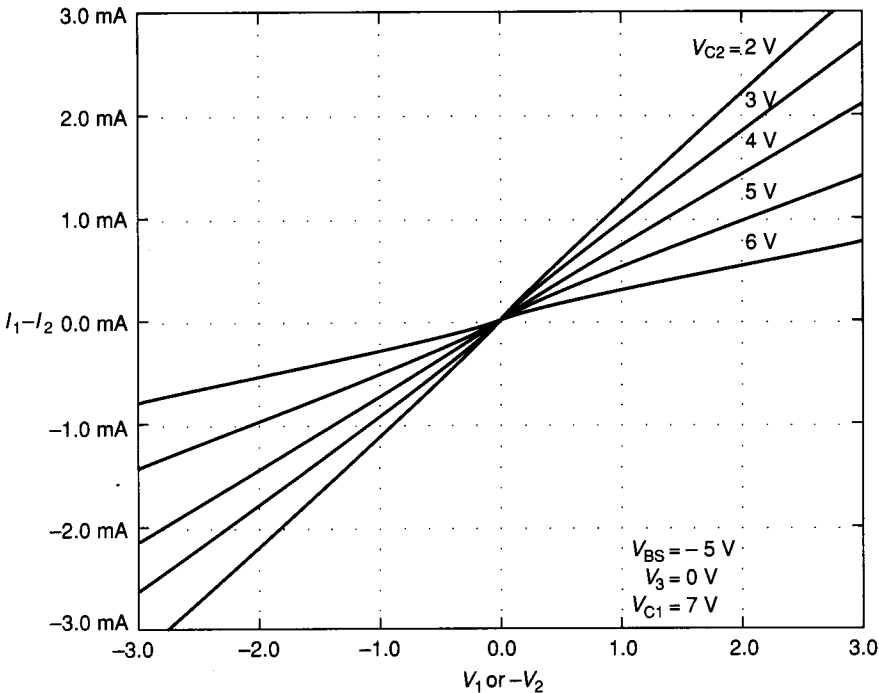

FIGURE 5.2-10
I–V characteristics of a double-MOS differential resistor.

to V_2 of Fig. 5.2-7b. The performances of the ac resistor realizations that have been presented are summarized in Table 5.2-1.

A second approach to realizing ac resistors uses switches and capacitors. This approach is *discrete-time* and is often called the *switched capacitor* (SC) realization. If the clock rate is high enough, combinations of switches and capacitors can implement a resistor that is dependent only on the clock frequency and the capacitor. Four combinations of switches and capacitors will be considered.

The first approach to resistor simulation is called the parallel switched capacitor realization and is shown in Fig. 5.2-11a. It will be shown that under certain conditions, namely those found in a sampled data system, that the switched capacitor of Fig. 5.2-11a is an approximate realization of the resistor of Fig. 5.2-11b. Figure 5.2-11c shows the clock waveforms that control the opening and closing of the switches in Fig. 5.2-11a. Let us assume that V_1 and V_2 are two independent dc voltage sources. This assumption represents no loss of generality since the conditions for a sampled data system state that the "signals," V_1 and V_2, are sampled at a rate that is sufficiently high that any change in V_1 or V_2 during a sampling period can be ignored.

Under steady state conditions, we can express the charge flow in the direction of I_1 over a time period from t_0 to $t_0 + T$ as

$$q_1(t_0 + T) = \int_{t_0}^{t_0 + T} I_1(t)dt \qquad (5.2\text{-}26)$$

However, this charge flow in the direction of I_1 during the time period from t_0 to $t_0 + T$ can be broken into two parts. The first part is the charge flowing from t_0 to $T/2$ and is given as

$$q_1\left(t_0 + \frac{T}{2}\right) = C\left[V_1\left(t_0 + \frac{T}{2}\right) - V_2(t_0)\right] \simeq C(V_1 - V_2) \qquad (5.2\text{-}27)$$

TABLE 5.2-1
Summary of R_{ac} realization characteristics

AC resistance realization	Figure	Linearity	How controlled	Restrictions
Single MOSFET	5.1-4	Poor	Gate voltage W/L	$V_{BULK} < \min(V_S, V_D)$
Parallel MOSFET	5.2-6	Good	V_C W/L	$V < V_C - V_T$ $V_{BULK} < \min(V_S, V_D)$
Single-MOSFET differential resistor	5.2-7a	Good	V_C W/L	$\|V_1 - V_2\| < V_C - V_T$ $V_{BULK} < -V_1$ Differential around V_2
Double-MOSFET differential resistor	5.2-9a	Good	$(V_{C1} - V_{C2})$ W/L	$V_1, V_2 < \min(V_{C1} - V_T, V_{C2} - V_T)$ $V_{BULK} < \min(V_1, V_2)$ Transresistance only

(a)

(b)

(c)
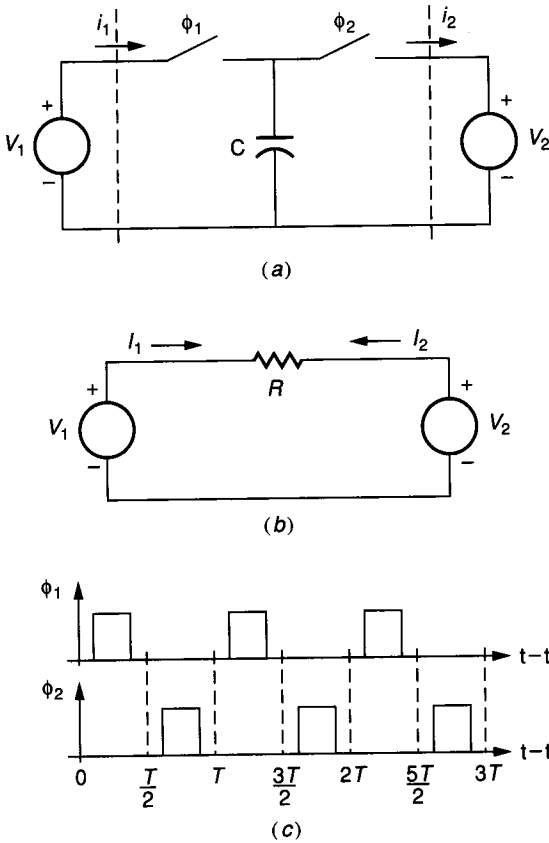
FIGURE 5.2-11
(a) Parallel switched capacitor resistor realization, (b) A continuous resistor, (c) Clock waveforms for the switches of a.

The second part is the charge flowing from $T/2$ to T and is given as

$$q_1(t_0 + T) - q_1\left(t_0 + \frac{T}{2}\right) = 0$$

Therefore, Eq. 5.2-26 can be written as,

$$q_1(t_0 + T) = C(V_1 - V_2) = \int_{t_0}^{t_0 + T} I_1(t)\,dt \qquad (5.2\text{-}28)$$

Dividing both sides of Eq. 5.2-28 by T results in

$$\frac{C(V_1 - V_2)}{T} = \frac{1}{T}\int_{t_0}^{t_0 + T} I_1(t) = I_1(\text{aver}) \qquad (5.2\text{-}29)$$

Now let us find the average current, $I_1(\text{aver})$, flowing into the left-hand side of the continuous resistor of Fig. 5.2-11b. This value is given as

$$I_1(\text{aver}) = I_1 = \frac{V_1 - V_2}{R} \qquad (5.2\text{-}30)$$

Equating Eqs. 5.2-29 and 5.2-30 results in

$$R = \frac{T}{C} = \frac{1}{Cf_{clock}} \tag{5.2-31}$$

where $f_{clock} = 1/T$ is the frequency of the clock signals ϕ_1 and ϕ_2.

Therefore, we have shown that the switched capacitor circuit of Fig. 5.2-11a simulates the continuous resistor of Fig. 5.2-11b. We see that the switched capacitor resistor realization is dependent upon the capacitor C and the period or the frequency of the clock. The following example illustrates that very large resistors can be realized with a small amount of silicon area using switched capacitors.

> **Example 5.2-4. Switched capacitor resistor realization.** If a 1 MΩ resistor is to be realized using the SC technique of Fig. 5.2-11 with a clock frequency of 100 kHz find the value of the capacitor and its area assuming that the capacitor is a polysilicon-to-polysilicon type. Compare this area to that required for a polysilicon resistor of the same value.
>
> *Solution.* Equation 5.2-31 shows that the capacitance is 10 pF. Assuming a capacitance per unit area of 0.2 pF/mil^2 gives an area of 50 mils^2. Using a polysilicon resistor with a sheet resistivity of 25 Ω/square requires an area of 3600 mils^2 using a minimum width of 0.3 mils. In addition to the capacitor area, the switched capacitor resistor realization requires two minimum-size MOS devices as the switches.

There are several other types of switched capacitor realizations of resistors. Figure 5.2-12 shows a realization called a series switched capacitor resistor, which results in a resistance given by Eq. 5.2-31. Figure 5.2-13 illustrates a series-parallel switched capacitor realization. It can be shown (see Prob. 5.15) that the equivalent resistance of the series-parallel switched capacitor resistor realization is

$$R = \frac{T}{C_1 + C_2} = \frac{1}{(C_1 + C_2)f_{clock}} \tag{5.2-32}$$
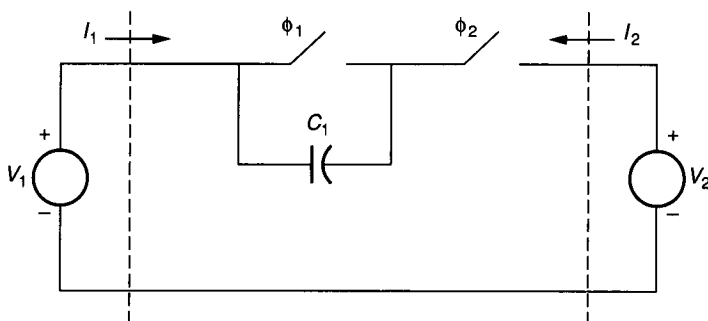

FIGURE 5.2-12
Series switched capacitor realization of a continuous resistor.
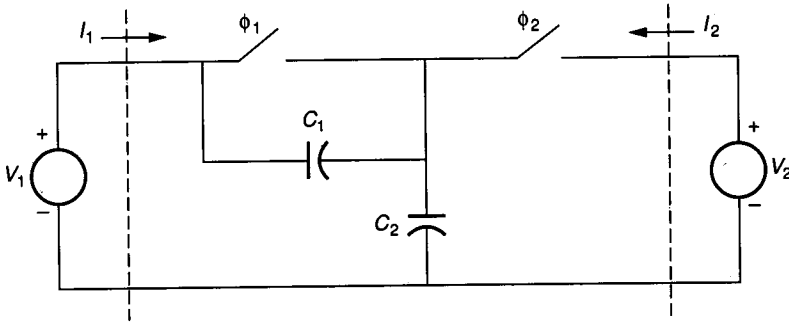
FIGURE 5.2-13
Series-parallel switched capacitor realization of a continuous resistance.

Figure 5.2-14 shows a switched capacitor resistor realization called the bilinear realization. The equivalent resistance of the bilinear switched capacitor resistance realization is (see Prob. 5.16)

$$R = \frac{T}{4C} = \frac{1}{4Cf_{\text{clock}}} \tag{5.2-33}$$

Table 5.2-2 summarizes the four switched capacitor resistor realizations discussed here.

This section has focused on the realization of dc and ac resistors using methods compatible with the standard IC technologies. It is discovered the MOS technology offers many more opportunities in this area. The reader will see all of these resistor realizations used along with other components in the following material. The most important concepts presented are the methods by which the dependence of drain current on the drain–source and bulk–source voltages can be reduced and the method by which resistors can be simulated by switches
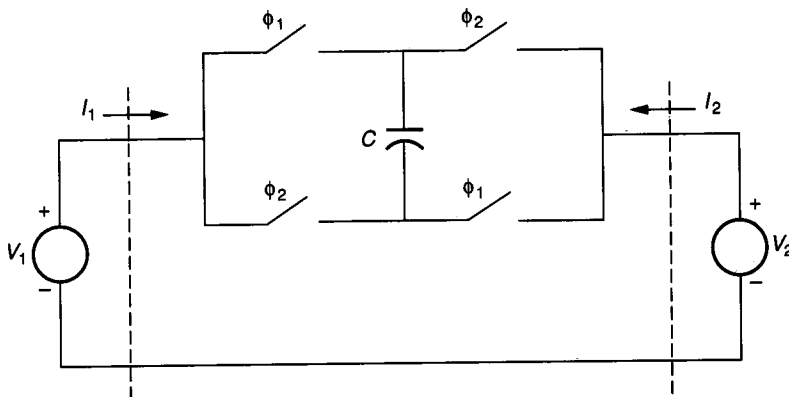

FIGURE 5.2-14
Bilinear switched capacitor realization of a continuous resistance.

TABLE 5.2-2
Summary of switched capacitor resistance realizations

SC resistor realization	Figure	Equivalent resistance	Type of resistance
Parallel	5.2-11a	T/C	Transresistance
Series	5.2-12	T/C	Resistance or transresistance
Series-parallel	5.2-13	$\dfrac{T}{C_1 + C_2}$	Transresistance
Bilinear	5.2-14	$\dfrac{T}{4C}$	Transresistance or resistance

and capacitors. Because the resistors realized by switched capacitor circuits are inversely proportional to capacitance, the effective RC time constants become proportional to capacitor ratios. The result is that time constants can be accurately realized using capacitors and switched capacitor resistor realizations.

5.3   CURRENT SOURCES AND SINKS

In this section we consider the realization of current sinks and sources that use standard bipolar or MOS devices. An ideal *current source* is a two-terminal element whose current is constant for any voltage across the source. The voltage across a current source depends upon the external circuitry. Figures 5.3-1a and b give the schematic symbol and the *I–V* characteristics of a current source whose value is I_0. Most current source applications require one of their terminals to be common with the most positive or the most negative dc voltage in the circuit. This leads to the two possible configurations illustrated in Fig. 5.3-2. V_P and V_N are the most positive and most negative dc voltages, respectively. The configuration of Fig. 5.3-2a will be referred to as a *current sink*. The configuration of Fig. 5.3-2b will be called a *current source* even though we have used this notation for the general current source of Fig. 5.3-1. These two categories will become important in the practical considerations of implementing current sources/sinks. A third category is the *floating current source*, where neither terminal is connected to V_P or V_N.
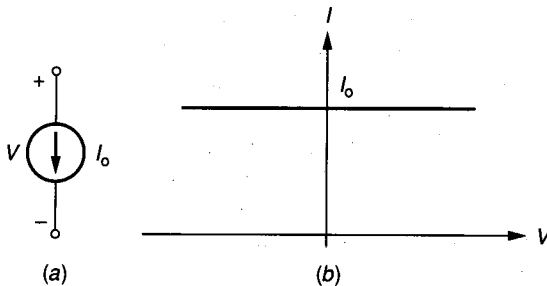

FIGURE 5.3-1
(a) Schematic symbol for a current source, (b) *I–V* characteristics of an ideal current source.
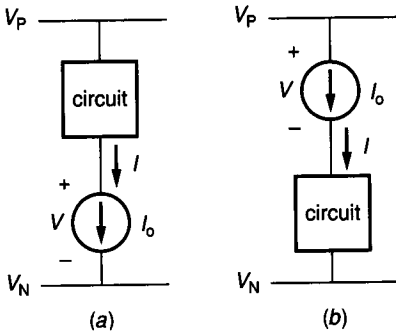
(a)   (b)

FIGURE 5.3-2
(a) A current sink, (b) A current source.

In most current source/sink realizations, the ideal curve of Fig. 5.3-1b is only approximated over a limited range of the voltage V. Also the current is rarely bidirectional. The resulting I–V characteristics of a practical current source/sink realization are shown in Fig. 5.3-3. It is seen that there is a minimum voltage, V_{MIN}, below which the current source/sink will not be a good approximation to I_o. Further, it is seen that even in the region where the current source/sink is a reasonably good approximation to I_o, the actual source/sink deviates by a resistance R_o, which represents the parallel resistance of the current source/sink and ideally is infinite. Thus, the two major aspects by which a current source/sink is characterized are V_{MIN} and R_o.

Figure 5.3-4a shows a BJT realization of a current sink. V_{BB} is a battery used to bias Q1. It follows that for $V > V_{CE}$ (sat) the current value is given by the following relation.

$$I_o = I_S \exp\left(\frac{V_{BB}}{V_t}\right) \tag{5.3-1}$$

V_{CE} (sat) is the collector-emitter voltage where Q1 enters the forward saturation region.
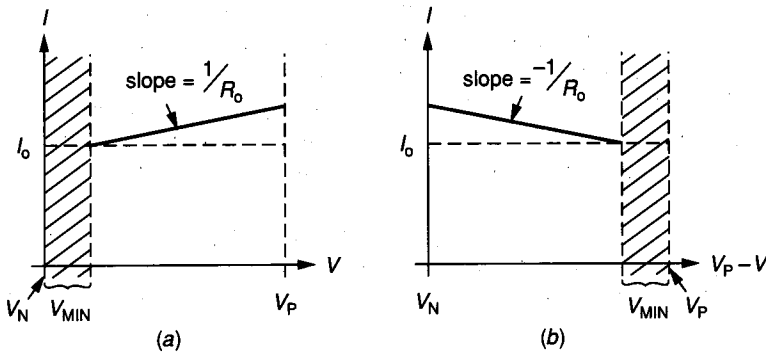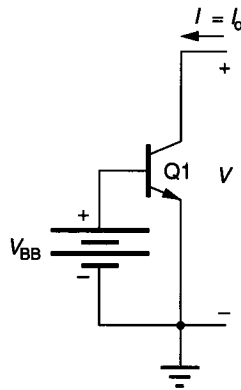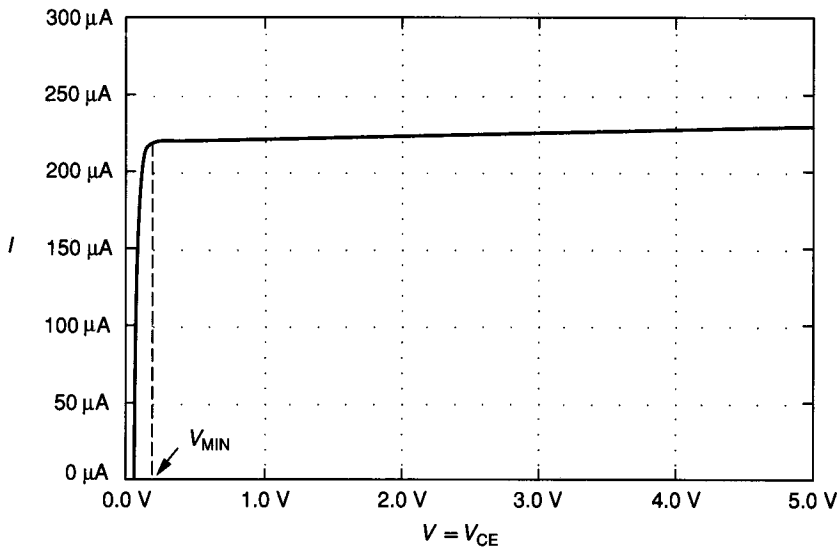

FIGURE 5.3-3
Practical I–V characteristics for: (a) A current sink, (b) A current source.

(a)

(b)

FIGURE 5.3-4
(a) BJT current sink, (b) I–V characteristics of a.

The region from $V = 0$ to $V = V_{MIN}$ corresponds to the forward saturation region of Q1. As a result V_{MIN} is approximated by

$$V_{MIN} \approx V_{CE} \text{ (sat)} \tag{5.3-2}$$

which is normally around 0.2 V (see Table 3.3-2). For $V > V_{MIN}$, the slope of the current is proportional to g_o, where the small signal output conductance is given in Table 3.3-4. Thus, the output resistance of the current sink, R_o, is

$$R_o \approx \frac{1}{g_o} = \frac{V_{AF}}{I_o} \tag{5.3-3}$$

Equations 5.3-1 through 5.3-3 also hold for the current source as characterized by Fig. 5.3-3b.

Figure 5.3-4b shows the I–V characteristics of the circuit of Fig. 5.3-4a with $V_{BE} = 0.7$ V, $I_S = 0.4$ fA, $\beta_F = 100$, and $V_{AF} = 200$ V. With these values V_{MIN} should be approximately 0.2 V, $I_o = 219\ \mu A$, and $R_o = 913$ kΩ for $V_t = 25.9$ mV. A SPICE simulation for the circuit of Fig. 5.3-4b gives $V_{MIN} = 0.2$ V, $I_o = 220\ \mu A$, and $R_o = 889$ kΩ.

Figure 5.3-5a shows a MOS realization of a current sink. From Eq. 3.1-5, if $\lambda = 0$, the value of I_o is given as
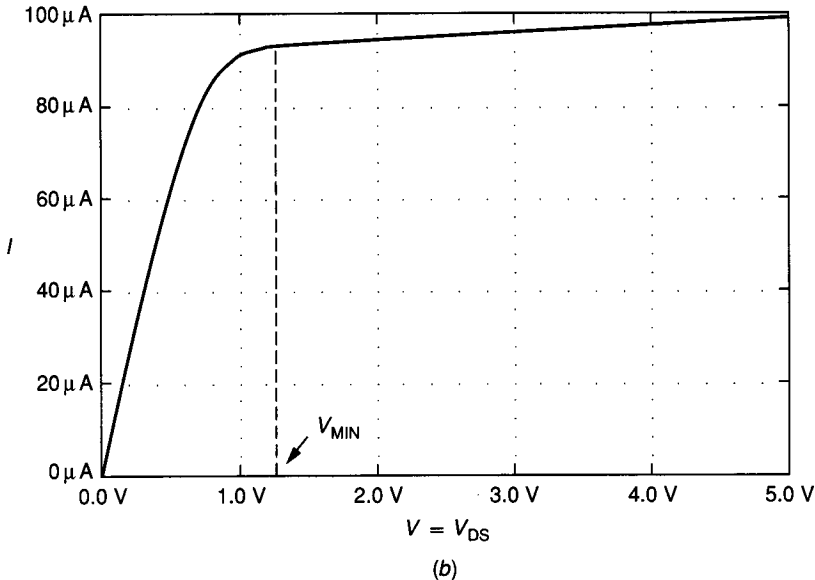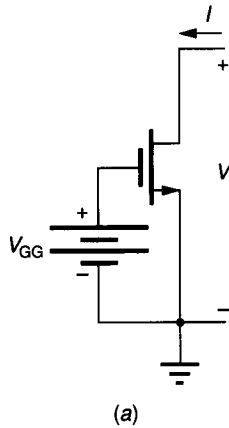
$$I_o = \frac{K_N' W}{2L}(V_{GG} - V_T)^2 \tag{5.3-4}$$

(a)

(b)

FIGURE 5.3-5
(a) MOS current sink, (b) I–V characteristics of a.

The value of V_{MIN} is equal to $V_{DS}(sat)$ and is given in Eq. 3.1-3 as

$$V_{MIN} = V_{GG} - V_T \tag{5.3-5}$$

The output resistance of the current sink for $V > V_{MIN}$ is equal to $1/g_{ds}$ of the small signal model parameters of the MOS (see Table 3.1-3) and is

$$R_o = \frac{1}{g_{ds}} = \frac{1}{\lambda |I_o|} \tag{5.3-6}$$

Equations 5.3-4 through 5.3-6 also hold for the MOS current source using the characterization of Fig. 5.3-3b.

Figure 5.3-5b shows the $I-V$ characteristics of the circuit of Fig. 5.3-5a with $V_{GG} = 2.0$ V, $W = 50\,\mu$, $L = 10\,\mu$, $V_T = 0.75$ V, $K'_N = 24\,\mu$ A/V^2, $\gamma_N = 0.8\,V^{1/2}$, $\lambda = 0.01\,V^{-1}$ and $\phi = 0.6$ V. With these values, $V_{MIN} = 1.25\,V$, $I_o = 94\,\mu A$, and $R_o = 1.064$ MΩ. A SPICE simulation for Fig. 5.3-5b gives $V_{MIN} = 1.2$ V, $I_o = 97\,\mu A$, and $R_o = 1.079$ MΩ.

The BJT and MOS current source/sinks are reasonable approximations of the ideal for limited values of voltage. While the output resistance of both are similar, the BJT has a much smaller value of V_{MIN}. In many cases, the output resistance of the simple BJT or MOS current source/sinks is not sufficiently large. Of course, R_o can be increased by decreasing I_o but other methods exist which allow R_o to be increased without decreasing I_o. Two methods will be investigated. The first uses negative feedback and the second uses positive feedback.

Consider the BJT current sink of Fig. 5.3-6a, which has a resistor R connected between the emitter and ground. The output resistance seen at the terminals across which V is defined will be called R_o. R_o is defined as a ratio of
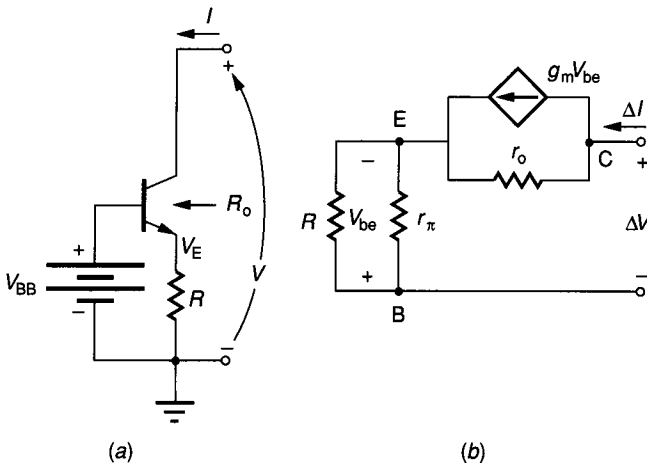

(a)   (b)

FIGURE 5.3-6
(a) Increasing the output resistance of the BJT current source/sink by negative feedback, (b) Small signal model of a.

ΔV over ΔI. Assume that an increase in ΔV causes an increase in ΔI. However, the ΔI increase causes a ΔV_E increase resulting in a ΔV_{BE} decrease. The ΔV_{BE} decrease will cause a decrease in I opposing the assumed increase in ΔI. The feedback is negative series, which will cause the value of R_o to be larger than R_o with $R = 0$ by approximately the value of the feedback loop gain.

The dc current I_0 can be found by iteratively solving the voltage loop equation consisting of V_{BB}, V_{BE}, and the drop across R. The small signal model of the circuit of Fig. 5.3-6a (see Fig. 3.3-8) is shown in Fig. 5.3-6b. ΔV and ΔI are the small signal values of V and I, respectively. Analysis of this circuit gives

$$R_o = \frac{\Delta V}{\Delta I} = r_o[1 + (g_m + g_o)(r_\pi \| R)] \qquad (5.3\text{-}7)$$

If $R = 0$, Eq. 5.3-7 reduces to r_o. The magnitude of the feedback loop gain is given by the second term in the brackets. As R becomes large, Eq. 5.3-7 approaches $r_o(1 + \beta_F)$, which means that the output resistance of the circuit of Fig. 5.3-6a with $R = 0$ can be increased by a factor of up to $1 + \beta_F$ for large values of R.

Figure 5.3-7a shows this principle applied to the MOS current sink. I_o can be found from the large signal model and letting $V_S = I_o R$. In the MOS case, the value of V_{BS} is not zero, so the small signal model is that shown in Fig. 5.3-7b. The output resistance of the circuit of Fig. 5.3-7b is

$$R_o = \frac{\Delta V}{\Delta I} = r_{ds}[1 + (g_m + g_{mb} + g_{ds})R] \approx r_{ds}(1 + g_m R) \qquad (5.3\text{-}8)$$

where $g_m > g_{mb} > g_{ds}$. In the MOS case, the magnitude of the feedback loop gain is $g_m R$ and continues to increase as R increases which helps to compensate for the fact that the g_m in Eq. 5.3-8 is typically less than the g_m in Eq. 5.3-7.
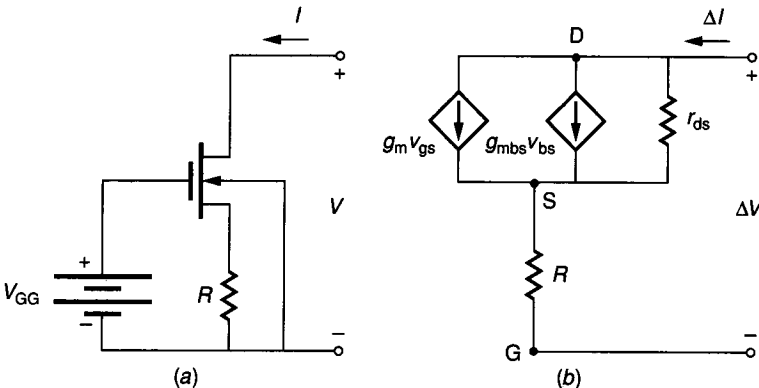

FIGURE 5.3-7
(a) Increasing the output resistance of the MOS current sink by negative feedback, (b) Small signal model of a.
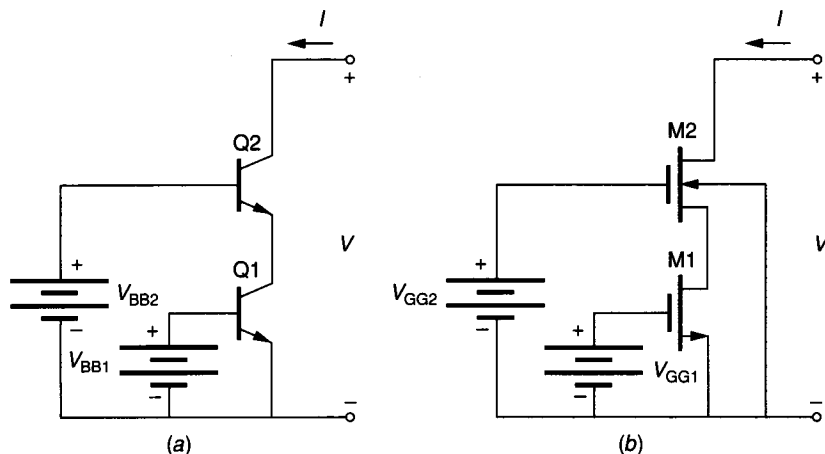
FIGURE 5.3-8
Practical implementation of: (*a*) Fig. 5.3-6*a*, (*b*) Fig. 5.3–7*a*.

An implementation of the circuits of Figs. 5.3-6*a* and 5.3-7*a* is shown in the circuits of Figs. 5.3-8*a* and 5.3-8*b*, respectively. The output current is the same as given in Eqs. 5.3-1 and 5.3-4. The output resistance of the circuit of Fig. 5.3-8*a* can be found by replacing R in Eq. 5.3-7 by the output resistance of Q1, r_o to give

$$R_o = r_{o2}[1 + (g_{m2} + g_{o2})(r_{\pi 2} \| r_{o1})] \qquad (5.3-9)$$

Similarly, Eq. 5.3-8 can be used to find the output resistance of the circuit of Fig. 5.3-8*b* resulting in

$$R_o = r_{ds2}[1 + (g_{m2} + g_{mb2} + g_{ds2})r_{ds1}] \qquad (5.3-10)$$

Assuming that Q1 and Q2 of Fig. 5.3-8*a* are identical to the BJT used in Fig. 5.3-4*b*, we find that $g_{m2} = 8.456$ mS, $r_{o1} = r_{o2} = 913$ kΩ, and $r_{\pi 2} = 11.826$ kΩ. Substituting into Eq. 5.3-9 gives an output resistance of 91.05 MΩ. The increase of R_o from 0.913 MΩ to 91.05 MΩ is an increase of almost $1 + \beta_F$. Assuming that M1 and M2 of Fig. 5.3-8*b* are identical with the MOS device used in Fig. 5.3-5*a* gives a $g_{m2} = 152.6 \mu$S and $g_{ds1} = g_{ds2} = 0.97 \mu$S ignoring for the moment g_{mb2}. Substituting these values into Eq. 5.3-10 and neglecting g_{mb2} gives an output resistance of 171.9 MΩ.

While the values of R_o have been significantly increased for both the BJT and MOSFET current source/sinks, the value of V_{MIN} has also been increased. The design of V_{BB2} in Fig. 5.3-8*a* or V_{GG2} in Fig. 5.3-8*b* is crucial to achieving the minimum value of V_{MIN}. Fig. 5.3-9*a* shows the circuit of Fig. 5.3-8*a* biased for the minimum value of V_{MIN} which is equal to $2V_{CE}(\text{sat})$. Therefore, if both transistors are identical, then $V_{BE1} = V_{BE2}$ will give the same current assuming large β_F. Thus V_{BB2} should be designed to equal
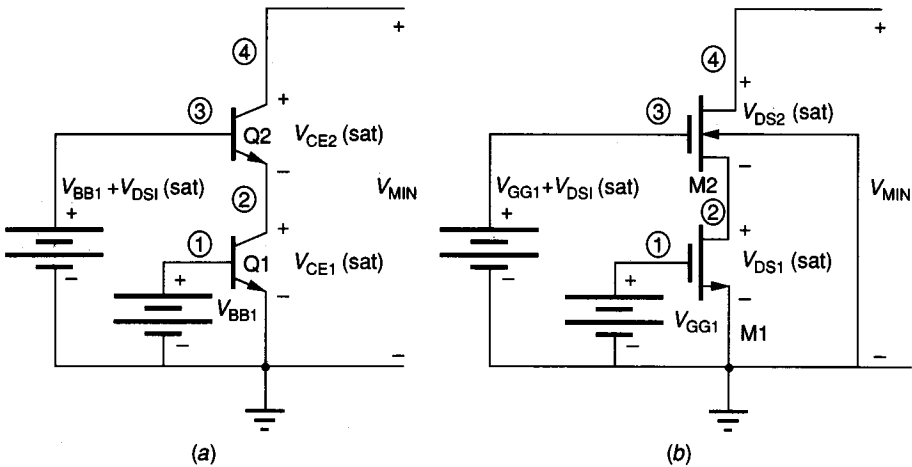
FIGURE 5.3-9
Minimum V_{MIN} design of: (a) Fig. 5.3-8a, (b) Fig. 5.3-8b.

$$V_{BB2} = V_{CE1}(\text{sat}) + V_{BB1} \qquad (5.3\text{-}11)$$

to achieve the minimum value of V_{MIN}. A similar consideration holds for the MOSFETs of Fig. 5.3-8b, which are redrawn in Fig. 5.3-9b. In this analysis we must include the effects of the bulk–source voltage on M2. To have the same current in both M2 and M1 implies that the following relationship must be true

$$V_{GS1} - V_{T1} = V_{GS2} - V_{T2} \qquad (5.3\text{-}12)$$

Therefore V_{GG2} of Fig. 5.3-8b is

$$V_{GG2} = V_{DS1}(\text{sat}) + V_{GS2} = V_{DS1}(\text{sat}) + V_{GG1} - V_{T1} + V_{T2} \qquad (5.3\text{-}13)$$

With this value of V_{GG2} the minimum value of V_{MIN} will be $2(V_{GG1} - V_{T1})$.

Figures 5.3-10a and b are the results of SPICE simulation of the circuits of Figs. 5.3-9a and b using the same model parameters as for the previous simulation and with $V_{BB2} = 0.4$ V and $V_{GG2} = (1.25 + 2.0 - 0.75 + 1.218) = 3.718$ V. It is seen that V_{MIN} for the BJT current sink of Fig. 5.3-9a is approximately 0.4 V. The output resistance is too large to be determined with any accuracy from the plots of Fig. 5.3-10a and b. Figure 5.3-10b shows that V_{MIN} for the MOS current sink of Fig. 5.3-9b is about 1.8 V. The advantage of BJTs over MOSFETs with regard to signal swing is very apparent in the circuits studied above.

The second method of increasing the value of R_o of a simple current source/sink uses positive feedback. Figure 5.3-11a shows the concept of this technique. I_o and R_o represent the current source or sink of Figs. 5.3-4a or 5.3-5a. The amplifier A of Fig. 5.3-11a is an ideal voltage-controlled, voltage source controlled by V. The battery V_o is used to permit a dc voltage drop across the
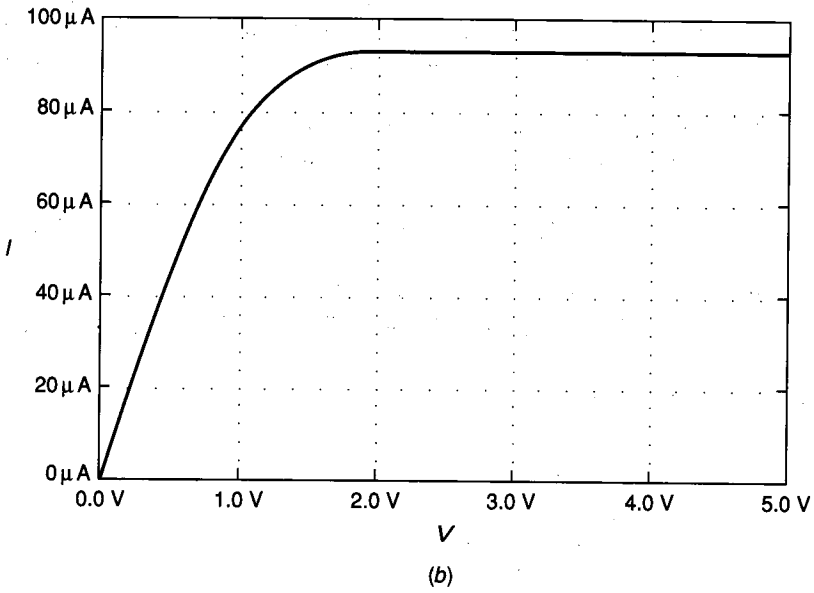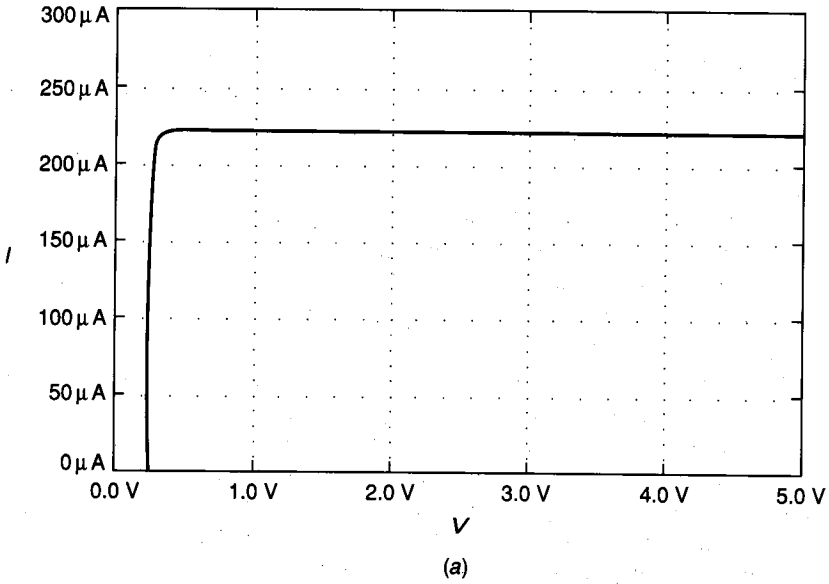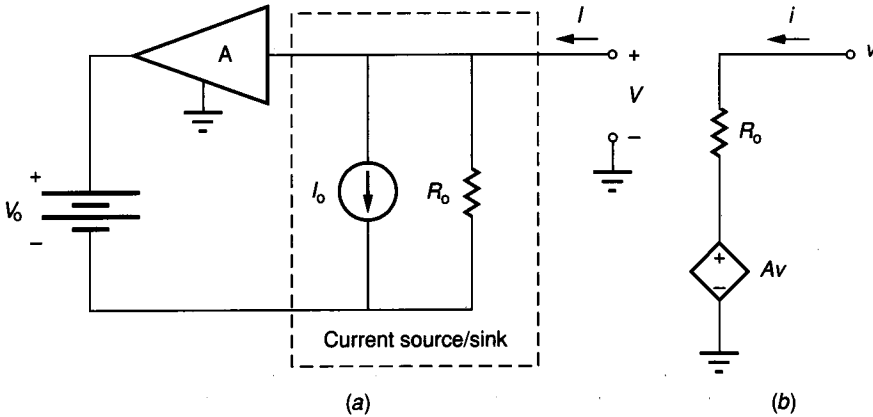
(a)

(b)

FIGURE 5.3-10
Simulation of: (a) Fig. 5.3-9a (b) Fig. 5.3-9b.

FIGURE 5.3-11
(a) Concept of using positive feedback to increase R_0, (b) ac model of a.

current sink/source. Figure 5.3-11b shows the ac model of the circuit of Fig. 5.3-11a. The output resistance can easily be found as

$$R_{\text{out}} = \frac{v}{i} = \frac{R_0}{1 - A} \qquad (5.3\text{-}14)$$

If A is slightly less than unity then $(1 - A)^{-1}$ is a large number causing R_{out} to be much greater than R_0. This technique is called *bootstrapping* and has many uses.

   While this technique works better with depletion devices (e.g., can make V_0 in Fig. 5.3-11a with a depletion device), we shall first show how to apply bootstrapping to BJT and enhancement MOS transistors. Figure 5.3-12a shows how the current source of Fig. 5.3-4a can be bootstrapped by Q2. Because the ac voltage gain from the base of Q2 to the emitter of Q2 is always less than one, then the ac voltage at the emitter of Q1 follows the ac voltage at the collector of Q1. Consequently, there is very little ac change in voltage from the collector to emitter of Q1 thus boosting the output resistance value. The resistor R is necessary to allow the emitter of Q1 to follow its collector. Note that as the voltage V changes that all of this change is across R, and the current necessary to create this voltage comes from Q2. I_0 is approximately equal to I_1.

   The value of V_{EE2} can be zero without influencing the circuit because Q1 is in the forward active region when $V_{\text{CE1}} = V_{\text{BE2}}$. Unfortunately, the resistance R keeps the bootstrapped current sink from having a low V_{MIN}. As V_{CE1} approaches V_{CE1} (sat), Q2 turns off. The voltage across R will be $I_1R = IR$ until Q1 goes into saturation. As a result

$$V_{\text{MIN}} = V_{\text{CE}}(\text{sat}) + I_0R \qquad (5.3\text{-}15)$$

If R is small and V_{EE2} negative ($V_{\text{CE1}}(\text{sat}) - V_{\text{BE2}}$), a very low value of V_{MIN} with high R_0 could be achieved.

Figure 5.3-12*b* gives the small signal model of Fig. 5.3-12*a* where the $g_{m2}v_{be2}$ has been simplified by source reduction. From this model the ac output resistance can be calculated as

$$R_o = \frac{v}{i} = \frac{r_{\pi 2} \| r_{o1} + 1/g_{m2} \| R}{1 - g_{m2}R/(1 + g_{m2}R)} = \left[r_{\pi 2} \| r_{o1} + \frac{1}{g_{m2}} \| R \right][1 + g_{m2}R]$$

$$(5.3\text{-}16)$$

Unfortunately, $r_{\pi 2}$ tends to work against obtaining large values of ac output resistance using the BJT bootstrapped current sink.

Figure 5.3-13*a* shows a MOS implementation of the bootstrapped current sink. The MOS version does not suffer the $r_{\pi 2}$ effects of the BJT version. The minimum value of V_{MIN} is given as

$$V_{\text{MIN}} = V_{\text{DS1}}(\text{sat.}) + I R \qquad (5.3\text{-}17)$$

and is achievable only when $V_{\text{SS2}} < V_{\text{DS1}}(\text{sat.}) - V_{\text{T2}}$. The bulk-source influence in M1 and M2 must also be considered in the design of Fig. 5.3-13*a*. The small signal model of the MOS bootstrapped current sink in Fig. 5.3-13*b* can be used to find the output resistance given as

$$R_o = \frac{v}{i} = \left[\frac{r_{\text{ds1}} + 1/g_m \| R}{1 - g_{m2}R/(1 + g_{m2}R)} \right] = \left(r_{\text{ds1}} + \frac{1}{g_{m2}} \| R \right)(1 + g_{m2}R) \quad (5.3\text{-}18)$$

It can be seen that the value of R_o of Fig. 5.3-5*a* can be increased by approximately $(1 + g_{m2}R)$.
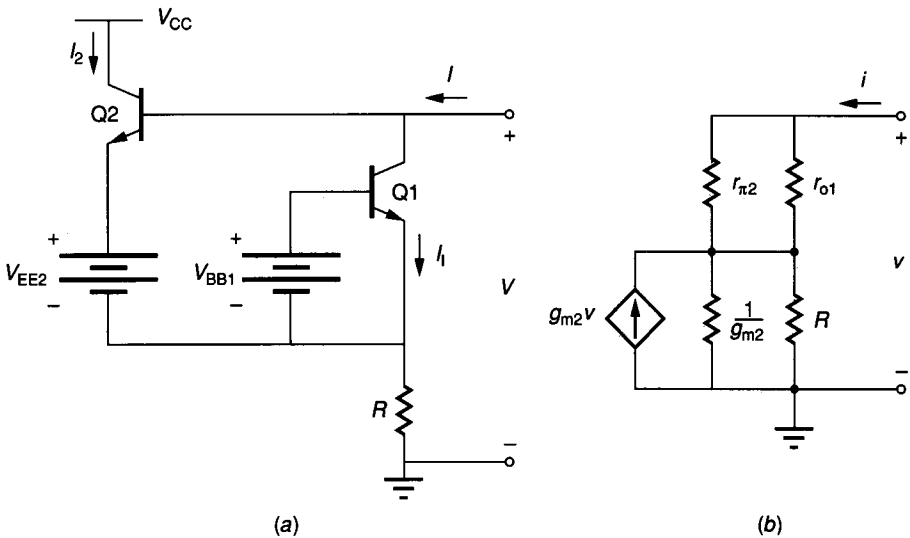

(a)   (b)

FIGURE 5.3-12
(*a*) BJT bootstrapped current sink, (*b*) ac model of *a*.
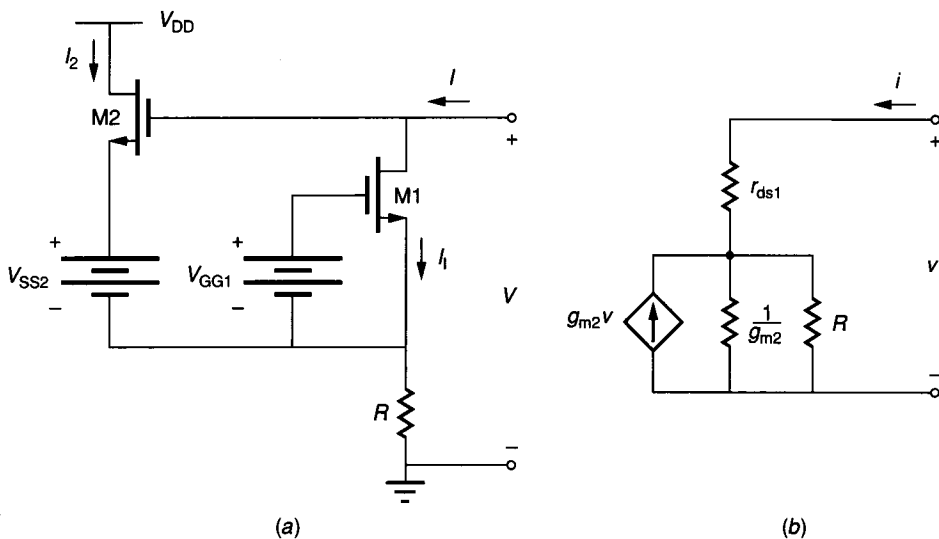
FIGURE 5.3-13
(a) MOS bootstrapped current sink, (b) ac model of a.

For depletion devices the dc polarity of V_{DS} and V_{GS} can be opposite. Examples are the depletion-mode MOSFET, the JFET, and the GaAs MESFET. Let us consider the n-channel depletion MOSFET as an example. Figure 5.3-14a shows that a depletion MOSFET current sink can be obtained by simply connecting the gate to the source. The I–V characteristics are shown in Fig. 5.3-14b, where V_T is the pinch-off voltage and I_o is the drain-source current with $V_{GS} = 0$. The bootstrapping principle can be applied to the depletion MOSFET very conveniently, as shown in Fig. 5.3-15a. In this circuit, M2 bootstraps the channel resistance r_{ds1} of M1, causing the output resistance

FIGURE 5.3-14
(a) n-channel, JFET current sink, (b) I–V characteristics of a.

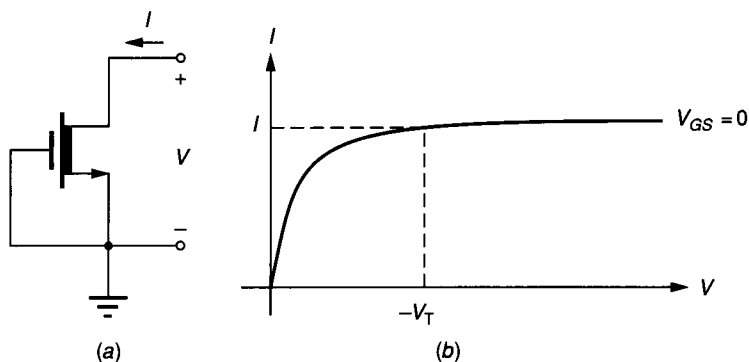of this current source to be increased. Fig. 5.3-15*b* gives the small signal model of Fig. 5.3-15*a*. The small signal output resistance is given as

$$R_o = \frac{v}{i} = \frac{r_{ds1} + (1/g_{m2}) \parallel r_{ds2}}{1 - (g_{m2}r_{ds2})/(1 + g_{m2}r_{ds2})} = \left(r_{ds1} + \frac{1}{g_{m2}}\right) \parallel r_{ds2})(1 + g_{m2}r_{ds2})$$

(5.3-19)

Unfortunately, the minimum value of V_{MIN} is not small and is at least equal to $\mid V_T \mid$. Without the flexibility of bias voltages, the geometries of M1 and M2 will have to be adjusted to account for the fact that $V_{GS1} \neq V_{GS2}$.

A MOS current source/sink that outperforms any of the previous current source/sinks considered so far in the area of high R_o and low V_{MIN} is shown in Fig. 5.3-16*a*[3] and is called a *regulated cascode current sink*. The output current is given by Eq. 5.3-4. The ac output resistance of M1 can be increased by stabilizing its drain-source voltage. In the regulated cascode current sink, the gate voltage of M2, which is the same as the drain-source voltage of M1, is regulated by a feedback loop consisting of M2 and M4 as an amplifier and M3 as a voltage follower. If all transistors operate in saturation and if the bulk effects are ignored, the ac output resistance can be found as

$$R_o \simeq r_{ds1}\left(\frac{g_{m2}g_{m3}}{g_{ds3}(g_{ds2} + g_4)}\right)$$

(5.3-20)

where g_4 is the output conductance of the I_4 current source. It is seen that the output resistance is higher than any MOS circuit considered so far. If $I_4 = 2$ μA, and $I = 94$ μA; then $g_1 = 0.02$ μS, $g_{d2} = 0.02$ μS, $g_{m2} = 21.9$ μS, r_{ds1}
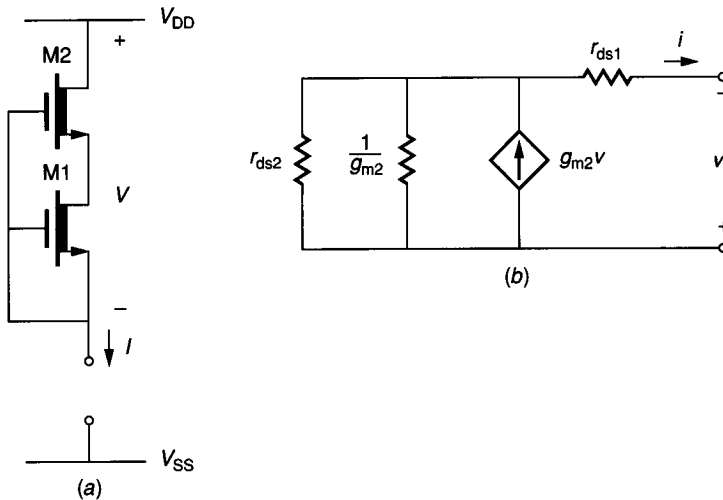
FIGURE 5.3-15
(*a*) Bootstrapped JFET current source, (*b*) Small signal model of *a*.
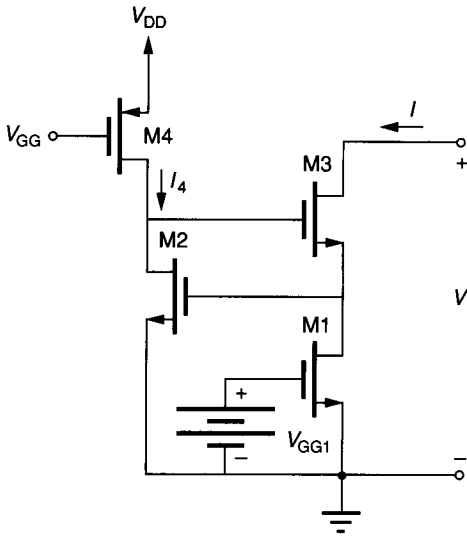
(a)
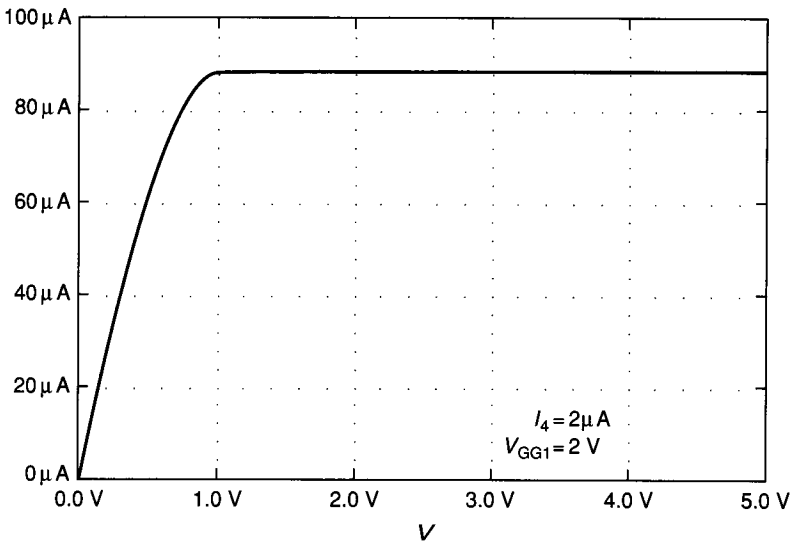
(b)

FIGURE 5.3-16
(a) Regulated cascode current sink, (b) Simulation results of Fig. 5.3-16a.

$= 1.064 \ M\Omega$, $g_{m3} = 150.2 \ \mu S$, and $g_{ds3} = 0.94 \ \mu S$. Thus, the calculated value of R_o is 93.08 GΩ!

The circuit of Fig. 5.3-16a even works with a somewhat reduced R_o performance when the drain–source voltage across M3 is lowered to the point where it starts to operate in the ohmic region. The gate voltage of M3 may be driven by the feedback loop almost up to V_{DD}, causing the V_{DS} drop across M3 to stay

small. Thus, the minimum value of V_{MIN} is given approximately by V_{GS2} and is written as

$$V_{MIN} = V_{GS2} = \sqrt{\frac{2I_1 L_2}{K_N' W_2}} + V_{T2} \qquad (5.3\text{-}21)$$

Figure 5.3-16b is a simulated output of the circuit of Fig. 5.3-16a when $I_1 = 2$ μA and all transistors are identical with $W = 50$ μ and $L = 10$ μ using the model parameters previously employed. For the conditions stated above, the minimum value of V_{MIN} is 0.93 V. The current of Fig. 5.3-16b is slightly less than the anticipated 94 μA because the value of V_{GS2}, 0.93 V, is less than the 1.25 V required to keep M1 in saturation. Using Eq. 3 of Table 3.1-1 gives $I_o = 87.6\mu$A, which matches well with Fig. 5.3-16b. Similar considerations could be used to develop a high-performance BJT current-sink.

In this section, we have examined methods of implementing current source/sinks. It was seen that a current source/sink can be characterized by its current, small signal output resistance, R_o, and its minimum voltage drop, V_{MIN}. It was shown how negative and positive feedback could be used to increase the value of R_o. Because these techniques increased V_{MIN} it was necessary to consider how to minimize this characteristic. Methods of implementing the bias supplies will be considered in the next several sections. A regulated cascode MOS current sink was introduced that had superior performance to all previous MOS current sink realizations. A comparison of the various current sinks considered in this section is given in Table 5.3-1. The current sources have similar characteristics.

TABLE 5.3-1
Comparison of current sinks

Current sink	Figure	R_O	Minimum V_{MIN}
Simple BJT	5.3-4a	$\dfrac{V_{AF}}{I_o}$	$V_{CE}(sat)$
Simple MOS	5.3-5a	$r_o = \dfrac{1}{\lambda I_o}$	$V_{GG1} - V_T$
Cascade BJT	5.3-9a	$r_{o2}[1 + g_{m2}(r_{\pi 2} \| r_{o1})]$	$2V_{CE}(sat)$
Cascade MOS	5.3-9b	$r_{ds2}[1 + (g_{m2} + g_{mbs2})r_{ds1}]$	$2(V_{GG1} - V_{T1})$
Bootstrapped BJT	5.3-12a	$\left[(r_{\pi 2} \| r_{o1}) + \left(\dfrac{1}{g_{m2}}\middle\| R\right)\right](1 + g_{m2}R)$	$V_{CE}(sat) + I_o R$
Bootstrapped MOS	5.3-13a	$\left(r_{ds1} + \dfrac{1}{g_{ms1}}\middle\| R\right)(1 + g_{m2}R)$	$V_{DS}(sat) + I_o R$
Regulated cascoded	5.3-16a	$r_{ds1}\left(\dfrac{g_{m2}g_{m3}}{g_{ds3}(g_{ds2} + g_4)}\right)$	$\sqrt{\dfrac{2I_1 L_2}{K_N' W_2}} + V_{T4}$

5.4 CURRENT MIRRORS/AMPLIFIERS

In the previous section we considered the subject of current sources and sinks where the objective was to implement the ideal I–V characteristics of Fig. 5.3-1b. A dc voltage source was used to bias the implementation of the current sources or sinks. This section considers similar circuits, with the exception that the current source or sink is biased by a dc current rather than a dc voltage.

The circuits of this section are distinct from those of the last in that they use the principle of matched devices. This section will begin by applying the principle of matched devices to bipolar and then to MOSFET circuits resulting in current mirrors/amplifiers. It will also be shown how to analyze so-called matched circuits when they are not matched. Because the matching principle is much like looking into a mirror, the circuits of this section are called *current mirrors*. The term *current amplifier* is also used for current mirrors when an input current change creates an output current change.

One of the advantages of integrated circuits over discrete components is the ability to practically match components without trimming. This matching feature is used in this section to provide a very versatile and useful block called the current mirror. Before considering the current mirror, let us introduce the principles of matched devices. Consider initially two npn bipolar junction transistors. If the Early voltage effects are neglected, it follows from Eq. 3.3-13 that the large signal collector currents in the active region with the base-emitter junction forward-biased and the base-collector junction reverse-biased are given as

$$I_{C1} = I_{S1}\exp\left(\frac{V_{BE1}}{V_t}\right) = I_{S1}\exp\left(\frac{qV_{BE1}}{kT}\right) \tag{5.4-1}$$

and

$$I_{C2} = I_{S2}\exp\left(\frac{V_{BE2}}{V_t}\right) = I_{S2}\exp\left(\frac{qV_{BE2}}{kT}\right) \tag{5.4-2}$$

where from Eq. 3.3-6 and Eq. 3.3-7 of Chapter 3,

$$I_{Si} = \frac{qn_i^2\overline{D_n}A_i}{Q_{Bi}(V_{CBi})} \, , \, i = 1, 2 \tag{5.4-3}$$

The parameters of Eq. 5.4-3 have been defined in Chapter 3. Solving for V_{BE1} and V_{BE2} gives

$$V_{BE1} = V_t \ln\left(\frac{I_{C1}}{I_{S1}}\right) \tag{5.4-4}$$

and

$$V_{BE2} = V_t \ln\left(\frac{I_{C2}}{I_{S2}}\right) \tag{5.4-5}$$

Now if the base and emitter of Q1 are connected to the base and emitter of Q2 and a source of base current exists, then the following relationship between I_{C1} and I_{C2} results.

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} = \frac{qn_i^2\overline{D_n}A_1}{Q_{B1}(V_{CB1})} \times \frac{Q_{B2}(V_{CB2})}{qn_i^2\overline{D_n}A_2} = \frac{A_1 Q_{B2}(V_{CB2})}{A_2 Q_{B1}(V_{CB1})} \qquad (5.4\text{-}6)$$

If the transistors are matched and if $V_{CB1} = V_{CB2}$, $A_1 = A_2$ and $Q_{B1} = Q_{B2}$, then $I_{C1} = I_{C2}$, which illustrates the principle of matched devices. This principle is very important and will be used both in biasing and small signal design of integrated circuits.

The application of the matching principle to implement a simple bipolar current sink is shown in Fig. 5.4-1. In this circuit, the base and the collector of Q1 are physically connected together for two reasons. The first is to provide a source of base current for both Q1 and Q2. The second is to keep V_{CE1} small so that R_1 essentially defines the current I_{IN}. The reader can note that V_{CC}, R_1 and the base-collector connected transistor Q1 actually implement V_{BB} of the current sink of Fig. 5.3-4a.

The above results will now be used to calculate the ratio of I_{C2} to I_{IN}. Initially, the emitter areas of Q1 and Q2 will be assumed to be equal and the Early voltage will be neglected so that differences in V_{CB1} and V_{CB2} can be ignored. If the bases of Q1 and Q2 and the emitters of Q1 and Q2 are physically connected together, then the matching principle gives

$$I_{C2} = I_{C1} \qquad (5.4\text{-}7)$$

However,

$$I_{C1} = I_{IN} - I_{B1} - I_{B2} \qquad (5.4\text{-}8)$$

and

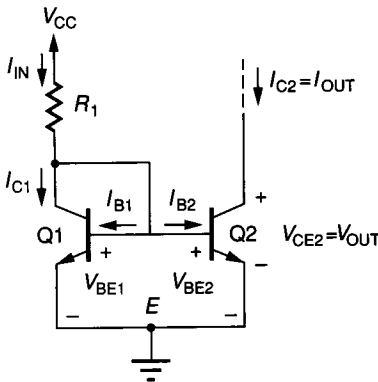$$I_{IN} = \frac{V_{CC} - V_{BE1}}{R_1} \qquad (5.4\text{-}9)$$

FIGURE 5.4-1
A simple bipolar current mirror.

Using the relationship, $I_C = \beta_F I_B$ and assuming $I_{B1} = I_{B2} = I_B$ and $B_{F1} = B_{F2} = B_F$, gives

$$I_{C2} = \frac{I_{IN}}{1 + (2/\beta_F)} = \frac{V_{CC} - V_{BE1}}{R_1[1 + (2/\beta_F)]} \qquad (5.4\text{-}10)$$

It should be noted that as β_F approaches infinity, I_{C2} approaches I_{IN}.

In the considerations above, the Early voltage was neglected which turns out to be a poor assumption in some applications. If the Early voltage, V_{AF} is included in the large signal expressions for the collector current, Equations 5.4-1 and 5.4-2 are modified as

$$I_C = I_S\left(1 + \frac{V_{CE}}{V_{AF}}\right)\exp\left(\frac{V_{BE}}{V_t}\right) \qquad (5.4\text{-}11)$$

Using the matched transistor principle, we can solve for the ratio of I_{C2} to I_{C1} as

$$\frac{I_{C2}}{I_{C1}} = \frac{I_{S2}[1 + (V_{CE2}/V_{AF})]}{I_{S1}[1 + (V_{CE1}/V_{AF})]} = \frac{1 + (V_{CE2}/V_{AF})}{1 + (V_{CE1}/V_{AF})} = \frac{1 + (V_{CE2}/V_{AF})}{1 + (V_{BE1}/V_{AF})} \qquad (5.4\text{-}12)$$

Note that even though the transistors are matched, I_{C2} is not necessarily equal to I_{C1}. As an example, assume that $V_{CE2} = 10$ V, $V_{BE1} = 0.6$ V and $V_{AF} = 100$ V. The ratio of I_{C2} to I_{C1} is 1.093. It should be apparent that the Early voltage effects cannot be neglected in some practical applications. Although a 9% error is somewhat discouraging, alternative configurations will be developed which significantly reduce this error in matched devices.

Before developing the configurations which eliminate the Early voltage effects, let us consider what happens if the transistors are not exactly matched. Assume that A, Q_B and $\alpha_F(=\beta_F/(1 + \beta_F))$ are not matched and are given by

$$A_1 = A + (\Delta A/2) \qquad (5.4\text{-}13)$$

$$A_2 = A - (\Delta A/2) \qquad (5.4\text{-}14)$$

$$Q_{B1} = Q_B + (\Delta Q_B/2) \qquad (5.4\text{-}15)$$

$$Q_{B2} = Q_B - (\Delta Q_B/2) \qquad (5.4\text{-}16)$$

$$\alpha_{F1} = \alpha_F + (\Delta\alpha_F/2) \qquad (5.4\text{-}17)$$

and

$$\alpha_{F2} = \alpha_F - (\Delta\alpha_F/2) \qquad (5.4\text{-}18)$$

where A, Q_B and α_F are the nominal values and corresponding parameters ΔA, ΔQ_B and $\Delta\alpha_F$ are the differences between the two values. I_{C1} may be expressed from Eq. 5.4-8 and Eq. 3.3-12 as

$$I_{C1} = \alpha_{F1}I_{IN} - \frac{\alpha_{F1}}{\beta_{F2}}I_{C2} \qquad (5.4\text{-}19)$$

Substituting Eq. 5.4-19 into Eq. 5.4-6 with $V_{CB1} = V_{CB2}$ results in

$$I_{C2} = \frac{(A_2 Q_{B1}/A_1 Q_{B2})\alpha_{F1}}{1 + (\alpha_{F1}A_2 Q_{B1}/\beta_{F2}A_1 Q_{B2})}I_{IN} \approx \left(\frac{A_2 Q_{B1}}{A_1 Q_{B2}}\right)\alpha_{F1}\alpha_{F2}I_{IN} \qquad (5.4\text{-}20)$$

where it has been assumed that

$$\frac{\alpha_{F1} A_2 Q_{B1}}{A_1 Q_{B2}} \approx 1 \tag{5.4-21}$$

Substituting Eqs. 5.4-13 through 5.4-18 into Eq. 5.4-20 results in

$$I_{C2} = I_{IN} \left[\frac{(1 - \Delta A/2A)(1 + \Delta Q_B/2Q_B)(1 + \Delta \alpha_F/2\alpha_F)(1 - \Delta \alpha_F/2\alpha_F)}{(1 + \Delta A/2A)(1 - \Delta Q_B/2Q_B)} \right] \tag{5.4-22}$$

which can be approximated for small ΔA, ΔQ_B and $\Delta \alpha_F$ by,

$$I_{C2} \cong I_{IN} \left[1 - \frac{\Delta A}{A} + \frac{\Delta Q_B}{Q_B} + \frac{\Delta \alpha_F}{\alpha_F} \right] \tag{5.4-23}$$

It can be shown that

$$\frac{\Delta I_S}{I_S} \cong \frac{\Delta A}{A} - \frac{\Delta Q_B}{A_B} \tag{5.4-24}$$

so that Eq. 5.4-23 can be written as

$$I_{C2} \cong I_{IN} \left[1 - \frac{\Delta I_S}{I_S} + \frac{\Delta \alpha_F}{\alpha_F} \right] \tag{5.4-25}$$

If a 5% mismatch for I_S and a 10% mismatch for β_F (which is a 0.1% mismatch in α_F for $\beta_F = 100$) is assumed, then Eq. 5.4-25 shows that the variation for the ratio of I_{C2} to I_{IN} is 0.949 to 1.051, or about $\pm 5\%$.

The simulated performance of the simple BJT current mirror is shown in Fig. 5.4-2. The transistors have been assumed to be equal and have the model parameters of $\beta_F = 200$, $\beta_R = 0.43$, $I_S = 0.4$ fA, $V_{AF} = 200$ V and $V_{AR} = 20$ V. An ideal current mirror would have horizontal curves whose value of $I_{C2}(I_{OUT})$ would be exactly equal to $I_{C1}(I_{IN})$ independent of V_{OUT}. As in the previous section, a measure of the "horizontalness" of the curves is given by the small signal resistance or conductance looking back into Q2 from the collector to ground. We shall designate this resistance or conductance as r_{out} or g_{out}. In the circuit of Fig. 5.4-1, r_{out} is simply r_{o2} which was derived in Chapter 3 as

$$r_{out} = r_{o2} = \frac{V_{AF}}{I_{C2}} \tag{5.4-26}$$

The small signal output resistance of the current mirror will be important in determining its performance.

When β_F is not large it can cause current ratio errors which may total a few percent, as indicated in Eq. 5.4-10. Since β_F is not accurately controlled at processing, the β_F effects are unacceptably large in some applications. Figure 5.4-3 shows a configuration which reduces the effect of β_F upon the current ratio of Q1 and Q2. Transistor Q3 requires less current by a factor of β_F from I_{IN} in order to provide the base currents for Q1 and Q2. Neglecting mismatch effects and Early voltage effects, it can be shown that
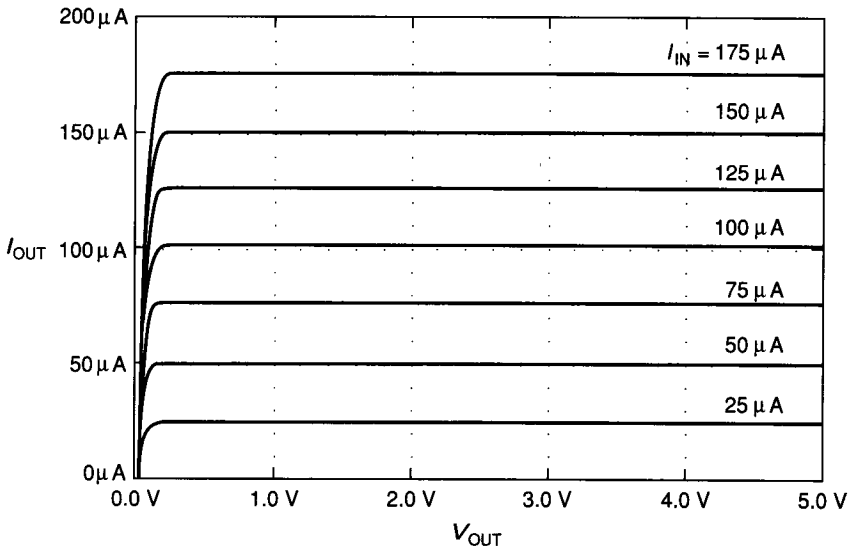
FIGURE 5.4-2
$I-V$ characteristics of the simple bipolar current mirror of Fig. 5.4-1.

$$I_{C2} = \frac{I_{IN}}{1 + 2/[\beta_F(1 + \beta_F)]} \qquad (5.4\text{-}27)$$

Comparing Eqs. 5.4-10 and 5.4-27 shows that the transistor Q3 has reduced the β_F effects by about a factor of β_F, which is quite significant. It is also observed that two base-emitter drops rather than the single drop in Eq. 5.4-9 are subtracted from V_{CC} to find the voltage drop across R_1 which determines I_{IN}. This implies that for small values of V_{CC}, I_{IN} will be less well defined in the circuit of Fig. 5.4-3 than it was in the circuit of Fig. 5.4-1.
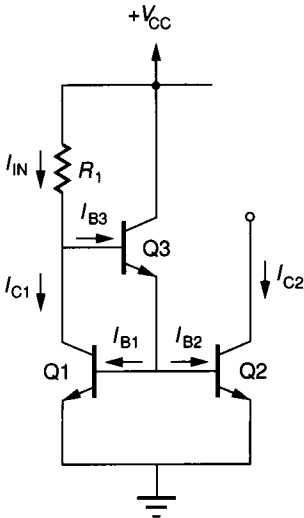

FIGURE 5.4-3
A circuit reducing the influence of β_F on the current mirror of Fig. 5.4-1.
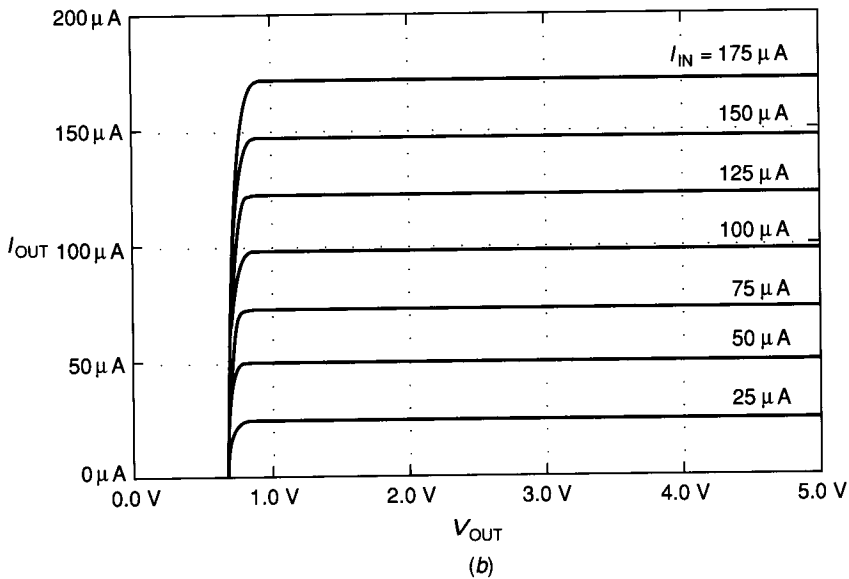
(a)

(b)
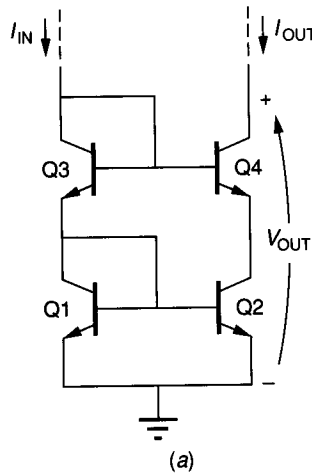
FIGURE 5.4-4
(a) Bipolar cascode current mirror, (b) Simulated performance of the BJT cascode current mirror.

Two methods of reducing Early voltage effects will now be considered. One is to constrain V_{CE1} and V_{CE2} of Fig. 5.4-1 to be equal, and the other uses negative feedback. The first method is illustrated by the cascode current mirror shown in Fig. 5.4-4a. Since the value of V_{BE3} is approximately equal to V_{BE4}, then V_{CE1} (V_{BE1}) is approximately equal to V_{CE2}, thereby eliminating the Early effect from Eq. 5.4-12. Although the effect of the Early voltage has been eliminated on the ratio of I_{C2} to I_{C1} of the cascode current mirror, one may ask about the effect of the Early voltage on Q4. Fortunately, Q4 is operating with
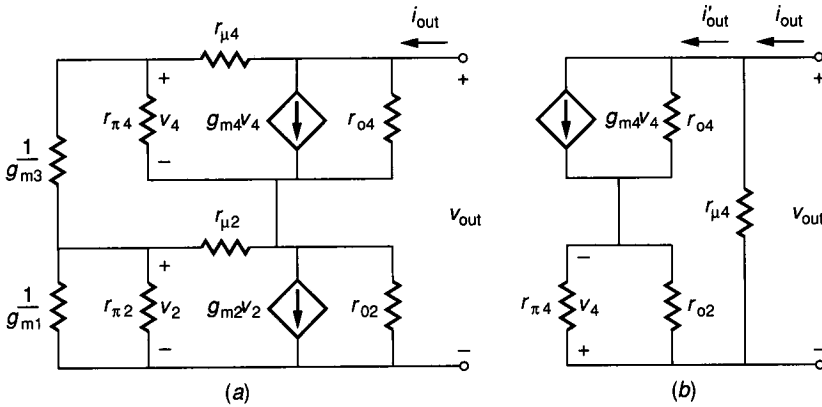
FIGURE 5.4-5
(a) Small signal model of Fig. 5.4-4a, (b) Simplified small signal model of a.

the base terminal at ac ground, which reduces the effect of the Early voltage by about a factor of β_F. The $I-V$ characteristics of the cascode current mirror are shown in Fig. 5.4-4b. The improvement of the cascode current mirror over the simple current mirror can be quantified by comparing the ac output impedances of the two circuits. The small signal model for the cascode current mirror is shown in Fig. 5.4-5a, where the frequency-independent, hybrid-pi model of Fig. 3.3-12 and the assumption that $(1/g_{m1})$ and $(1/g_{m3})$ are much less than $r_{\pi2}$ or $r_{\pi4}$ have been used. A simplified form of this model is shown in Fig. 5.4-5b. The small signal output resistance can be found by noting that

$$i'_{out} = g_{m4}v_4 + (v_{out} + v_4)/r_{o4} \tag{5.4-28}$$

and

$$v_4 = -i_{out}(r_{\pi4} \parallel r_{o2}) = -i_{out}\frac{r_{o2}}{1 + g_{m4}r_{o2}/\beta_{F4}} \tag{5.4-29}$$

Substituting Eq. 5.4-29 into 5.4-28 gives

$$\frac{v_{out}}{i'_{out}} = r_{o4}\left[1 + \frac{r_{o2}(1 + g_{m4}r_{o4})}{r_{o4}[1 + (g_{m4}r_{o2}/\beta_{F4})]}\right] \tag{5.4-30}$$

Finally, the small signal output resistance is found by combining the resistance represented by Eq. 5.4-30 and $r_{\mu4}$ in parallel to give

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{\mu4} \parallel r_{o4}\left[1 + \frac{r_{o2}(1 + g_{m4}r_{o4})}{r_{o4}[1 + (g_{m4}r_{o2}/\beta_{F4})]}\right] \cong \beta_{F4}r_{o4} \tag{5.4-31}$$

We see that the cascode current mirror does indeed have a small signal resistance, which is approximately β_F times the small signal resistance of the simple current mirror.

The emitter areas of Q1 and Q2 should be as large as possible for best matching. All other transistors can have minimum area.

A second method of increasing the small signal output resistance uses negative feedback and is shown in Fig. 5.4-6a. This circuit is called the Wilson current mirror.[4] The Wilson current mirror uses negative current-shunt feedback to stabilize the ratio of I_{C3} to I_{IN} and to increase r_{out}. The operation of the circuit is explained by assuming that I_{IN} is constant and that an incremental increase in V_{CE3} causes an increase in I_{C3}. This increase in I_{C3} causes V_{BE3} and V_{BE1} to increase. The V_{BE1} increase causes an increase in I_{C1}. However, since I_{IN} stays constant, an increase in I_{C1} means a decrease in I_{B3}, which causes a decrease in I_{C3} counteracting the original increase in I_{C3} caused by a change in V_{CE3}. The feedback loop consists of Q3 (as a voltage follower), Q1 and Q2 (as a current mirror), and Q1-R_1 (as an inverting voltage amplifier). The loop gain of the circuit is seen to be approximately $\beta_F/2$, so that the small signal output resistance will be comparable to that of the cascode current mirror. Figure 5.4-6b illustrates the I–V characteristics of the Wilson current mirror of Fig. 5.4-6a. It can be shown that

$$I_{OUT} = I_{IN}\left[1 - \frac{2}{\beta_F^2 + \beta_F + 2}\right] \tag{5.4-32}$$

r_{out} can be calculated from the small signal equivalent circuit of Fig. 5.4-6a shown in Fig. 5.4-7. The value of R_{eq} defined in Fig. 5.4–7 can be found to be

$$R_{eq} = \frac{v_1}{i} = \frac{r_{\pi 3} + R'}{1 + g_{m1}R'} \cong \frac{R'}{1 + g_{m1}R'} \cong \frac{1}{g_{m1}} \tag{5.4-33}$$

Using Eq. 5.4-33 allows us to express r_{out} as (see Prob. 5.27).

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{o3}\left[1 + \frac{g_{m1}\beta_{F3}}{g_{m1} + g_{m2}}\right] + \frac{1}{g_{m1} + g_{m2}} \cong \frac{r_{o3}\beta_{F3}}{2} \tag{5.4-34}$$

It is apparent from Eq. 5.4-34 that r_{out} has been improved over the simple current mirror of Fig. 5.4-1 by a factor of $\beta_0/2$. The small signal output resistance of current mirrors can be further increased by the use of special techniques.[5]

In many cases, the mirrored currents are designed not to be equal. This can be accomplished by making the base-emitter junction areas of the two mirror transistors unequal. They should be made as large as possible for best matching ratio accuracy. In Eq. 5.4-6, it can be seen that the ratio of the current in Q1 to that of Q2 is proportional to the ratio of the areas of the respective base-emitter junctions. This relationship can be expressed as

$$I_{C2} \cong \frac{A_2}{A_1}I_{C1} \tag{5.4-35}$$

If the ratio of the currents is much different from unity, this approach can use significant area and will become less accurate due to the decrease in relative accuracy of large area ratios.
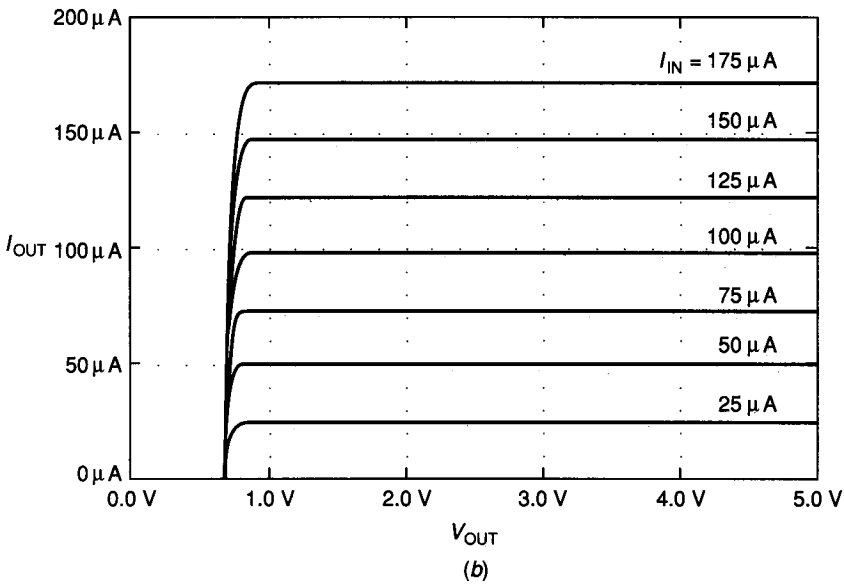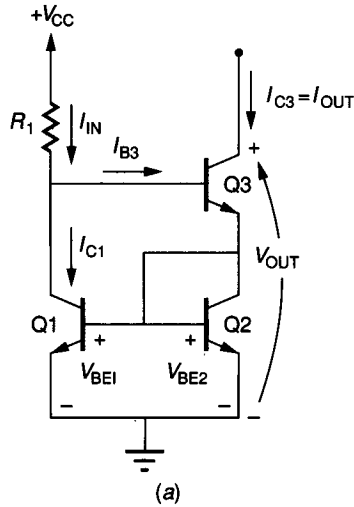
FIGURE 5.4-6
(a) Wilson BJT current mirror, (b) Simulated performance of the Wilson BJT current mirror of a.
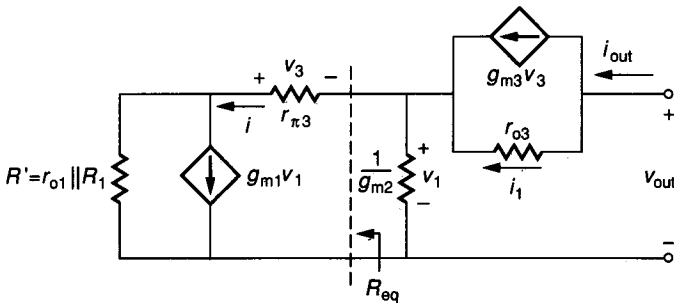

FIGURE 5.4-7
Small signal model for the Wilson current mirror of Fig. 5.4-6a.

The decrease in accuracy can be minimized using a principle called *replication*. Simply put, the replication principle states that an improvement in relative accuracy between two different sized areas occurs when the larger area is equal to an integer multiple of the smaller area. For example, suppose that $A_2 = mA_1$ where m is an integer. Improved relative accuracy is achieved when A_2 consists of m separate areas of A_1 connected appropriately. An example illustrates the replication principle.

> **Example 5.4-1.** Assume that Q1 and Q2 of Fig. 5.4-1 are being used to create a simple mirror having $I_{C2} = 5I_{C1}$. Assume further that A_1 is a rectangular area of W_1 times L_1, as shown in Fig. 5.4-8a. Q2 will have two different shapes. The first is shown in Fig. 5.4-8b and the second in Fig. 5.4-8c. Let $L_1 = L_2 = L$ and $W_1 = W$. Compare the ratio matching accuracy of the two layout approaches.

Solution. Assume resolution of any edge is given as

$$W_1 = W \pm \Delta W$$

$$W_2 = 5W \pm \Delta W$$

$$L_1 = L_2 = L \pm \Delta L$$

where ΔW and ΔL are the uncertainty of W and L. The ratio of A_2 to A_1 of Fig. 5.4-8b can be expressed as

$$\frac{A_2}{A_1} = \frac{(5W \pm \Delta W)(L \pm \Delta L)}{(W \pm \Delta W)(L \pm \Delta L)} = \frac{5 \pm (\Delta W/W)}{1 \pm (\Delta W/W)} \cong 5 \pm 4\frac{\Delta W}{W} \qquad (5.4\text{-}36)$$

Similarly the ratio of A_2 to A_1 of Fig. 5.4-8c is expressed as

$$\frac{A_2}{A_1} = \frac{5(W \pm \Delta W)(L \pm \Delta L)}{(W \pm \Delta W)(L \pm \Delta L)} = 5 \qquad (5.4\text{-}37)$$

The advantage of the replication principle is shown by the increased relative accuracy.

If the ratio of areas is not equal to an integer, the replication principle can still be used. If in Example 5.4-1 the value of I_{C2} were $5.5I_{C1}$, the larger transistor could consist of the replication of A_1 five times plus an area equal to $0.5A_1$. The designer has the option of making the $0.5A_1$ area the same shape as the A_1 area or choosing some other shape. The resulting ratio, while not as accurate as the integer case, will be more accurate than simply ratioing areas. If the areas represent transistors, the replicated areas are connected by connecting the collectors, bases and emitters of each replicated transistor.
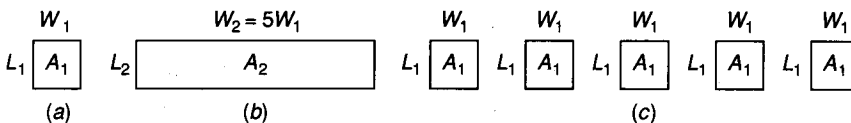

FIGURE 5.4-8
(a) Unit area A_1, (b) Area of $A_2 = 5A_1$, (c) Area of $A_2 = 5A_1$ obtained by replicating A_1 five times.

The large area ratio caused by unequal mirror currents can be avoided by using a resistor in series with the emitter of the lower current transistor, as shown in Fig. 5.4-9. This current mirror is called the Widlar current mirror[6] and can have large current differences with identical base-emitter areas. Note that the effect of R_2 will be to increase r_{out}. If Q1 and Q2 are matched and β_F is large, then the voltage drops around the base-emitter circuits can be written as

$$V_{BE1} - V_{BE2} = I_{C2}R_2 \tag{5.4-38}$$

If the V_{AF} effects are neglected, it follows from Eq. 5.4-11 that

$$V_t \ln\left(\frac{I_{IN}}{I_{C2}}\right) = I_{C2}R_2 \tag{5.4-39}$$

There are two cases in which Eq. 5.4-39 is used. The first is when I_{C2} and I_{IN} are known and R_2 is to be found. R_2 may be expressed as

$$R_2 = \frac{V_t}{I_{C2}} \ln\left(\frac{I_{IN}}{I_{C2}}\right) \tag{5.4-40}$$

For example, if $V_{CC} = 5$ V, $R_1 = 4.3\,\text{k}\Omega$ and $I_{C2} = 10\,\mu\text{A}$, then we find that $I_{C1} = (5 - 0.7)/4.3\,\text{k}\Omega = 1$ mA and $R_2 = 11.97\,\text{k}\Omega$ We note that the ratio of I_{C1} to I_{C2} is 100 in this example. The second case, which uses Eq. 5.4-40, occurs when R_2 and I_{IN} are known. In this case, an iterative solution is required for I_{C2}. The effect of R_2 on r_{out} is to increase it. It can be shown (see Prob. 5.28) that r_{out} of the Widlar current mirror is given as

$$r_{out} = r_{\pi2} \| R_2 + r_{o2}\left[1 + g_{m2}r_{\pi2} \| R_2\right] \cong r_{o2}(1 + g_{m2}R_2) \tag{5.4-41}$$

To obtain good ratio accuracies, Q1 and Q2 should have large emitter areas.

Because the output of the current mirrors is a current sink, it is important to have a small value of V_{MIN}, which was defined in the previous section. The same considerations for V_{MIN} and r_{out} apply to current mirrors. Unfortunately, the conditions of $V_{CE1} = V_{CE2}$ in order to eliminate the Early effects may not be
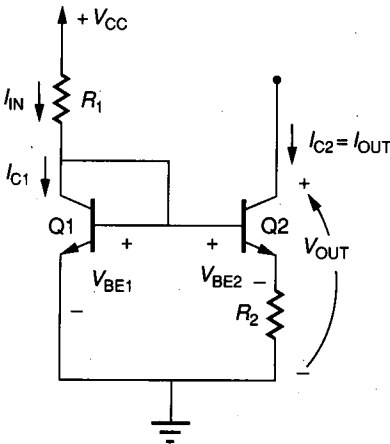

FIGURE 5.4-9
Widlar BJT current mirror.

compatible with the conditions for minimum V_{MIN}. For example, to obtain the minimum value of V_{MIN} in Fig. 5.4-4a requires that the dc voltage at the base of Q4 be equal to V_{CE2} (sat) $+ V_{BE4}$ (see Eq. 5.3-11). However, the voltage at the base of Q4 in Fig. 5.4-4a is equal to $2V_{BE2}$ assuming that all transistors are identical. A similar conflict between minimum V_{MIN} and large r_{out} exists for the Wilson current mirror of Fig. 5.4-6a. In this circuit, the minimum value of V_{MIN} is $V_{BE2} + V_{CE3}$(sat).

If one is willing to give up the constraint that V_{CE1} equals V_{CE2}, then it may be possible to achieve a minimum V_{MIN} design. Figure 5.4-10 shows one possible approach for the cascode current mirror of Fig. 5.4-4a. It has been assumed that Q1 through Q4 are identical transistors each having a base-emitter drop of V_{BE2}. It can be seen that if $V_{BE6} = V_{BE2} - V_{CE2}$(sat), that $V_{CE2} = V_{CE2}$(sat). V_{BE6} can be smaller than V_{BE2} by either decreasing the current of Q6 with respect to the current in Q1 through Q4 or by making the emitter area of Q6 much smaller than that of Q1 through Q4, or both. This can be seen by considering two different transistors designated as QA and QB. The difference in V_{BE} voltages can be expressed using Eqs. 5.4-4 and 5.4-5 as

$$\Delta V_{BE} = V_{BEA} - V_{BEB} = V_t \ln\left(\frac{I_{CA}\, I_{SB}}{I_{CB}\, I_{SA}}\right) \qquad (5.4\text{-}42)$$

Unfortunately, if ΔV_{BE} is much larger than V_t, the value of $(I_{CA}I_{SB})/(I_{CB}I_{SA})$ becomes too large to implement. For example, if the area of Q5 and Q6 of Fig.
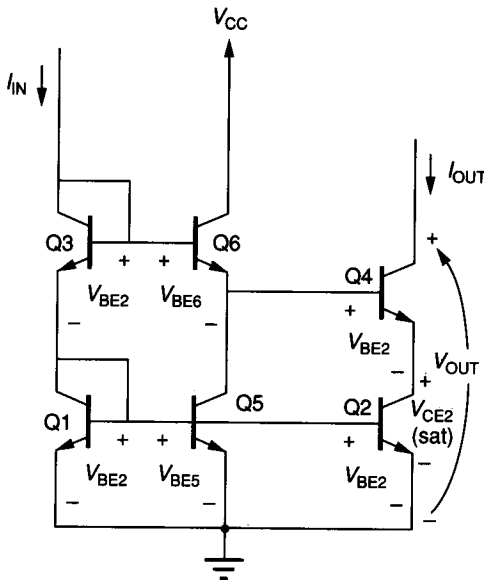

FIGURE 5.4-10
Reduction of V_{MIN} of the BJT cascode current mirror of Fig. 5.4-4a.

5.4-10 is 50 times less than the area of Q1 through Q4, then ΔV_{BE} of Eq. 5.4-42 would be approximately 200 mV at room temperature. However, any component whose area is 50 times different than another has several disadvantages. These disadvantages include a large area requirement and poor matching between devices. The principle behind the Widlar current mirror could be employed to reduce the current in Q5 and Q6 by placing a resistor in series with the emitter of Q5. The current ratio required to obtain a ΔV_{BE} of 200 mV is approximately 2500. This ratio results in a value of $R_2 = 507$ kΩ at room temperature with $I_{C1} = 1$ mA.

The BJT current mirrors that have been presented can be characterized from the viewpoint of accuracy, output resistance, and V_{MIN}. Table 5.4-1 summarizes the performance of the BJT current mirrors considered where $I_{C2} \approx I_{C1}$. Additional considerations include the proper sizes to achieve the desired matching accuracy.

The same principles developed in this section for current mirrors using the BJT device also hold true for the MOS device. In many cases, the MOS current mirrors are simpler in concept because no base current is required. On the other hand, the bulk effects create limitations not found in BJT mirrors. The matching principle applied to MOS devices can be developed from the simple current mirror of Fig. 5.4-11a. Note that for $V_{DS1} \geq V_{T1}$, M1 will always be in saturation since $V_{DG1} = 0$. Assuming that V_{DS2} is greater than $V_{GS1} - V_{T1}$ allows the use of the saturation model for both devices. Solving for $V_{GS1} - V_{T1}$ and $V_{GS2} - V_{T2}$ from Eq. 4 of Table 3.1-1 gives

$$V_{GS1} - V_{T1} = \left[\frac{2L_1 I_{D1}}{K'_{N1} W_1 (1 + \lambda_1 V_{DS1})} \right]^{1/2} \tag{5.4-43}$$

and

$$V_{GS2} - V_{T2} = \left[\frac{2L_2 I_{D2}}{K'_{N2} W_2 (1 + \lambda_2 V_{DS2})} \right]^{1/2} \tag{5.4-44}$$

TABLE 5.4-1
Comparison of BJT current mirror performance

BJT current mirror	Accuracy ($I_{C2} = I_{C1}$)	r_{out}	V_{MIN}
Simple Fig. 5.4-1	Poor	$r_o = V_{AF}/I_o$	$V_{CE}(\text{sat})$
Cascode Fig. 5.4-4	Excellent	$r_o \beta_F$	$V_{BE} + V_{CE}(\text{sat})$
Wilson Fig. 5.4-6	Good	$\dfrac{r_o \beta_F}{2}$	$V_{BE} + V_{CE}(\text{sat})$
Modified cascode Fig. 5.4-10	Good	$r_o \beta_F$	$2V_{CE}(\text{sat})$

Since the bulk-source voltages of M1 and M2 are identical, then V_{T1} and V_{T2} are identical and the following expression results.

$$\frac{I_{OUT}}{I_{IN}} = \frac{I_{D2}}{I_{D1}} = \frac{K'_{N1}W_1L_2(1 + \lambda_2 V_{DS2})}{K'_{N2}W_2L_1(1 + \lambda_1 V_{DS1})} \qquad (5.4\text{-}45)$$

It can be seen that the channel modulation effect, λ, has the same influence on the MOS current mirror that the Early voltage had on the BJT current mirror. Because transistor Ws and Ls are found in Eq. 5.4-45, the geometry of the MOS devices can be used to determine the gain of the current mirror. Figure 5.4-11b gives the simulated I–V characteristics using equal values of $W = 50\ \mu$ and $L = 10\ \mu$ and the model parameters of $V_T = 0.75$ V, $K'_N = 24\ \mu A/V^2$, $\gamma_N = 0.8\ V^{-1/2}$, $\lambda_N = 0.01\ V^{-1}$, and $\phi = 0.6$ V. These characteristics indicate
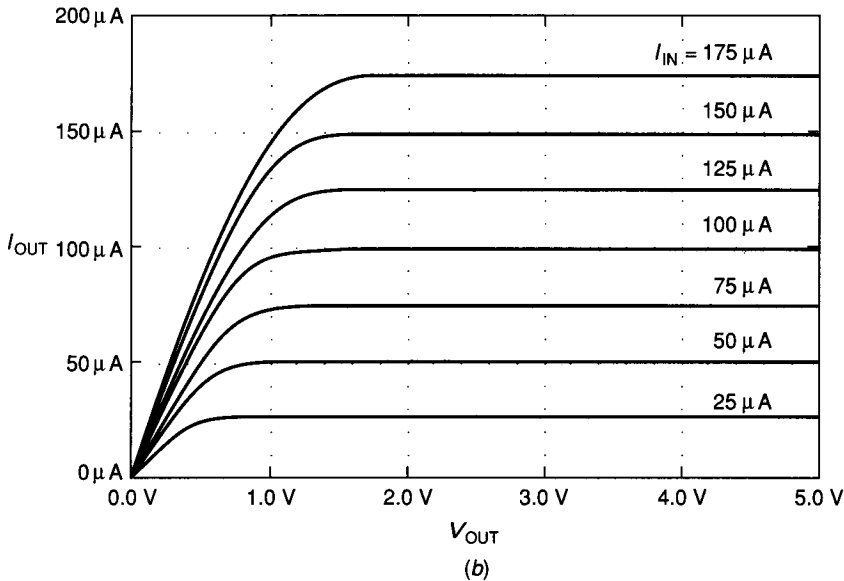

(a)

(b)
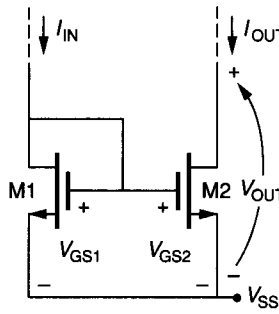
FIGURE 5.4-11
(a) Simple MOS current mirror, (b) Simulated performance of a.

that the channel modulation effect causes an increase in the slope of these curves preventing ideal current sink performance. A measure of the slope of these curves is given by the small signal output resistance and in this case is

$$r_{out} = \frac{v_{out}}{i_{out}} = r_{ds2} = \frac{1}{\lambda I_{D2}} = \frac{1}{\lambda I_{OUT}} \tag{5.4-46}$$

This corresponds to an output resistance of 1 MΩ when $I_{OUT} = 100$ μA. The value of V_{MIN} for the circuit of Fig. 5.4-11a which occurs when M2 transitions from the saturation to the active region can be shown to be 1.2 V when $I_{IN} = 100$ μA.

The matching accuracy of Eq. 5.4-45 can be determined in the same manner as was done for the BJT current mirror. The ratio of I_{D2} to I_{D1} (I_{OUT} to I_{IN}) can be expressed in general as

$$\frac{I_{D2}}{I_{D1}} = \frac{K'_{N2}(V_{GS2} - V_{T2})^2(1 + \lambda_2 V_{DS2})}{K'_{N1}(V_{GS1} - V_{T1})^2(1 + \lambda_1 V_{DS1})} \tag{5.4-47}$$

where it has been assumed that $W_2/L_2 = W_1/L_1$. In this discussion, the W/L ratios are assumed to be ideally matched. Using the following definitions

$$K'_{N1} = K'_N + (\Delta K'_N/2) \tag{5.4-48}$$

$$K'_{N2} = K'_N - (\Delta K'_N/2) \tag{5.4-49}$$

$$V_{T1} = V_T + (\Delta V_T/2) \tag{5.4-50}$$

$$V_{T2} = V_T - (\Delta V_T/2) \tag{5.4-51}$$

$$\lambda_1 = \lambda + (\Delta\lambda/2) \tag{5.4-52}$$

and

$$\lambda_2 = \lambda - (\Delta\lambda/2) \tag{5.4-53}$$

Eq. 5.4-47 may be expressed as

$$\frac{I_{D2}}{I_{D1}} = \frac{[K'_N - (\Delta K'_N/2)][V_{GS} - V_T + (\Delta V_T/2)]^2[1 + \lambda V_{DS} - (\Delta\lambda V_{DS}/2)]}{[K'_N + (\Delta K'_N/2)][V_{GS} - V_T - (\Delta V_T/2)]^2[1 + \lambda V_{DS} + (\Delta\lambda V_{DS}/2)]}$$
$$\tag{5.4-54}$$

or as

$$\frac{I_{D2}}{I_{D1}} = \frac{(1 - \Delta K'_N/K'_N)[1 + \Delta V_T/2(V_{GS} - V_T)]^2(1 + \lambda V_{DS} - \Delta\lambda V_{DS}/2)}{(1 + \Delta K'_N/K'_N)[1 - \Delta V_T/2(V_{GS} - V_T)]^2(1 + \lambda V_{DS} + \Delta\lambda V_{DS}/2)}$$
$$\tag{5.4-55}$$

Assuming that the differences in Eqs. 5.4-48 through 5.4-53 are small and that λV_{DS} is less than unity allows the simplification of Eq. 5.4-55 to

$$\frac{I_{D2}}{I_{D1}} \cong \left(1 - \frac{\Delta K'_N}{K'_N}\right)\left(1 + \frac{\Delta V_T}{V_{GS} - V_T}\right)^2(1 - \Delta\lambda V_{DS}) \tag{5.4-56}$$

or

$$\frac{I_{D2}}{I_{D1}} \cong 1 - \left(\frac{\Delta K'_N}{K'_N}\right) + \left(\frac{2}{(V_{GS}/V_T) - 1}\right)\left(\frac{\Delta V_T}{V_T}\right) - (\lambda V_{DS})\left(\frac{\Delta \lambda}{\lambda}\right) \qquad (5.4\text{-}57)$$

An example will illustrate these results

Example 5.4-1. Matching accuracy of a simple MOS mirror. Two MOS devices are used to implement the current mirror of Fig. 5.4-11a. Suppose that at $I_{IN} = 100\,\mu A$, the various voltages were observed: $V_{GS1} = V_{GS2} = 3.6$ V and $V_{DS2} = 3.6$ V. Assume that the nominal parameters are $K'_N = 24\ \mu A/V^2$, $V_T = 0.75$ V and $\lambda_N = 0.01 V^{-1}$. Furthermore, assume that the worst-case deviation about these values is $\pm 5\%$. Evaluate the deviation of the ratio of I_{D2}/I_{D1} from unity if $(W_1/L_1) = (W_2/L_2)$.

Solution. Substituting into Eq. 5.4-57 gives

$$\frac{I_{D2}}{I_{D1}} = 1 - (\pm 0.05) + (0.2598)(\pm 0.05) - (0.036)(\pm 0.05)$$

$$= 1 \pm 0.039$$

Under these conditions, the analysis of matching accuracy shows that a deviation of $\pm 4\%$ can occur. The value of this deviation will depend upon the operating conditions. In this example, V_{DS1} was chosen to be equal to V_{DS2} in order to eliminate the error due to λ.

A current mirror with higher output resistance than that obtained from the simple MOS mirror is shown in Fig. 5.4-12a. M3 and M4 keep the values of V_{DS1} and V_{DS2} nearly equal, effectively removing the influence of the channel modulation effect. M4 increases the output resistance of the mirror using the principle demonstrated in Fig. 5.3-7a to increase the output resistance of a simple MOS current sink. Figure 5.4-12a is called an MOS cascode current mirror and is topologically identical to the BJT cascode current mirror of Fig. 5.4-4a. If the mismatch effects are neglected, the current gain of the MOS cascode current mirror is given as

$$\frac{I_{OUT}}{I_{IN}} = \frac{(W_2/L_2)}{(W_1/L_1)} \qquad (5.4\text{-}58)$$

Figure 5.4-12b shows the I–V characteristics of the circuit of Fig. 5.4-12a when all Ws are 50 μ, all Ls are 10 μ, $V_T = 0.75$ V, $K'_N = 24\ \mu A/V^2$, $\gamma_N = 0.8\ V^{1/2}$, $\lambda_N = 0.01\ V^{-1}$, and $\phi = 0.6$ V. These characteristics show that the output resistance of the MOS cascode mirror is significantly greater than the simple MOS mirror and that the accuracy is good.

The improvement in the slope reduction can be quantified by finding the small signal output resistance of the circuit of Fig. 5.4-12a. The output resistance of the MOS cascode current mirror is calculated using the small signal model of Fig. 5.4-13. First solve for v_{out}, which can be written as

$$v_{out} = v_4 + v_2 = r_{ds4}[i_{out} + g_{mb4}v_2 - g_{m4}(v_3 + v_1 - v_2)] + v_2 \qquad (5.4\text{-}59)$$
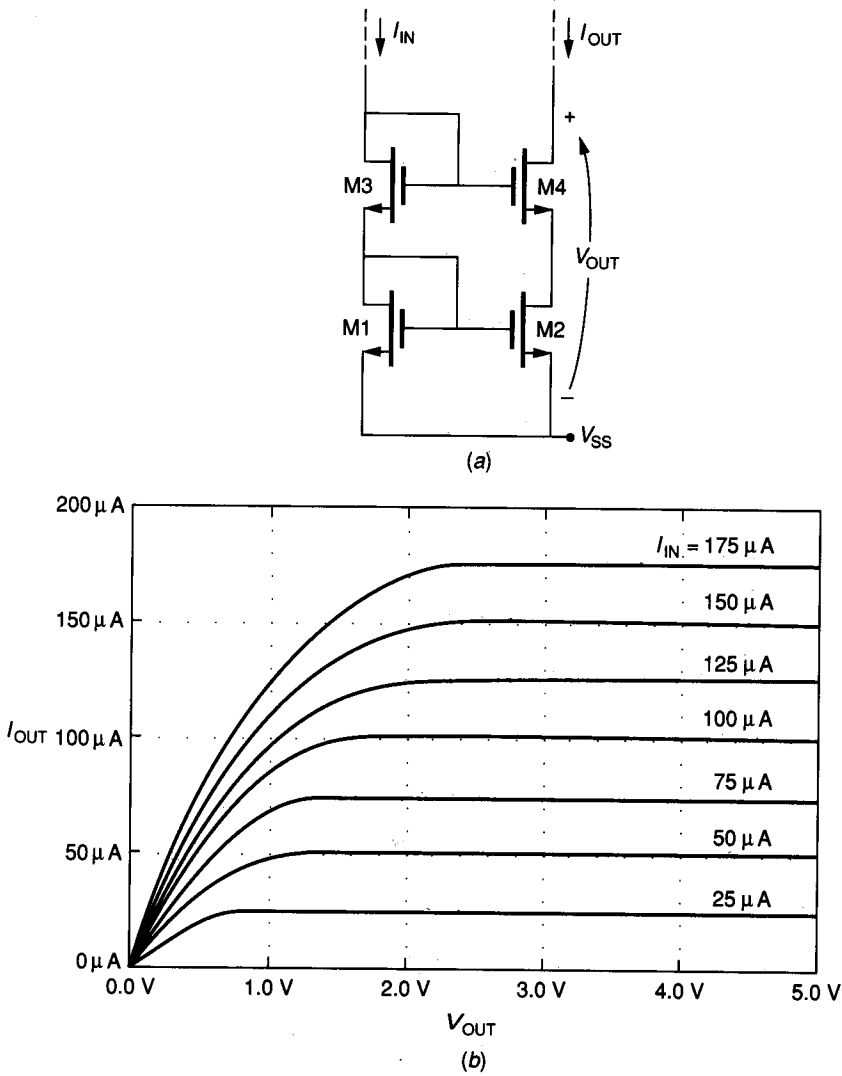
FIGURE 5.4-12
(*a*) MOS cascode current mirror, (*b*) Simulated performance of *a*.

Also,

$$v_2 = r_{ds2}(i_{out} - g_{m2}v_1) \tag{5.4-60}$$

Since $i_{in} = 0$ under small signal conditions, then v_1 and v_3 are also zero. Therefore, substitution of Eq. 5.4-60 into Eq. 5.4-59 results in,

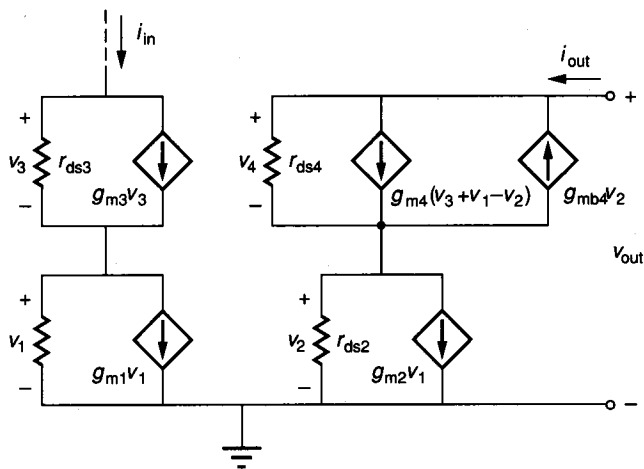$$v_{out} = i_{out}[r_{ds2} + r_{ds4} + r_{ds2}r_{ds4}(g_{m4} + g_{mb4})] \tag{5.4-61}$$

FIGURE 5.4-13
Small signal model of the current mirror of Fig. 5.4-12a.

Solving for the output resistance, r_{out}, gives

$$r_{out} = r_{ds2} + r_{ds4} + r_{ds2}r_{ds4}g_{m4}(1 + \eta_4) \qquad (5.4\text{-}62)$$

where $\eta_4 = g_{mb4}/g_{m4}$ is defined in Table 3.1-3.

Comparing Eq. 5.4-62 with Eq. 5.4-46 shows that the small signal output resistance has been increased by a factor of $r_{ds4}g_{m4}(1 + \eta_4)$. The approximate value of r_{out} at 100 μA is 155 MΩ. The value of V_{MIN} at 100 μA for the MOS cascode mirror above is approximately 1.6 V, which can be a significant portion of V_{OUT}.

The MOS version of the Wilson current mirror is shown in Fig. 5.4-14a. The simulated performance of this current mirror using $W_1/L_1 = W_2/L_2 = W_3/L_3 = 50 \ \mu/10 \ \mu$ and the previous MOS model parameters is shown in Fig. 5.4-14b. Several aspects of the MOS Wilson current mirror are apparent. The first is that V_{MIN} represents a large portion of V_{OUT}. The second is that the curves are much flatter than the simple MOS mirror, indicating an increase in r_{out}. And thirdly, it can be shown that the linearity (or accuracy) of the MOS Wilson current mirror is not good for high current levels. This nonlinearity is due to the difference in V_{DS1} and V_{DS2} for larger currents. Since V_{DS2} is less than V_{DS1}, Eq. 5.4-45 shows that the channel modulation effects will cause I_{D2} to be less than I_{D1} if M1 and M2 are matched. This problem can be alleviated if a fourth, drain-gate-connected device is connected in series with M1 between the drain of M1 and the gate of M3.

The output resistance of the MOS Wilson current mirror will quantify the slope reduction compared with the simple MOS mirror. It can be shown that the small signal output resistance of the Wilson current mirror is given as (see Prob. 5.31)
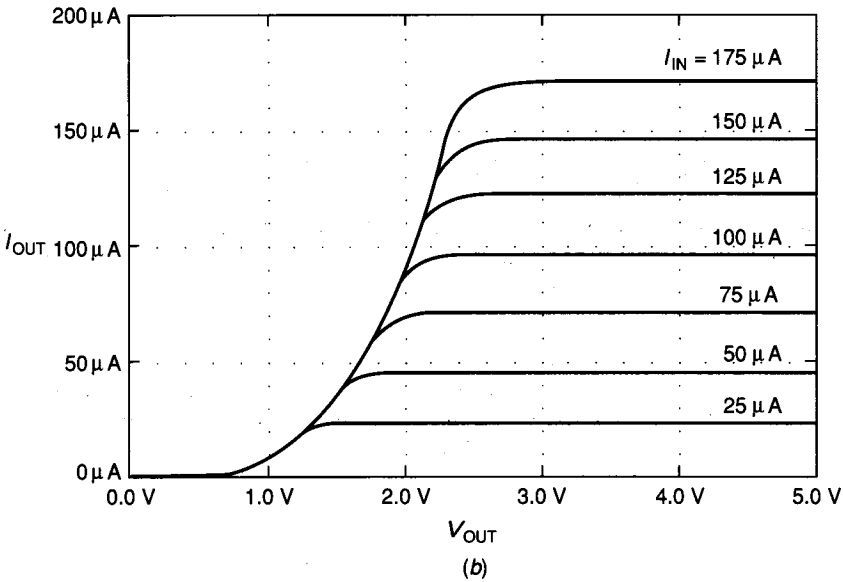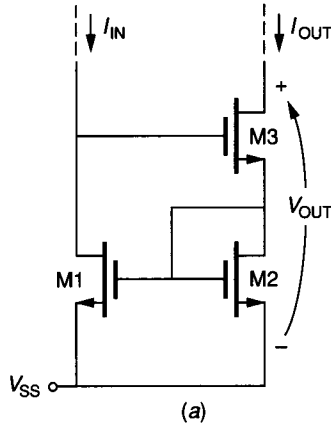
FIGURE 5.4-14
(a) MOS Wilson current mirror, (b) Simulated performance of a.

$$r_{out} = r_{ds3} + r_{ds2} \frac{1 + r_{ds3}g_{m3}(1 + \eta_3) + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + g_{m2}r_{ds2}} \qquad (5.4\text{-}63)$$

The output resistance of Fig. 5.4-14a is found to be comparable with the MOS cascode mirror of Fig. 5.4-12a. Unfortunately, both of these current mirrors require at least $2V_T$ across the input before they behave as described above.

The Widlar current mirror can also be implemented by MOS transistors and will be left as a problem (see Prob. 5.32). A practical consideration in matching the devices that are mirroring the current is to keep the channel lengths of both

devices equal. Since the channel length, L, is susceptible to lateral diffusion and the channel width is not, then the channel width, W, can be used to achieve nonunity current gains. Oxide encroachment has been ignored in this consideration. This was illustrated by the principle of replication, which was discussed earlier in this section.

In all the previous MOS current mirrors, the value of V_{MIN} became larger when the output resistance was increased. One circuit that minimizes V_{MIN} and still increases r_{out} is shown in Fig. 5.4-15a. This circuit is called the MOS regulated cascode mirror and uses the concept introduced in the regulated cascode
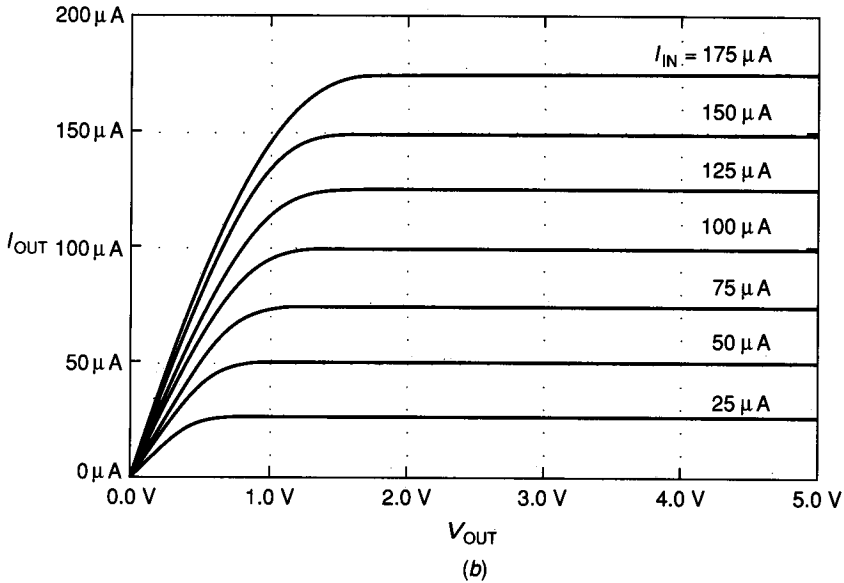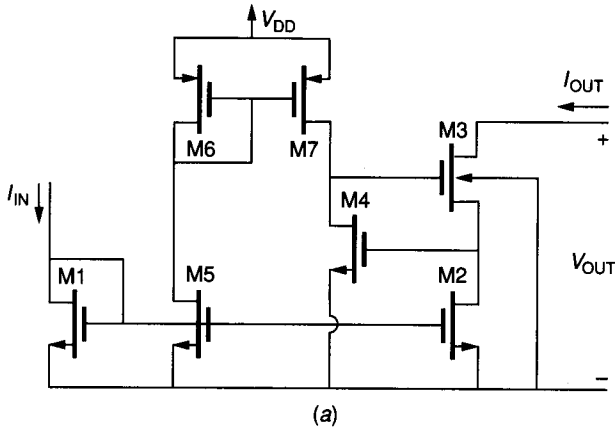

(a)

(b)

FIGURE 5.4-15
(a) MOS regulated cascode current mirror, (b) Simulated performance of a.

current sink of Fig. 5.3-16. The regulated cascode consists of M2, M3, and M4. M1 and M2 form a simple current mirror; however, because of M4, the value of V_{DS2} will not be much different than V_{DS1}, giving good accuracy. M5, M6, and M7 are used to provide a bias current for M4, which tracks the output current. If I_{D4} did not track I_{OUT} (I_{D3}), then the value of V_{GS2} would not be large enough at large values of I_{OUT} to keep M2 in saturation. If M2 is not in saturation, then the ratio of I_{D2} to I_{D1} will be smaller than what is expected. Figure 5.4-15b shows the simulated results for the regulated cascode current mirror of Fig. 5.4-15a when $W_1/L_1 = W_2/L_2 = W_3/L_3 = W_4/L_4 = W_5/L_5 = W_6/L_6 = 50\,\mu/10\,\mu$, $W_7/L_7 = 75\,\mu/10\,\mu$, and using the model parameters as before, with the addition of $K'_P = 8\,\mu A/V^2$, $V_{TP} = -0.75$ V, $\gamma_P = 0.4$ V$^{-1/2}$, $\lambda_P = 0.02$ V^{-1}, and $\phi = 0.6$ V. It is seen that V_{MIN} is almost identical to that of the simple MOS mirror of Fig. 5.4-11b. In addition, the output resistance is given by Eq. 5.3-20 and is much higher than any of the other MOS mirrors presented so far. Clearly, Fig. 5.4-15a is a superior MOS current mirror realization in many respects. If the ratio of I_{D5} to I_{D2} is decreased below the 0.5 of Fig. 5.4-15b, the value of V_{MIN} decreases, but the ratio of I_{OUT} to I_{IN} becomes nonlinear as the currents increase.

Table 5.4-2 summarizes the performance of the MOS current mirrors having unity gain from the viewpoint of accuracy (linearity), output resistance, and V_{MIN}. Additional considerations include the size of devices. More ratio accuracy will be obtained for larger size devices. All of the current mirrors presented in this section used npn BJTs or n-channel MOSFETs. Opposite-type current mirrors can be implemented using pnp BJTs or p-channel MOSFETs. The circuits perform in an identical manner. The parametric expressions for the small signal resistances are identical in either case.

The important principles developed and used in this section include the matching principle, the replication principle, and the method by which mismatches between similar devices can be calculated. These principles will be employed where appropriate in the material that follows. The circuits developed in this section will be very useful in designing more complex analog circuits. They will find use in dc biasing and as high-resistance ac loads.

TABLE 5.4-2
Comparison of MOS current mirror performance

MOS current mirror	Accuracy $(I_{D2} = I_{D1})$	r_{out}	V_{MIN}
Simple Fig. 5.4-11a	Poor	$r_o \cong \dfrac{1}{\lambda I_{out}}$	$V_{DS}(sat)$
Cascode Fig. 5.4-12a	Good	$g_m r_o^2$	$2V_{DS}(sat)$
Wilson Fig. 5.4-14a	Good	$\dfrac{g_m r_o^2}{2}$	$V_{GS} + V_{DS}(sat)$
Regulated cascode Fig. 5.4-15a	Good	$g_m^2 r_o^3$	$V_{DS}(sat)$

5.5   VOLTAGE AND CURRENT REFERENCES

In Sec. 5.3, current sinks/sources were presented. These circuits can be used to create a voltage by applying the current to a resistor. Such circuits represent one method of achieving a dc voltage or current. However, many applications require a dc voltage or current that is more stable than the circuits of Sec. 5.3. Circuits that yield a precise dc voltage or current independent of external influences are called *voltage references* or *current references*. The primary external influences of concern are power supply and temperature variations. The objective of this section will be to demonstrate the principles of voltage and current references that minimize their dependence on power supply and temperature.

In order to characterize the dependence of a reference on power supply and temperature, the concepts of sensitivity and fractional temperature coefficient are introduced. Assume that the reference is a voltage designated as V_{REF}. The sensitivity of V_{REF} to changes in a power supply V_{XX} is given as

$$S_{V_{XX}}^{V_{REF}} = \lim_{\Delta V_{XX} \to 0} \frac{\Delta V_{REF}/V_{REF}}{\Delta V_{XX}/V_{XX}} = \frac{V_{XX}}{V_{REF}} \left(\frac{\partial V_{REF}}{\partial V_{XX}} \right) \qquad (5.5\text{-}1)$$

Eq. 5.5-1 emphasizes how the sensitivity can be calculated. However, once the sensitivity is known, it can be applied using the following form.

$$\frac{\Delta V_{REF}}{V_{REF}} \simeq \left(S_{V_{XX}}^{V_{REF}} \right) \left(\frac{\Delta V_{XX}}{V_{XX}} \right) \qquad (5.5\text{-}2)$$

Eq. 5.5-2 can be interpreted as follows: if the sensitivity of V_{REF} with respect to V_{XX} is unity then a 10% change in V_{XX} will cause a 10% change in V_{REF}. Obviously, if V_{REF} is to be independent of V_{XX}, then the sensitivity of V_{REF} with respect to V_{XX} should approach zero. Sensitivities less than 1/100 are practical values for a monolithic voltage reference. The above formulation is valid for current references by simply replacing V_{REF} by I_{REF}.

While the sensitivity measure given in Eq. 5.5-1 with V_{XX} replaced with the temperature (i.e. $S_T^{V_{REF}}$) could be used as a measure of the dependence of the reference on temperature, it is customary to use the concept of fractional temperature coefficient introduced in Eq. 2.2-5 of Chapter 2. The fractional temperature coefficient (TC$_F$) of V_{REF} is defined as

$$TC_F(V_{REF}) = \frac{1}{V_{REF}} \frac{\partial V_{REF}}{\partial T} = \frac{1}{T} S_T^{V_{REF}} \qquad (5.5\text{-}3)$$

where the relationship between the fractional temperature coefficient of V_{REF} and the sensitivity of V_{REF} to temperature (T) is also illustrated. The units of TC$_F$ are expressed in terms of parts per million per °C, or ppm/°C. Assuming that a sensitivity of V_{REF} with respect to temperature equal to 1/100 is indicative of a good voltage reference, then at room temperature $(T = 300°K)$ the fractional temperature coefficient is $(1/300) \times (1/100) \times 1,000,000 = 33.3$ ppm/°C. References with a TC$_F$ of less than 50 ppm/°C are considered to be stable with respect to temperature.

Figure 5.5-1 shows three simple voltage references which will be more useful for illustrating the analysis techniques than for implementing a good voltage reference. Figure 5.5-1a is simply a voltage divider providing a dc voltage between V_{XX} and ground. The value of dc voltage is

$$V_{REF} = V_{XX}\left(\frac{R_2}{R_1 + R_2}\right) \tag{5.5-4}$$

The sensitivity of V_{REF} with respect to V_{XX} is found to be

$$S_{V_{XX}}^{V_{REF}} = \frac{V_{XX}}{V_{REF}}\frac{\partial V_{REF}}{\partial V_{XX}} = 1 \tag{5.5-5}$$

The fractional temperature coefficient of this simple voltage reference is found after some algebraic manipulation to be

$$\begin{aligned}TC_F(V_{REF}) &= \frac{1}{V_{REF}}\frac{\partial V_{REF}}{\partial T} = \left(\frac{R_1}{R_2}\frac{V_{REF}}{V_{XX}}\right)\left(\frac{\partial R_2}{R_2\partial T} - \frac{\partial R_1}{R_1\partial T}\right)\\[2mm] &= \left(\frac{R_1}{R_2}\frac{V_{REF}}{V_{XX}}\right)[TC_F(R_2) - TC_F(R_1)]\end{aligned} \tag{5.5-6}$$

where the resistors are assumed to be temperature-dependent and V_{XX} is temperature-independent. Equation 5.5-6 illustrates a very important property of temperature dependence. Note that if the fractional temperature coefficients of R_2, $TC_F(R_2)$, and of R_1, $TC_F(R_1)$, are equal then $TC_F(V_{REF})$ is zero. Thus, if both R_1 and R_2 are made from identical means, i.e., diffusion, polysilicon, etc., then temperature independence will be achieved. This result will hold true for ratios of similar components. It is easy to illustrate the principle from Eqs. 5.5-4 and
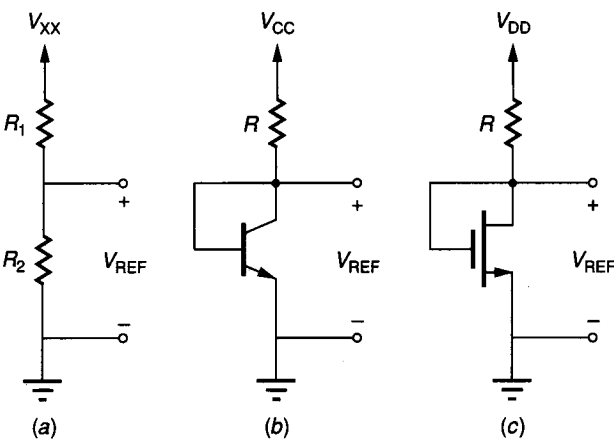

FIGURE 5.5-1
Simple voltage references: (a) Passive voltage divider, (b) BJT voltage reference and (c) MOS voltage reference.

5.5-6. If $TC_F(R_2)$ is equal to $TC_F(R_1)$, then the percentage changes are approximately equal. Suppose that $R_2 = 2\,\Omega$ and $R_1 = 1\,\Omega$. The value of V_{REF} is $V_{XX}/3$. If the temperature changes so that the resistors experience a 10% increase, they become $R_2' = 2.2\,\Omega$ and $R_1' = 1.1\,\Omega$. Substituting these values into Eq. 5.5-4 still gives V_{REF} of $V_{XX}/3$.

Figure 5.5-1b illustrates how a voltage reference can be achieved from a BJT and a resistor. The reference voltage can be found using the relationship for the collector current as a function of base–emitter voltage (Eq. 3.3-13 of Sec. 3.3). The result is

$$V_{REF} = V_t \ln\left(\frac{V_{CC} - V_{REF}}{R I_S}\right) \tag{5.5-7}$$

where V_t and I_S are parameters of the BJT defined in Chapter 3. Because V_{REF} is also inside the argument of the natural logarithm, an iterative solution is necessary to obtain V_{REF}. If V_{CC} is much greater than V_{REF}, then Eq. 5.5-7 simplifies to

$$V_{REF} \approx V_t \ln\left(\frac{V_{CC}}{R I_S}\right) \tag{5.5-8}$$

The sensitivity of V_{REF} with respect to V_{CC} can be found by differentiating either Eq. 5.5-7 or 5.5-8 and substituting into Eq. 5.5-1. Assuming that $V_{CC} \gg V_{REF}$ (see Prob. 5.34 when this is not true), the sensitivity of the circuit of Fig. 5.5-1b is

$$S_{V_{CC}}^{V_{REF}} \cong \frac{1}{\ln(V_{CC}/R I_S)} \tag{5.5-9}$$

If $V_{CC} = 5$ V, $R = 43\,k\Omega$ and $I_S = 0.4$ fA, the sensitivity of V_{REF} with respect to V_{CC} is 0.0379. If V_{CC} changes by 10%, V_{REF} will change by only 0.379%. Thus, a second principle emerges concerning low-sensitivity references. If two or more components which have different large signal voltage–current characteristics are used to divide voltage, it is possible to achieve sensitivities less than unity.

The temperature behavior of the circuit of Fig. 5.5-1b will be more complex than that of Fig. 5.5-1a because V_t, R, and I_S all vary with temperature. Differentiating Eq. 5.5-8 with respect to temperature yields

$$\frac{\partial V_{REF}}{\partial T} = \frac{V_{REF}}{T} - V_t\left(\frac{1}{I_S}\frac{\partial I_S}{\partial T} + \frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-10}$$

Assuming that I_S is given as

$$I_S = K T^3 \exp\left(\frac{-V_{GO}}{V_t}\right) \tag{5.5-11}$$

where V_{GO} is the band gap voltage of silicon (1.205 V), which is temperature independent, allows the derivative of I_S with respect to temperature to be expressed as

$$\frac{\partial I_S}{\partial T} = \frac{3 I_S}{T} + \frac{I_S}{T}\frac{V_{GO}}{V_t} \tag{5.5-12}$$

Substituting Eq. 5.5-12 into Eq. 5.5-10 and dividing by V_{REF} gives

$$TC_F(V_{REF}) = \frac{V_{REF} - 3V_t - V_{GO}}{V_{REF}T} - \frac{V_t}{V_{REF}}\left(\frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-13}$$

If $V_{REF} = 0.7$ V and the TC_F of R is 1500 ppm/°C, the $TC_F(V_{REF})$ of Fig. 5.5-1b at room temperature (300°K) is

$$TC_F(V_{REF}) = -2776\,\text{ppm/°C} - 56\,\text{ppm/°C} = -2832\,\text{ppm/°C} \tag{5.5-14}$$

It is seen that this voltage reference has a large temperature coefficient for a voltage reference.

Figure 5.5-1c shows how MOS technology can be used to implement a voltage reference similar to the simple BJT voltage reference of Fig. 5.5-1b. Since the drain and gate are physically connected, the device is in saturation for $V_{GS} \geq V_T$ and V_{REF} can be expressed as

$$V_{REF} = V_T + \sqrt{\frac{2(V_{DD} - V_{REF})}{RK'_N(W/L)}} \tag{5.5-15}$$

As before, an iterative method is used to solve for V_{REF}. If $V_{DD} = 10$ V, $V_T = 0.75$ V, $K'_N = 24\,\mu\text{A/V}^2$, $W/L = 10$, and $R = 100\,\text{k}\Omega$, then iterative methods give a V_{REF} of 1.972 V. If V_{DD} is greater than V_{REF}, then

$$V_{REF} \approx V_T + \sqrt{\frac{2V_{DD}}{RK'_N(W/L)}} \tag{5.5-16}$$

Using Eq. 5.5-16 with these parameters and values gives $V_{REF} = 2.085$. The sensitivity of the circuit of Fig. 5.5-1c with respect to V_{DD} can be found for the case where $V_{DD} \gg V_{REF}$ as

$$S_{V_{DD}}^{V_{REF}} = \frac{0.5}{1 + V_T\sqrt{RK'_N W/2V_{DD}L}} \tag{5.5-17}$$

Using the above parameters and values gives a sensitivity of V_{REF} with respect to V_{DD} of 0.274. The sensitivity of the circuit of Fig. 5.5-1c is larger than the circuit of Fig. 5.5-1b because the power supply in the BJT case is in the argument of the logarithm, while in the MOS case it is within the argument of the square root. Since the logarithm is a weaker function than the square root, the sensitivity of the BJT voltage reference is smaller than the MOS voltage reference.

In order to analyze the temperature dependence, the temperature dependence of the MOS transistor must be characterized. The primary temperature-dependent parameters of the MOS device are K' (mobility) and V_T. Their temperature dependence will be modeled as

$$K'_N = K'_{NO}\left(\frac{T}{T_O}\right)^{1.5} \tag{5.5-18}$$

and

$$V_T = V_{TO} - \alpha(T - T_O) \tag{5.5-19}$$

where K'_{NO} and V_{TO} are the values of K'_N and V_T at T_O and α is approximately 2.3 mV/°C. Assuming R, K'_N, and V_T are temperature-dependent and differentiating Eqs. 5.5-16, 5.5-18, and 5.5-19 gives

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_T}{\partial T} - \frac{1}{2}\sqrt{\frac{2V_{DD}}{K'_N R(W/L)}}\left(\frac{1}{R}\frac{\partial R}{\partial T}\right) - \frac{1}{2}\sqrt{\frac{2V_{DD}}{K'_N R(W/L)}}\frac{1}{K'_N}\frac{\partial K'_N}{\partial T}$$

(5.5-20)

$$\frac{\partial K'_N}{\partial T} = -\frac{1.5}{T}K'_N \qquad (5.5\text{-}21)$$

and

$$\frac{\partial V_T}{\partial T} = -\alpha \qquad (5.5\text{-}22)$$

Substituting Eqs. 5.5-21 and 5.5-22 into Eq. 5.5-20 and dividing by V_{REF} gives

$$TC_F(V_{REF}) = \frac{-1}{V_{REF}}\left[\alpha + \frac{1}{2}\sqrt{\frac{2V_{DD}}{K'_N R(W/L)}}\left(\frac{1}{R}\frac{\partial R}{\partial T} - \frac{1.5}{T}\right)\right] \qquad (5.5\text{-}23)$$

Using the values above with $V_{REF} = 2.085$ V and assuming that $TC_F(R) = 1500$ ppm/°C, the fractional temperature coefficient becomes

$$TC_F(V_{REF}) = \frac{-1}{2.085}[0.0023 - 0.0016] = -336 \text{ ppm/°C} \qquad (5.5\text{-}24)$$

While the $TC_F(V_{REF})$ of Fig. 5.5-1c is almost 10 times less than that of Fig. 5.5-1b, this is due to the selection of the resistor and the particular manner in which the temperature-dependent variables combine to give the overall temperature dependence.

The simple voltage references of Fig. 5.5-1 illustrate the methods by which more complex references can be characterized. The value of V_{REF} of Figs. 5.5-1b and 5.5-1c can be increased by cascading active devices or by the method illustrated in Fig. 5.5-2. It can be shown that the reference voltages of Fig. 5.5-2a and b are equal to $(1 + R_2/R_1)$ times the values given in Eqs. 5.5-8 and 5.5-16, respectively.

Current references are also of interest in this section. Figure 5.3-4a and Fig. 5.3-5a show examples of simple current references. However, one important aspect of these two current references is the implementation of V_{BB} and V_{GG}. In most cases V_{BB} and V_{GG} are implemented using the circuits of Figs. 5.5-1b and c, respectively. The result is shown in Fig. 5.5-3a and b and is in fact the simple current mirrors of Sec. 5.4, where I_{IN} is defined by the voltage across R. Using the relationships of the last section and assuming ideal current mirrors gives

$$I_{REF} = \frac{V_{CC} - V_{BE}}{R} \qquad (5.5\text{-}25)$$
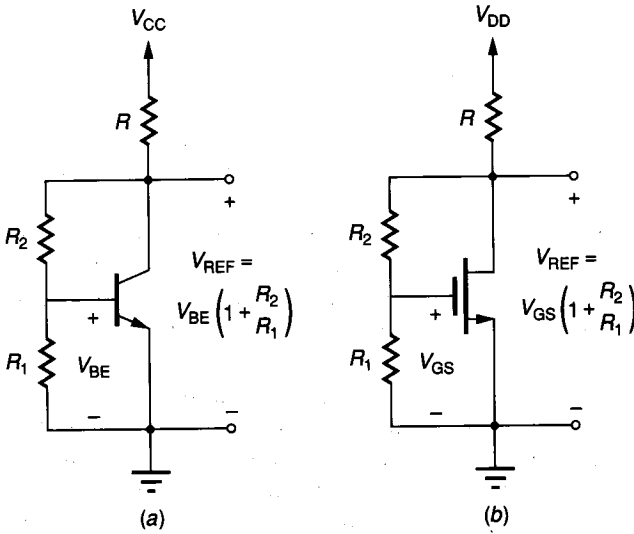
FIGURE 5.5-2
A method of increasing the value of V_{REF} for (a) Fig. 5.5-1b, (b) Fig. 5.5-1c.

and

$$I_{REF} = \frac{V_{DD} - V_{GS}}{R} \qquad (5.5\text{-}26)$$

for Figs. 5.5-3a and 5.5-3b. It is obvious that the sensitivity of I_{REF} with respect to power supply is unity for both references if $V_{CC} \gg V_{BE}$ or $V_{DD} \gg V_{GS}$. The temperature coefficient of I_{REF} for Fig. 5.5-3a can be found by differentiating Eq. 5.5-25 with respect to temperature and dividing by I_{REF}. The result is

$$TC_F(I_{REF}) = \frac{-1}{I_{REF}}\left[\frac{\partial V_{BE}}{R\,\partial T} + I_{REF}\left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\right] \qquad (5.5\text{-}27)$$

Using the previous results for $\partial V_{BE}/\partial T$ yields

$$TC_F(I_{REF}) \approx \frac{1}{I_{REF}}\left[\frac{V_{GO} + 3V_t - V_{BE}}{RT}\right] - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right) \qquad (5.5\text{-}28)$$

where it is assumed that V_t is much less than $V_{CC} - V_{BE}$. If $I_{REF} = 100\,\mu A$, then $V_{BE} = 0.682$ V for $I_S = 0.4$ fA. If $R = 43$ kΩ($V_{CC} = 5$ V), $TC_F(R) = 1500$ ppm/°C and $T = 300$ K, then $TC_F(I_{REF})$ is equal to

$$TC_F(I_{REF}) = 466 \text{ ppm/°C} - 1500 \text{ ppm/°C} = -1034 \text{ ppm/°C} \qquad (5.5\text{-}29)$$

The current reference above has an additional term with an opposite sign in the expression for $TC_F(I_{REF})$, which suggests the possibility of achieving a zero value of $TC_F(I_{REF})$. Setting Eq. 5.5-28 to zero results in

$$I_{REF}R = V_{CC} - V_{BE} = \frac{V_{GO} + 3V_t - V_{BE}}{T(1/R)(\partial R/\partial T)} \qquad (5.5\text{-}30)$$
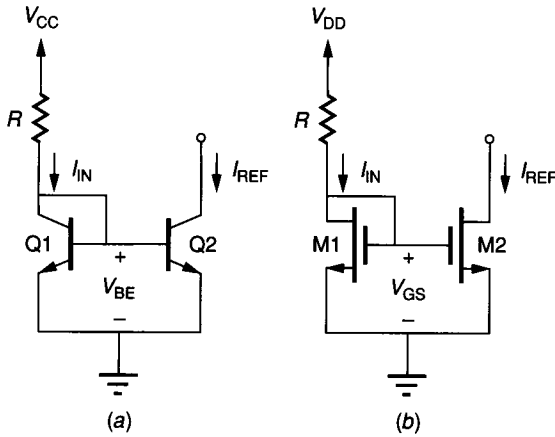
FIGURE 5.5-3
(a) A simple BJT current reference,
(b) A simple MOS current reference.

(a)   (b)

Using the previous values, we can solve for the value of V_{CC} that will give a zero $TC_F(I_{REF})$. The result is $V_{CC} = 2.018$ V. To achieve $I_{REF} = 100\ \mu$A, R would have to be decreased to $(2.018 - 0.682)/100\ \mu$A $= 13.36$ kΩ, which would not change the zero value of $TC_F(I_{REF})$.

The fractional temperature coefficient of the MOS current reference of Fig. 5.5-3b is found by differentiating Eq. 5.5-26 with respect to temperature and dividing by I_{REF} to get the following

$$TC_F(I_{REF}) = \frac{-1}{I_{REF}}\left[\frac{\partial V_{GS}}{R\partial T} + \frac{I_{REF}}{R}\frac{\partial R}{\partial T}\right] \tag{5.5-31}$$

Using the results of Eqs. 5.5-20 through 5.5-23 in Eq. 5.5-31 gives

$$TC_F(I_{REF}) = \frac{1}{I_{REF}}\left[\frac{\alpha}{R} + \frac{1}{R}\sqrt{\frac{V_{DD}}{2K'_N R(W/L)}}\left(\frac{1}{R}\frac{\partial R}{\partial T} - \frac{3}{4T}\right)\right] - \left(\frac{1}{R}\frac{\partial R}{\partial T}\right) \tag{5.5-32}$$

Assuming that $I_{REF} = 100\ \mu$A, $K'_N = 24\ \mu$A/V^2, $V_{TN} = 0.75$ V, and $W/L = 10$ gives $V_{GS} = 1.663$ V. If $V_{DD} = 10$ V, then $R = 83.37$ kΩ. Finally if $\alpha = 2/3$ mV/°C and $TC_F(R) = 1500$ ppm/°C, the TC_F of the circuit of Fig. 5.5-3b is

$$TC_F(I_{REF}) = 216\ \text{ppm/°C} - 1500\ \text{ppm/°C} = -1284\ \text{ppm/°C} \tag{5.5-33}$$

Again, zero TC_F is possible. Setting Eq. 5.5-32 to zero and solving for $I_{REF}R$ gives

$$I_{REF}R = V_{DD} - V_{GS} = \frac{\alpha + \sqrt{(V_{DD}L)/(2K'_N RW)}[(1/R)(\partial R/\partial T) - (3/4T)]}{(1/R)(\partial R/\partial T)} \tag{5.5-34}$$

Using the above values in Eq. 5.5-34 gives a $V_{DD} = 2.863$ V for a zero $TC_F(I_{REF})$. This lower supply voltage causes R to become 28.63 kΩ. The above analysis is only approximate since in calculating the temperature change of V_{GS}, Eq. 5.5-16 rather than Eq. 5.5-15 was used. The chapter problems deal with the exact case.
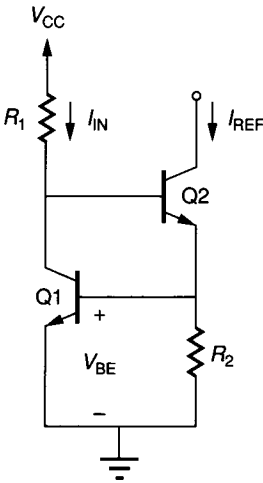
FIGURE 5.5-4
A method of obtaining a supply independent source by using V_{BE} to define the current.

So far, the references considered are not representative of stable voltage or current references. The remainder of the references presented will attempt to minimize the power supply dependence, the temperature dependence, or both. To achieve a reduction of the dependence of the current on the supply voltage, a technique of using the V_{BE} drop of a forward-biased pn junction is used. Such a circuit is shown in Fig. 5.5-4. Neglecting the base current, it follows from Eq. 3.3-10 that the reference current is expressed as

$$I_{REF} = \frac{V_{BE1}}{R_2} = \frac{V_t}{R_2} \ln\left(\frac{I_{IN}}{I_{S1}}\right) \qquad (5.5\text{-}35)$$

It can be shown that

$$S_{V_{CC}}^{I_{REF}} \approx \frac{V_t}{I_{REF}R_2} \qquad (5.5\text{-}36)$$

If $I_{IN} = 1$ mA, $I_{REF} = 100$ μA, and $I_{S1} = 0.4$fA, then from Eq. (5.5-35) $R_2 = 7.42$ kΩ. Therefore, the sensitivity of I_{REF} to V_{CC} is 0.035. Because the temperature performance of this current reference is not necessarily good and because the behavior is similar to that of Fig. 5.5-3a, it will not be pursued in further detail.

Another approach which uses the concept of generating the current from V_{BE} is shown in the bootstrap biasing circuit of Fig. 5.5-5a. The operating point of this circuit can be found by noting that if Q4 and Q5 are matched and if diode D1 is cutoff then these two devices form a simple unity gain current mirror. Neglecting base currents we obtain

$$I_{C1} = I_{C2} \qquad (5.5\text{-}37)$$

and

$$V_{BE1} = V_t \ln\left(I_{C1}/I_{S1}\right) = I_{C2}R_1 \qquad (5.5\text{-}38)$$
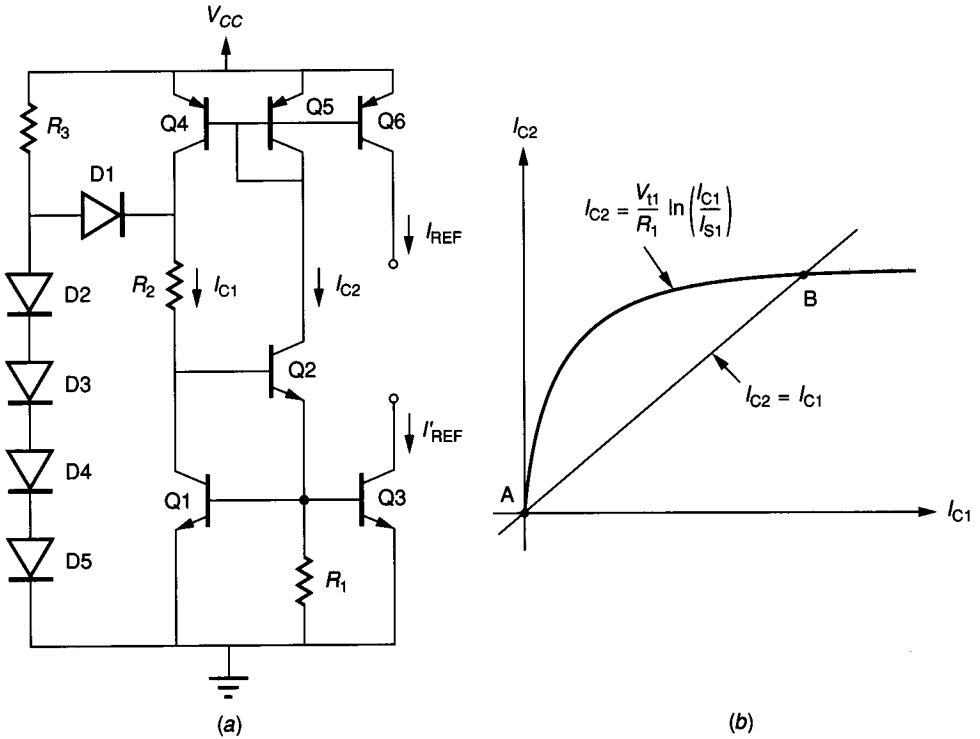
FIGURE 5.5-5
(a) A bootstrapped current source/sink, (b) Two possible operating points.

A closed form explicit expression for I_{C2} obtained by simultaneously solving Eqs. 5.5-37 and 5.5-38 in terms of basic functions does not exist. Plotting both Eqs. 5.5-37 and 5.5-38 on a curve of I_{C2} versus I_{C1} results in the curve of Fig. 5.5-5b. There are two operating points possible, designated as A and B. The operating point at A is undesirable since the value of $I_{C2}(I_{REF})$ is zero. Operation at the desired operating point, B, is determined by the start–up circuit consisting of R_3 and the five diodes. When V_{CC} is applied to the circuit, current flows through D_1 and R_2, forcing the circuit to the operating point at B. The value of $I_{C1}R_2$ is designed so that when the circuit is operating at B, D_1 is biased off disconnecting the start up circuit from the bootstrap current source/sink. Once the bootstrap current source/sink is operating at point B, the value of I_{REF} which is related to I_{C2} by the current mirror, Q5–Q6, should be independent of V_{CC}. I'_{REF} illustrates how a current sinking reference can be achieved.

The bootstrap current source can also be implemented in MOS technology as shown in Fig. 5.5-6a. The two equations corresponding to Eq. 5.5-37 and Eq. 5.5-38 are

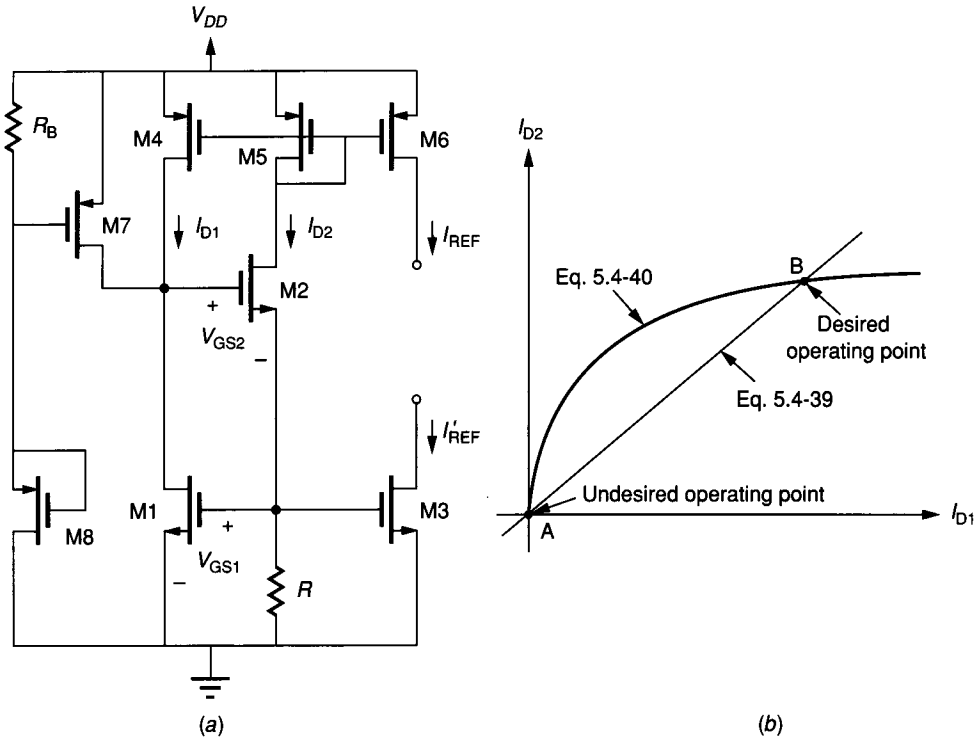$$I_{D1} = I_{D2} \qquad\qquad (5.5\text{-}39)$$

FIGURE 5.5-6
(*a*) A CMOS bootstrapped current source/sink, (*b*) Illustration of the two possible operating points.

and

$$I_{D2} = (V_{T1}/R) + \left[(2I_{D1}L_1/K'_N W_1)^{1/2}/R \right] \qquad (5.5\text{-}40)$$

Plotting Eq. 5.5-39 and Eq. 5.5-40 results in the curves shown in Fig. 5.5-6*b* where again two operating points are possible. R_B, M7, and M8 are used to start up the circuit, causing it to operate at point B. The values of V_{GS2} and V_{GS1} are designed so that M7 will be cutoff if the bootstrap current source/sink is operating at point B.

Both the BJT and MOS bootstrapped current sources represent good references for independence of power supply. However, second-order effects must be taken into account to achieve a minimum dependence. These second-order effects include the errors in current mirrors (see Sec. 5.4). Without including the second-order effects such as current mirror matching, the lower limit of power supply sensitivity is about 0.01 with these circuits.

In most silicon technologies it is possible to obtain a breakdown diode from a pn junction that is heavily doped on one side of the junction. In a bipolar process, a breakdown diode can be obtained by reverse biasing the base–emitter junction. In a CMOS process, a low voltage breakdown diode results from the

overlap of the p^+ and n^+ diffusions. The I–V characteristic of a breakdown diode is shown in Fig. 5.5-7. When the voltage V exceeds the breakdown voltage, BV, the I–V characteristic becomes nearly vertical. The slope of the breakdown diode characteristic can be approximated in this region by $1/r_z$ where r_z is the ac impedance of the breakdown diode in the high-conductance region.

A power supply–independent voltage reference using the breakdown diode is shown in Fig. 5.5-8. The power supply sensitivity can be expressed as

$$S_{V_{\text{cc}}}^{V_{\text{REF}}} = \frac{V_{\text{CC}}}{V_{\text{REF}}} \frac{\partial V_{\text{REF}}}{\partial V_{\text{CC}}} = \left(\frac{V_{\text{CC}}}{BV}\right)\left(\frac{v_{\text{ref}}}{v_{\text{cc}}}\right) = \left(\frac{V_{\text{CC}}}{BV}\right)\left(\frac{r_z}{r_z + r_{\text{out}}}\right) \qquad (5.5\text{-}41)$$

where v_{ref} and v_{cc} are the ac changes of V_{REF} and V_{CC} and r_{out} is the output resistance of the current source. If $BV = 6.5$ V, $V_{\text{CC}} = 10$ V, $r_z = 1000\ \Omega$ and $r_{\text{out}} = 100$ kΩ, the power supply sensitivity of Fig. 5.5-8 is 0.0065, which is the lowest power supply sensitivity of the circuits considered so far. It could be easily improved by using a current mirror having higher output resistance.

Unfortunately, the breakdown diode typically has a V_{REF} which is larger than 5 V. Such references can only be used with higher values of V_{DD} or V_{CC}.

The temperature coefficient of the breakdown diode depends on the doping levels and varies from negative values at low values of BV to positive values at higher values of BV. One must first measure the temperature coefficient before attempting to minimize the TC_F of the breakdown diode used as a voltage reference.

The TC_F of the MOS bootstrapped current source/sink of Fig. 5.5-6a can be found as

$$\text{TC}_F = \left(\frac{1}{V_{\text{T1}} + (I_{\text{D1}}L_1/K_N'W_1)^{1/2}}\right)\frac{\partial V_{\text{T1}}}{\partial T} - \frac{\partial R}{R\partial T} = \frac{1}{V_{\text{GS1}}}\frac{\partial V_{\text{T1}}}{\partial T} - \frac{\partial R}{R\partial T}$$
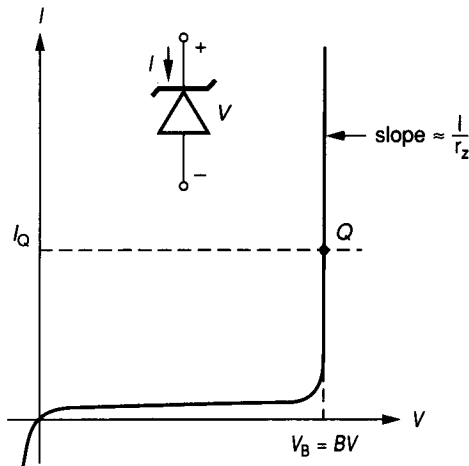
$$(5.5\text{-}42)$$

FIGURE 5.5-7
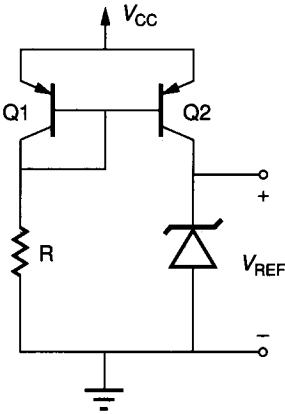Current–voltage characteristics of a breakdown diode.

FIGURE 5.5-8
Power supply–independent voltage reference using the breakdown diode.

where we have assumed that I_{D1} and K_N' are independent of temperature. If I_{D2} has been designed such that $V_{GS1} = 1.5$ V and the value of the temperature coefficient of V_T is -0.18 mV/°C and the fractional temperature coefficient of R is $+1500$ ppm/°C (polysilicon), then the TC_F of the MOS bootstrapped current/sink is

$$TC_F = -110 \text{ ppm/°C} - 1500 \text{ ppm/°C} = -1610 \text{ ppm/°C}$$

It is interesting to note in this and previous references that R is the major contributor to temperature variation.

One approach to reducing the TC_F of current references is to try to use the opposite temperature coefficients of breakdown diodes and pn junction diodes (diode connected transistors) to cancel the dependence of the source upon temperature. Figure 5.5-9 shows a voltage reference that has the possibility of achieving this objective. It is assumed that I_0 is sufficiently well-defined so that $V_B = BV$ can be assumed to be independent of V_{CC}. The reference voltage can be expressed as

$$V_{REF} = \left(\frac{R_2}{R_1 + R_2}\right) V_B - 2V_{BE}\left(\frac{R_2}{R_1 + R_2}\right) + V_{BE}\left(\frac{R_1}{R_1 + R_2}\right) \qquad (5.5\text{-}43)$$

assuming all V_{BE} are equal and all diodes are matched.

If Eq. 5.5-43 is differentiated with respect to T and set equal to zero, we get

$$-\frac{\partial V_B/\partial T}{\partial V_{BE}/\partial T} = \frac{R_1}{R_2} - 2 \qquad (5.5\text{-}44)$$

But if the temperature dependence of the breakdown diode is $+3$ mV/°C, then

$$\frac{\partial V_B/\partial T}{\partial V_{BE}/\partial T} \cong \frac{+3 \text{ mV/°C}}{-2 \text{ mV/°C}} \qquad (5.5\text{-}45)$$

Therefore, the ratio of R_1/R_2 for zero temperature dependence is 3.5. The value of V_{REF} under this constraint is $(2/9)V_B$ or approximately 1.4 V. The voltage reference of Fig. 5.5-9 should also be relatively independent of V_{CC}.
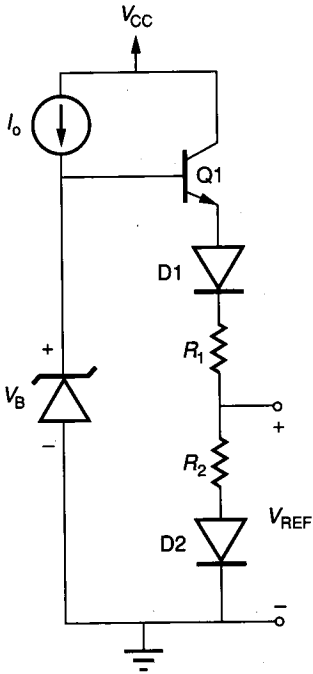
FIGURE 5.5-9
Use of cancellation between pn diode and breakdown diode temperature coefficients to obtain a temperature independent voltage reference.

One of the more popular and successful approaches to achieving a voltage reference, which is independent of both supply and temperature, is the *bandgap voltage reference*. The concept behind the bandgap voltage reference is illustrated in Fig. 5.5-10. A voltage V_{BE} is generated from a pn junction diode having a temperature coefficient of -2 mV/°C at room temperature. Also a voltage
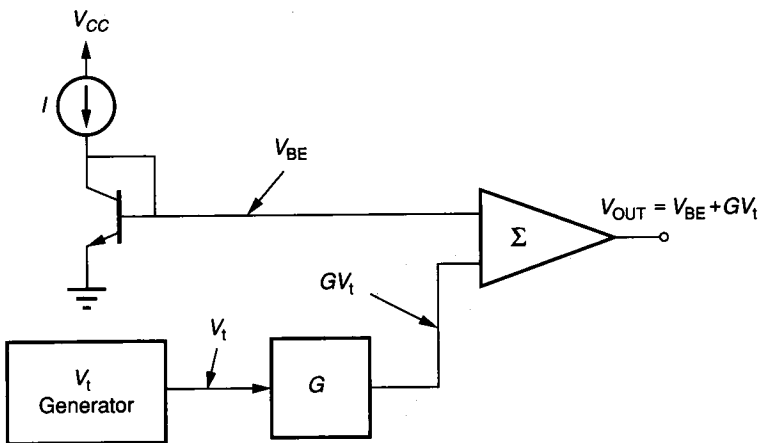

FIGURE 5.5-10
General concepts of a bandgap voltage reference.

$V_t (V_t = kT/q)$ is generated that has a temperature coefficient of $+0.085$ mV/°C at room temperature. If the V_t voltage is multiplied by a constant G and summed with the V_{BE} voltage, then the output voltage is given as

$$V_{REF} = V_{BE} + GV_t \qquad (5.5\text{-}46)$$

On a first order basis, the value of G would be that which gives a zero value of temperature coefficient for V_{REF}. This value of G corresponds to 23.5 and produces a reference voltage of 1.26 V assuming V_{BE} is 0.65 V. A more detailed analysis is necessary to design the bandgap voltage reference so that zero temperature coefficient is achieved over a wide range of temperatures.[7]

A BJT version of the bandgap voltage reference is shown in Fig. 5.5-11. This voltage reference is called the Widlar bandgap reference.[8] As V_{CC} is increased from zero, Q1 and Q2 conduct when V_{BE1} is approximately 0.7 V. Since R_2 is greater than R_1, Q2 saturates. Further increase of V_1 (due to increasing V_{CC} during turn on) causes Q2 to come out of saturation due to R_3. The circuit stabilizes at $V_{BE3} = V_{BE}$ (on). Q1, Q2, and R_3 form a Widlar current mirror, as was discussed in Sec. 5.4. The current I_2 can be expressed as

$$I_2 = \frac{V_t}{R_3} \ln\left(\frac{I_1}{I_2}\right) \qquad (5.5\text{-}47)$$

Equation 5.5-47 shows that the voltage V_t in Fig. 5.5-10 is generated by the difference between two base–emitter drops. The reference voltage of Fig. 5.5-11 can be given as

$$V_{REF} = V_{BE3} + \left(\frac{R_2}{R_3}\right) V_t \ln\left(\frac{I_1}{I_2}\right) \qquad (5.5\text{-}48)$$
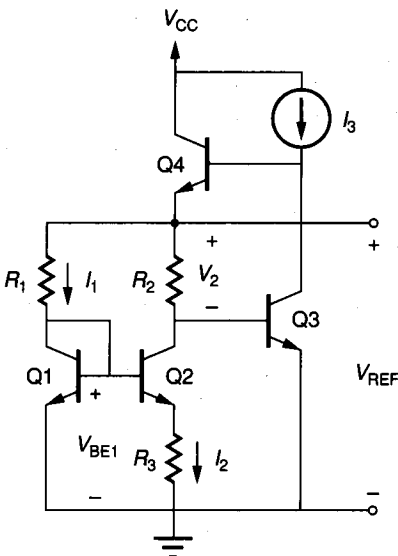

FIGURE 5.5-11
Widlar bandgap voltage reference.

Comparing (5.5-48) with (5.5-46) shows that

$$G = \left(\frac{R_2}{R_3}\right) \ln\left(\frac{I_1}{I_2}\right) \qquad (5.5\text{-}49)$$

If we assume that $I_1/I_2 = 10$, then at room temperature we must have $R_2/R_3 = 10.2$ to obtain a zero temperature coefficient. Selecting $I_1 = 1$ mA gives $I_2 = 0.1$ mA and R_3 is found from Eq. 5.5-47 as 60 Ω. Thus, R_2 is 610 Ω. If we assume that $V_{BE3} = 0.65$ V, then V_{REF} is equal to 1.26 V. Figure 5.5-12 shows that the bandgap reference possesses zero temperature coefficient only around a nominal temperature. Another problem with this circuit is the dependence of I_3 on the supply voltage. Better implementations of the bandgap reference are discussed below.

An improved bandgap voltage reference can be developed using an op amp, as shown in Fig. 5.5-13a and b. The advantage of the op amp is to remove the dependence of the currents upon the power supply. The method by which this is done is to force the relationship

$$I_1 R_1 = I_2 R_2 \qquad (5.5\text{-}50)$$

and to replace I_1/I_2 in the argument of the logarithm by R_2/R_1 which is independent of supply voltage. The performance of both the circuits is identical and can be described as follows. The current I_2 is found by writing a voltage loop equation around V_{BE1}, V_{BE2} and R_3, resulting in

$$I_2 = \frac{1}{R_3} V_T \ln\left(\frac{R_2 I_{S2}}{R_1 I_{S1}}\right) \qquad (5.5\text{-}51)$$

The reference voltage can be expressed as

$$V_{REF} = V_{BE1} + I_2 R_2 = V_{BE1} + \frac{R_2}{R_3} V_t \ln\left(\frac{R_2 I_{S2}}{R_1 I_{S1}}\right) \qquad (5.5\text{-}52)$$
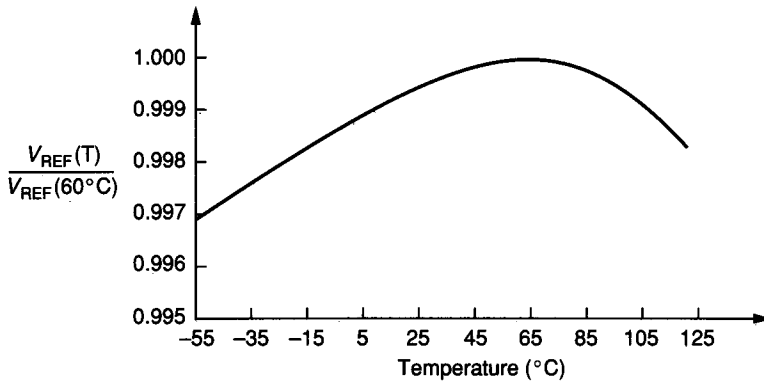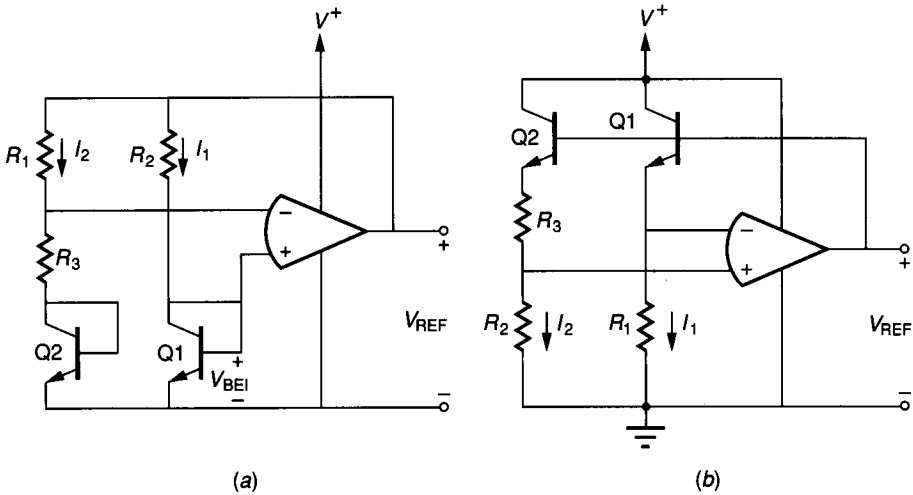

FIGURE 5.5-12
Illustration of the temperature dependence of the Widlar bandgap voltage reference.

FIGURE 5.5-13
(a) A bandgap voltage reference using an op amp, (b) An alternate form of (a).

which is of the same form as the expression in Eq. 5.5-46. The areas of the emitters of transistors Q1 and Q2 are used to scale the argument of the logarithm. For example, if $A_{E2} = 10A_{E1}$, then $I_{S2} = 10I_{S1}$ and for zero temperature coefficient we find that $R_2/R_3 = 10.2$ if $R_2/R_1 = 1$.

The bandgap voltage reference of Fig. 5.5-10 can be implemented by either bipolar or CMOS technology. Q1 and Q2 would be the substrate transistors, which are available in CMOS technology. For p-well CMOS using an n^- substrate, the BJT is an npn substrate transistor and would be compatible with Fig. 5.5-13b. For an n-well CMOS technology using a p^- substrate, the circuit of Fig. 5.5-13a can be used if Q1 and Q2 are replaced by pnp transistors.

Exact cancellation of the dependence of V_{REF} upon temperature will not be possible because of component tolerances and second-order effects such as the nonlinearity of the dependence of V_{BE} on temperature[9] which has been neglected. Problem 5.41 shows that the influence of the op amp offset voltage is multiplied by $(1 + R_2/R_1)$ and can become a significant source of error and temperature dependence. Offset effects may be reduced by using multiple pn junctions or by offset canceling techniques.

Q1 and Q2 of Fig. 5.5-13 can be replaced by MOS devices operating in the weak inversion region if the current levels are small. Such voltage references use very little power. In the weak inversion region, the I–V characteristics of the MOS transistor are exponential and can be used to generate V_t. An equation describing the MOS transistor in weak inversion is given as (see (Eq. 3.1-32)[10]

$$I_D = \frac{W}{L} I_{DO} e^{-V_{BS}[(1/n\,V_t) - (1/V_t)]} (1 - e^{-V_{DS}/V_t}) e^{(V_{GS} - V_T)/n\,V_t} \qquad (5.5\text{-}53)$$

where $V_t = kT/q$
         n = slope factor
         I_{DO} = characteristic current

Eq. 5.5-53 only holds for the weak inversion region where $V_{DS} > 3V_t$. It is found[11] that n is controllable but has a strong temperature dependence. I_{DO} is difficult to control and also has a strong temperature dependence. A voltage reference using the above concepts was proposed by Tsividis and Ulmer[12]. While the reference voltage of this circuit was independent of I_{DO}, it was dependent upon n, which prevented satisfactory reduction of the temperature coefficient. A CMOS bandgap voltage reference which eliminated the dependence on n is shown in Fig. 5.5-14. The current mirrors M1–M3 and M2–M4 form a closed loop with an initial loop gain greater than unity. Therefore, the current in both branches increases until equilibrium is achieved when the loop gain is reduced to one by the voltage V_{R1} across R_1. If we assume that M1 through M4 operate in the weak inversion region and that V_{DD} is high enough to ensure saturation of M1 and M4, then V_{R1} can be expressed as follows where $S = W/L$

$$V_{R1} = V_t \ln\left(\frac{S_1 S_4}{S_2 S_3}\right) \tag{5.5-54}$$

Note that V_{R1} depends only on the thermal voltage and the ratio of the geometry of the devices and is independent of n. I_{R1} and I_E are related as

$$\frac{I_{R1}}{I_E} = \frac{S_3}{S_6} \tag{5.5-55}$$
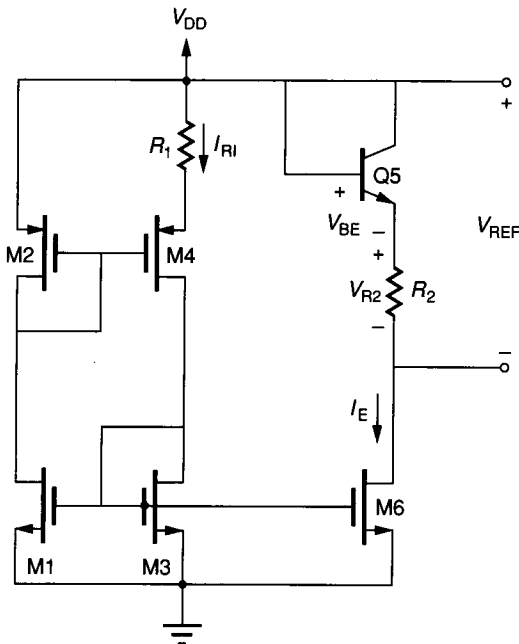

FIGURE 5.5-14
A CMOS bandgap voltage reference operating in weak inversion with no dependence on the process parameter n.

Solving for I_E gives

$$I_E = \left(\frac{S_6}{S_3}\right)\frac{V_t}{R_1} \ln\left(\frac{S_4 S_1}{S_2 S_3}\right) \tag{5.5-56}$$

V_{REF} is given as

$$V_{REF} = V_{BE} + I_E R_2 = V_{BE} + \left(\frac{R_2}{R_1}\right)\left(\frac{S_6}{S_3}\right)V_t \ln\left(\frac{S_1 S_4}{S_2 S_3}\right) \tag{5.5-57}$$

An expression for V_{BE} which emphasizes its temperature dependence is given by[13]

$$V_{BE}(T) = V_{GO}(1 - \frac{T}{T_o}) + V_{BEO}(\frac{T}{T_o}) + \frac{mkT}{q} \ln\left(\frac{T_o}{T}\right) \tag{5.5-58}$$

where V_{GO} = the extrapolated bandgap voltage of silicon
$\quad\quad V_{BEO}$ = V_{BE} of a diode connected transistor at $T = T_o$
$\quad\quad m$ = constant dependent on the diode fabrication and temperature characteristics

It can be shown that the condition for $dV_{REF}/dT = 0$ is given by

$$\left(\frac{R_2 S_6}{R_1 S_3}\right)\ln\left(\frac{S_1 S_4}{S_2 S_3}\right) = \frac{q(V_{GO} - V_{BEO})}{kT} + m \tag{5.5-59}$$

This results in a reference voltage of

$$V_{REF} = V_{GO} + \frac{mkT}{q} \tag{5.5-60}$$

In order to ensure proper operation of the voltage reference described, the following precautions must be taken. First, the devices must be in weak inversion even at the highest temperature of operation. Secondly, leakage currents particularly in the n-channel devices must be minimized to prevent these currents from becoming a major source of error at higher temperature. Lastly, the output resistance of the devices must be large enough to ensure proper operation of the devices as current mirrors. This can be accomplished by using long devices or by use of the various current mirrors presented earlier.

This section has introduced the techniques and methods used to design voltage and current references that minimize their dependence on power supply and/or temperature. There are other characteristics of references which are important but are beyond the scope of the treatment given in this section. One of these is the noise introduced by the reference. Noise can be reduced by minimizing the number of devices and using small values of resistance. If MOS devices are used, p-channel MOS devices generally have less noise and the noise is reduced if the area of the device is increased.

Another area that was not covered was the creation of a voltage reference from a current reference and vise versa. At least one resistor will be present in this conversion process and cause the TC_F to be different. These conversions are best accomplished by using an op amp as a current-to-voltage or voltage-to-current converter.

5.6 SUMMARY

Five categories of building blocks have been presented in this chapter. These categories include switches, active resistors, current sources and sinks, current mirrors/amplifiers, and voltage and current references. Figures 5.0-1 and 5.0-2 show how these basic building blocks can be used to design or build more complex circuits. This chapter has paved the way to combine these building blocks with others to be discussed in the next chapter to form analog circuits.

The material discussed in this chapter has provided the opportunity to describe and illustrate many important principles and concepts that can be used in other applications. The section on active resistors illustrated methods by which the drain current dependence on the drain–source and the bulk–source voltage can be minimized. The use of switches and capacitors to implement a resistor was presented. Both positive and negative feedback were used to increase the small signal output resistance of current sources and sinks. Negative series feedback was used to increase the resistance while positive feedback was used for bootstrapping a resistor, increasing its effective resistance. The principles of replication and analyzing mismatched devices were demonstrated in the section describing current mirrors/amplifiers.

Finally, the last section introduced techniques which reduced the influence of temperature and power supply variation on the value of a voltage or current reference. It was shown how the temperature dependence can be reduced to zero in some cases.

REFERENCES

1. M. Banu and Y. Tsividis: "Floating Voltage–Controlled Resistors in CMOS Technology," *Electronic Letters*, vol. 18, no. 15, pp. 678–679, July 1982.
2. M. Banu and Y. Tsividis: "Fully Integrated Active RC Filters in MOS Technology," *IEEE J. of Solid–State Circuits*, vol. SC–18, no. 6, pp. 644–651, December 1983.
3. E. Sackinger and W. Guggenbuhl: "A Versatile Building Block: The CMOS Differential Difference Amplifier," *IEEE J. of Solid–State Circuits*, vol. SC–22, no. 2, pp. 287–294, April 1987.
4. G. R. Wilson: "A Monolithic Junction FET–NPN Operational Amplifiers," *IEEE J. of Solid–State Circuits*, vol. SC–3, no. 4, pp. 341–349, December 1968.
5. R. C. Jaeger: "A High Output Resistance Current Source," *IEEE J. of Solid–State Circuits*, vol. SC–9, no. 4, pp. 192–194, August 1974.
6. R. J. Widlar: "Some Circuit Design Techniques for Linear Integrated Circuits," *IEEE Transactions on Circuit Theory*, vol. CT–12, no. 4, pp. 586–590, December 1965.
7. P. R. Gray and R. G. Meyer: *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, New York, pp. 254–258, 1977.
8. R. J. Widlar: "New Developments in IC Voltage Regulators," *IEEE J. of Solid–State Circuits*, vol. SC–6, no. 1, pp. 2–7, February 1977.
9. G. C. M. Meijer, P. C. Schmale, and K. van Zalinge: "A New Curvature–Corrected Bandgap Reference," *IEEE J. of Solid–State Circuits*, vol. SC–17, no. 6, pp. 1139–1143, December 1982.
10. E. Vittoz and J. Fellrath: "CMOS Analog Integrated Circuits Based on Weak Inversion Operation," *IEEE J. of Solid–State Circuits*, vol. SC–12, no. 3, pp. 224–231, June 1977.
11. G. Tzanateas, C. Salama and Y. Tsividis: "A CMOS Bandgap Voltage Reference," *IEEE J. of Solid–State Circuits*, vol. SC–12, no. 3, pp. 655–657, June 1979.
12. Y. P. Tsividis and R. W. Ulmer: "CMOS Reference Voltage Source," *ISSCC Digest of Technical Papers*, pp. 49–59, February 1978.
13. J. S. Brugler: "Silicon Transistor Biasing for Linear Collector Current Temperature Dependence," *IEEE J. of Solid–State Circuits*, vol. SC–2, no. 2, pp. 57-58, June 1967.

PROBLEMS

Section 5.1

5.1. What causes the nonsymmetry between the first and third quadrants in Fig. 5.1-4 for the MOS switch?

5.2. Assume a switch is made from a MOS transistor with equal W and L. If the CMOS parameters in Table 3.1-2 are applicable to this transistor, what are the highest and lowest values of voltages that can exist on the source/drain when the bulk is at -5 V and the gate at 5 V and still keep the switch on and working properly? Define the switch as on when the switch large signal resistance is 20 kΩ or less.

5.3. Calculate R_{ON} for the transistor of Fig. 5.1-5 when $V_{GS} = 5V_T$ and $W = L$ for $V_{BS} = 0$ V, $V_{DS} \simeq 0$, and for $V_{BS} = 5$ V. Assume that $\gamma = 0.8$ V$^{-0.5}$ and $\phi = 0.6$ V.

5.4. Find R_{ON} of an n-channel MOS switch if $V_D \approx V_S = 2$ V, $V_B = 0$ V and $V_G = 5$ V if $W = L$ and the n-channel parameters of Table 3.1-2 are applicable.

5.5. Calculate the voltage feedthrough from the clock of Fig. 5.1-13a to C_1 of Fig. 5.1-13b (a) if C_1 is 5 pF and (b) if C_1 is 1 pF and $C_{GD} = C_{GS} = 50$ fF.

5.6. Use the SPICE computer simulation program to plot the on resistance of the circuit of Fig. 5.1-15 if $W/L = 10$ for all transistors. Assume that $V_{DD} = 5$ V and that $\overline{\phi}$ is 0 V and ϕ is 5 V. Use the parameters of Table 3.1-2 and obtain a plot of R_{ON} as a function of the voltage at the switch terminals to ground from 0 to 5 V. Note that because the switch is on, that the terminal voltages should be approximately equal.

Section 5.2

5.7. Evaluate the ac and dc resistance of the circuit of Fig. 5.2-2a when $V = 2V_T$ using the model parameters of Table 3.1-2. Repeat for the circuit of Fig. 5.2-2b. Assume that the source and bulk are connected together.

5.8. Use the small signal model of Fig. 5.2-2d to rederive Eq. 5.2-5 and include the bulk effect assuming that V_{BS} is positive.

5.9. Evaluate the ac and dc resistance of the circuit of Fig. 5.2-3a when $V = 0.6$ V using the model parameters of $I_s = 0.4$ fA and $\beta_F = 100$ at room temperature.

5.10. Repeat Ex. 5.2-1 if V_{out} is to be -1 V.

5.11. Repeat Ex. 5.2-2 if the bulk–source voltages are not neglected using the bulk threshold parameter of Table 3.1-2.

5.12. If W/L of M1 and M2 of Fig. 5.2-6 is 5, find the value of V_C necessary to realize an ac resistance of 2000 Ω using the model parameters of Table 3.1-2. Compare your results with that of Fig. 5.2-8a.

5.13. If the difference between V_{C1} and V_{C2} can vary from 1 to 5 V and W/L can vary from 1 to 10, what range of ac resistance can the double-MOS resistor implementation of Fig. 5.2-9 realize?

5.14. Use the double-MOS ac resistor configuration of Fig. 5.2-9 to implement the voltage amplifier shown in Fig. P5.14. The op amp is an ideal, differential-in, differential-out op amp. Assume that $V_{C1} = 5$ V and $V_{C2} = 4$ V. Use the parameters of Table 3.1-2.

5.15. Use the approach illustrated in the text for the parallel switched capacitor of Fig. 5.2-11 to show that the equivalent resistance of the series–parallel switched capacitor resistor realization of Fig. 5.2-13 is given by Eq. 5.2-32.

5.16. Use the approach illustrated in the text for the parallel switched capacitor of Fig. 5.2-11 to show that the equivalent resistance of the bilinear switched capacitor resistor realization of Fig. 5.2-14 is given by Eq. 5.2-33.
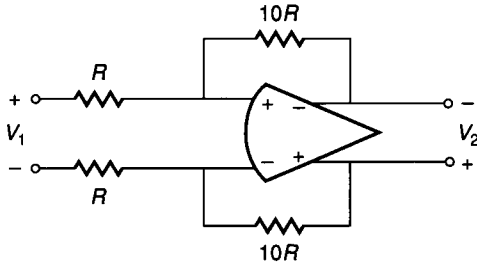
FIGURE P5.14

5.17. Figure P5.17 shows an inverting integrator. If R_1 is replaced by the series switched capacitor realization of Fig. 5.2-12, find an approximation expression for the transfer function, $V_2(s)/V_1(s)$. What is the accuracy of the integration constant $(1/R, C_2)$ in terms of the accuracy of the capacitors and the clock frequency?

Section 5.3

5.18. Assume that the model parameters of the npn transistor of Fig. 5.3-4a are $I_S = 0.4$ fA and $V_{AF} = 200$ V. Find the value of V_{BB} which will give a current sink of 500 μA. Using the values of Table 3.2-2, V_{MIN} and the value of the ac output resistance.

5.19. Use the model parameters of Table 3.1-2 for the MOS current sink of Fig. 5.3-5a to find V_{GG}, V_{MIN}, and R_o if the current is to be 500 μA.

5.20. Verify Eq. 5.3-8 for the MOS current sink of Fig. 5.3-7.

5.21. Verify Eqs. 5.3-15 and 5.3-16 for the bootstrapped current sink of Fig. 5.3-12.

5.22. Verify Eq. 5.3-19 for the output resistance of Fig. 5.3-15a.

5.23. Discuss a BJT realization of the regulated cascode MOS current sink of Fig. 5.3-16a. Give a schematic of a possible realization and find the output resistance and the minimum voltage drop across the current sink.

5.24. Verify Eq. 5.3-20 for the output resistance of Fig. 5.3-16a.

Section 5.4

5.25. Consider the circuit of Fig. 5.4-1 as a current amplifier. The input current will consist of a dc and an ac current. If the dc input current is 1 mA, find the ac input resistance, the ac output resistance, and the ac current gain (i_{out}/i_{in}) if $I_S = 0.4$ fA, $\beta_F = 100$, and $V_{AF} = 200$ V.

5.26. Find the ac input resistance of the circuit of Fig. 5.4-3 looking from R_1 toward the base of Q3 and collector of Q1. Compare this input resistance to that of the circuit of Fig. 5.4-1.
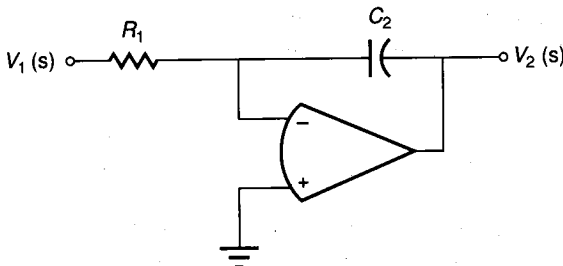

FIGURE P5.17

5.27. Verify Eqs. 5.4-33 and 5.4-34 of the BJT Wilson current mirror in Fig. 5.4-6.

5.28. Verify the ac output resistance of the BJT Widlar current mirror given in Eq. 5.4-41.

5.29. Assume that the output current is 0.5 mA for the BJT current mirrors listed in Table 5.4-1. Assume that the npn BJT parameters are $I_S = 0.4$ fA, $\beta_F = 100$, $V_{AF} = 200$ V, $V_{BE}(sat) = 0.7$ V and $V_{CE}(sat) = 0.2$ V. Find the value of r_{out} and V_{MIN} for each of the mirrors of Table 5.4-1.

5.30. Consider the circuit of Fig. 5.4-11a as a current amplifier. The input current will consist of a dc and an ac current. If the dc input current is 0.1 mA, find the ac input resistance, the ac output resistance, and the ac current gain (i_{out}/i_{in}) using the model parameters of Table 3.1-2 and assuming that both W/L values are equal.

5.31. Verify the ac output resistance of the MOS Wilson current mirror given in Eq. 5.4-63.

5.32. Develop a MOS realization of the BJT Widlar current mirror and find an expression for the output resistance and minimum voltage drop across the output of the mirror.

5.33. Assume that the output current is 0.2 mA for the MOS current mirrors listed in Table 5.4-2. Using the model parameters of Table 3.1-2 and assuming all W/L values are equal, find the value of r_{out} and V_{MIN} for each of the mirrors of Table 5.4-2.

Section 5.5

5.34. Redevelop Eq. 5.5-9 for the sensitivity of Fig. 5.5-1b when V_{CC} is not much greater than V_{REF}.

5.35. Use two collector–base connected BJTs in series in place of the single collector–base connected BJT in the circuit of Fig. 5.5-1b and find an expression for the sensitivity of V_{REF} with respect to V_{CC}.

5.36. If $V_{DD} = 10$ V, $W/L = 5$, and $R = 50$ kΩ, find the value of V_{REF} of the cirucit of Fig. 5.5-1c. Use the model parameters of Table 3.1-2. Assume that the TC_F of R is $+1000$ ppm/°C and find the TC_F of V_{REF}.

5.37. Assume for the circuit of Fig. 5.5-2a that $V_{CC} = 10$ V, $R_2 = 2R_1 = 2$ MΩ, $R = 100$ kΩ, and $I_S = 0.4$ fA. Assume also that $I_{R2} \ll I_C$ and find V_{REF}.

5.38. Repeat the development leading to Eq. 5.5-34 which gives the conditions for a zero TC_F using Eq. 5.5-15 rather than Eq. 5.5-16. Evaluate the value of V_{DD} for the conditions given in the text.

5.39. Assume that the voltage V_{GS} in Fig. P5.39 is independent of temperature. Develop an expression that will give the value of V_{GS} necessary to achieve a drain current,
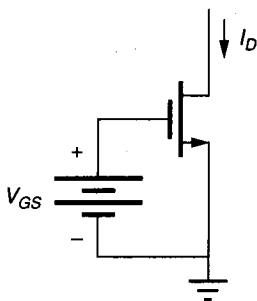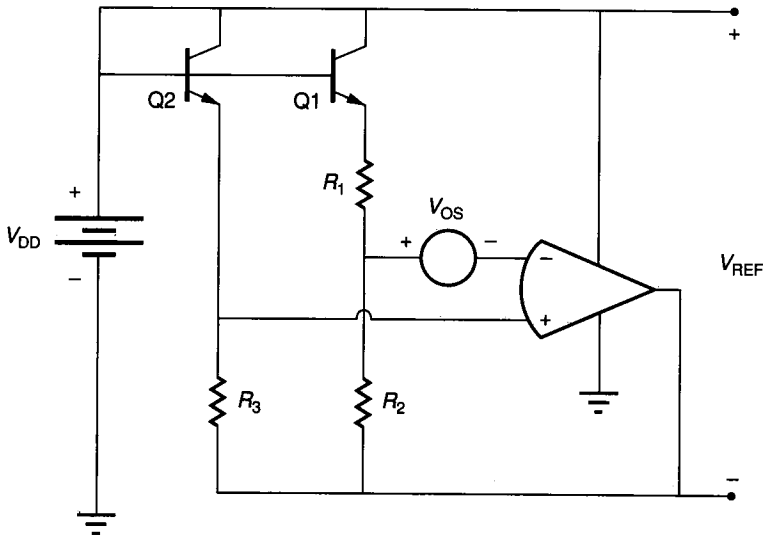

FIGURE P5.39

FIGURE P5.40

I_D, which will have zero temperature dependence. Assume that the temperature dependence of the MOS transistor is given by Eqs. 5.5-18 and 5.5-19. Find the value of V_{GS} and I_D which gives zero temperature dependence at (a) $T = 27°C$ and (b) $T = 200°C$.

5.40. For the bandgap voltage reference of Fig. P5.40, assume that the emitter area of Q1 is 10 times that of Q2, $V_{BE2} = 0.7$ V, $R_2 = R_3$, and $V_t = 0.026$ V. Find the value of R_2/R_1 necessary to give zero temperature coefficient at room temperature. For this problem assume $V_{OS} = 0$.

5.41. Develop an expression for V_{REF} for Fig. P5.40 if V_{OS} is not zero. Assume that R_2/R_1 is 10 and use the conditions of the previous problem to find V_{REF} if V_{OS} is 10 mV.

Design Problems

5.42. Design a switch using MOS technology which when closed will allow an uncharged 10 pF capacitor to be connected to a 5 V dc voltage source. The capacitor should reach 4.95 V within 10 ns. What is the value of the clock voltage which will meet this specification? Assume that the MOS technology to be used is defined by Table 3.1-2. Minimize the switch area in order to minimize the clock feedthrough.

5.43. Design a voltage divider which will provide 1 V dc from a 5 V dc voltage source. The temperature coefficient of the 1 V dc should not be larger than that of the 5 V dc voltage source. The sensitivity of the 1 V dc to changes in the 5 V dc supply should be less than 0.05. Keep the power dissipation of this voltage divider to less than 0.1 mW.

5.44. Design a current source having a value of 100 μA, output resistance of greater than 1 MΩ, and a minimum voltage of at most 1 V. Assume that ± 5 V power supplies are available. The design should be complete in the sense that when an external resistor is connected to it (the other end of the resistor is at -5 V) that 100 μA flows.

5.45. Use the current mirror concept to design a differential, current input amplifier which will provide an output current which is proportional to the difference between two input currents. Choose the gain control as 10 so that the expression

$$I_{out} = 10(I_1 - I_2)$$

is realized. The input resistances of this amplifier should be less than 1 kΩ and the output resistance should be greater than 1 MΩ. Assume that ± 5 V power supplies are available.

5.46. Design a bandgap voltage reference using the form of Fig. 5.5-13a or 5.5-13b. Use this bandgap voltage reference to design a dc current reference which doesn't deteriorate the temperature characteristics of the bandgap voltage. Assume that ± 5 V power supplies are available.