CHAPTER 6

AMPLIFIERS

6.0 INTRODUCTION

This chapter uses the building blocks of the last chapter to develop basic analog circuits and amplifiers. This material represents the middle step in the analog design hierarchy of Table 5.0-1. The primary focus of this chapter is the development of integrated circuit amplifiers using the building blocks of the last chapter. The concepts illustrated in Figs. 5.0-1 and 5.0-2 will be implemented in the following material.

The circuits included in this chapter are the inverting amplifier, the improved inverting amplifier, the differential amplifier, the output amplifier, the operational amplifier, and the comparator. The inverting amplifier, sometimes called an inverter, is one of the primary gain stages of analog amplifiers. The performance of the inverting amplifier can be improved as discussed in Sec. 6.2 by the use of additional devices. These additional devices typically appear in the cascode configuration, and are often termed *cascode amplifiers*. The improvements are not only in the area of performance, but also in the area of more degrees of design freedom.

Next in importance to the inverting amplifier is the differential amplifier. It is very useful as an input stage and is highly compatible with integrated circuit technology. The next one-stage amplifier to be considered is the output amplifier. This amplifier is necessary to interface the output of an amplifier to a low-resistance or low-capacitance load. Normally, amplifiers are incapable of driving a low-resistance/high-capacitance load. The output amplifier is difficult to design since it requires large, linear output swings across low resistive loads.

These amplifiers can be combined in the manner suggested by Figs. 5.0-1 and 5.0-2 to result in an operational amplifier. The operational amplifier is often considered the most useful circuit in analog integrated circuit design. It represents a good example in implementing circuit functions independent of its own performance characteristics using negative feedback. The last circuit presented in this chapter is the comparator. It is a circuit used to detect voltage thresholds and finds use in many analog and digital functions.

The emphasis of this chapter varies as the material progresses. The focus of the sections on inverting and differential amplifiers is on the small signal performance. This includes the ac gain, input and output resistances, bandwidth, and noise. These amplifiers are typically used as input or interstage amplifiers and do not have large signal swing requirements. The focus shifts to large signal considerations for output amplifiers. Here the key performance aspects include large signal swing, linearity, efficiency, and low output impedance. In operational amplifiers, the emphasis includes both small signal and large signal considerations. For the comparator, the focus is primarily on the large signal transient performance.

6.1 INVERTING AMPLIFIERS

One of the most useful amplifiers is the inverting amplifier, also called the inverter. As its name implies, the inverter produces an output that is inverted with respect to the input. If the input signal is changing in a positive (negative) manner, then the output will be changing in a negative (positive) manner. The inverter is widely used in both analog and digital circuits. In digital circuits, the inverter accomplishes the Boolean operation of negation or inversion. In analog circuits, the inverter is used to achieve amplification. Topologically, the simple analog and digital inverters are often identical. The use of the inverter in digital circuits will be described in more detail in Chapter 7. This section will examine the use of the inverter in analog circuits.

Coverage of the inverter naturally follows the material presented in the last chapter. Descriptions of the various forms of the inverter will use concepts from each section of Chapter 5, particularly the sections on active resistors and current sources/sinks. This section will be divided into three parts. The first part will present the general concepts of the inverter, independent of the technology used to implement it. The second part will examine inverters that use MOS technology. The last part will examine inverters using BJT technology.

The inverting amplifiers discussed in this section will be restricted to small signal, linear applications. Consequently, the emphasis will be on the fundamental concepts, the various inverter architectures, the small signal performance, and the noise performance. Large signal considerations, such as power dissipation, signal swing, nonlinearity and efficiency, will be emphasized in the section dealing with output amplifiers.

6.1.1 General Concepts of Inverting Amplifiers

The objective of the inverting amplifier used in analog circuits is to provide an inverting, small signal voltage gain greater than 1. One can appreciate the advantage of the inverting amplifier over a noninverting amplifier by noting that two cascaded inverters can implement a noninverting amplifier, but a noninverting amplifier cannot implement an inverting amplifier. Although inverting amplifiers are not restricted to voltage input and output variables, this form of the inverter will be considered here.

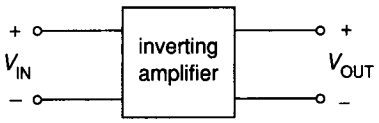


FIGURE 6.1-1
Two-port representation of an inverting voltage amplifier.

Figure 6.1-1 shows a two-port representation of the inverting voltage amplifier. The inverter can be characterized by the transfer characteristics defining the dependence of V_{OUT} on V_{IN}, the input resistance (R_{IN}), and the output resistance (R_{OUT}). In this section the characterization of the inverter is from the small signal viewpoint. Thus, an inverting voltage amplifier would be characterized by the small signal voltage gain, $v_{out}/v_{in} = A_v$, the small signal input resistance, r_{in}, and the small signal output resistance, r_{out}. It is necessary that the value of A_v should be negative and greater than unity. It is desirable but not necessary to have r_{in} large and r_{out} small.

The small signal performance of the inverter can be further characterized in the frequency or time domain. In the frequency domain, $A_v(\omega)$ of the ideal inverter should have a magnitude, A_{v0}, independent of frequency and a phase shift of $\pm 180°$. At some frequency, the magnitude of $A_v(\omega)$ of the practical inverter will decrease. The frequency at which the magnitude of $A_v(\omega)$ is equal to $A_{v0}/\sqrt{2}$ is called the -3 dB frequency ($\omega_{-3\text{ dB}}$). Although inverters built from discrete components may have a finite lower -3 dB frequency (due to coupling capacitors), the gain of integrated circuit inverters is A_{v0} for all frequencies sufficiently below $\omega_{-3\text{dB}}$. Thus the bandwidth of the inverter is equal to $\omega_{-3\text{dB}}$. It is important that the inverter have sufficient bandwidth for its given application.

The small signal frequency response can alternately be characterized by the small signal time domain response. For the case just discussed, the inverter acts as a low-pass amplifier with a cutoff frequency of $\omega_{-3\text{dB}}$. The pulse response of a first-order system would be characterized by a 10% to 90% rise time given approximately as $2.2/\omega_{-3\text{dB}}$. Another important aspect of the small signal performance of the inverter is noise. In many cases, the inverter is used as an input stage for a more complex amplifier. In order to reduce the noise of the complex amplifier, it is important to reduce the noise of the input stage.

In its most simple form, the inverting amplifier can be represented by two blocks. One of the blocks is a voltage-controlled current source, and the other is a load. It is important to recognize two types of voltage-controlled current sources. The distinction will be based on Fig. 5.3-2, which defined a current sink and a current source. In this case, the currents are controlled by the voltage at a third terminal. We shall define the blocks in Fig. 6.1-2 to schematically represent a voltage-controlled current sink and a voltage-controlled current source. V_P and V_N are defined as the most positive and negative dc voltages, respectively. The notation G will be used to designate a voltage-controlled current sink/source. The voltage-controlled current sinks/sources of Fig. 6.1-2 are three-terminal devices. The terminals are designated I for input, O for output, and X for the terminal common with V_N or V_P. The voltage between terminals I and X (X and I) controls the current at terminal O for Fig. 6.1-2*a* (Fig. 6.1-2*b*). In general, I_O for Fig. 6.1-2*a* can be expressed as

$$I_O = g_{sink}(V_{IX}, V_{OX}) \tag{6.1-1}$$

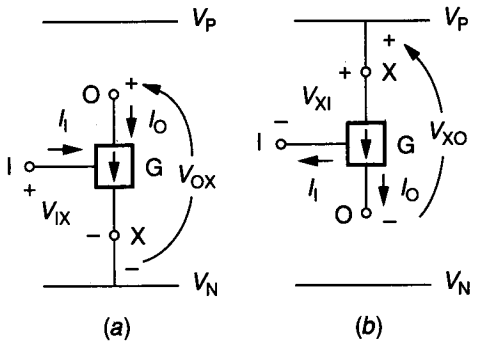


FIGURE 6.1-2
Schematic representations for (*a*) A voltage-controlled current sink and (*b*) A voltage-controlled current source.

and for Fig. 6.1-2*b* as

$$I_O = g_{source}(V_{XI}, V_{XO}) \tag{6.1-2}$$

The nonlinear functions in Eqs. 6.1-1 and 6.1-2 depend on the technology used to implement the controlled source/sink.

The voltage-controlled sources/sinks are combined with the two-terminal loads to implement the three basic types of inverter architectures shown in Fig. 6.1-3. Figure 6.1-3*a* illustrates an inverter using a voltage-controlled current sink and a load connected between O and V_P. This inverter is called a *sinking inverter* because it sinks the current through the load. Figure 6.1-3*b* uses a voltage-controlled current source and a load connected between O and V_N. This type

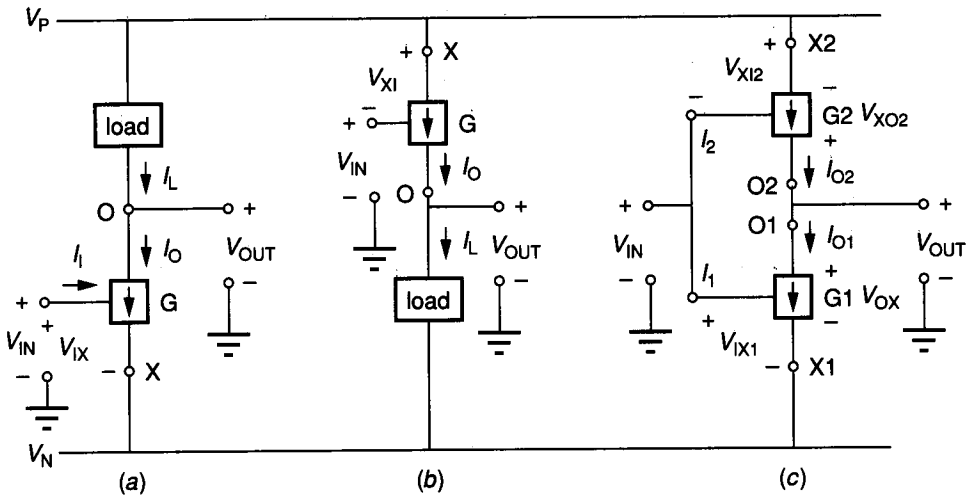


FIGURE 6.1-3
Generic representations of inverter architectures: (*a*) Sinking inverter, (*b*) Sourcing inverter, (*c*) Push-pull inverter.

of inverter is called a *sourcing inverter* because it sources the current in the load. The third architecture is shown in Fig. 6.1-3*c*. It uses a voltage-controlled current sink and a voltage-controlled current source. There is no external load in this architecture. This type of inverter is called a *push-pull inverter*. The loads in Fig. 6.1-3 can be any of the two-terminal active resistor realizations of Sec. 5.2 (Fig. 5.2-2, 5.2-3, or 5.2-6) or the dc current sources or sinks of Sec. 5.3. The use of dc current sources or sinks to realize the load will lead to high values of small signal voltage gain, A_v.

The large signal transfer behavior of the inverter can be intuitively developed. Consider the sinking inverter of Fig. 6.1-3*a*. Assume that V_{IN} is taken to V_N. With V_{IX} equal to zero, I_O will also be zero. We will call this the *off* state of the controlled sink. Because we are assuming that no external current flows, then I_L is also zero. When no current flows through the load, the voltage across it will be zero or close to zero. Therefore, V_{OUT} is approximately V_P. This corresponds to the upper left-hand corner of the plot of Fig. 6.1-4*a*. To simplify the analysis, we shall assume that the controlled sink turns on when $V_{IX} = V_{TH}$ ($V_{IN} = V_{TH} + V_N$). At this point the current I_O will start to flow. Because $I_O = I_L$, the voltage across the load starts to increase, causing V_{OUT} to decrease. As V_{IN} continues to increase, the voltage drop across the load approaches $V_P - V_N$, which implies that V_{OUT} approaches V_N. Under this condition, the controlled sink reaches a state where the current can no longer increase and the voltage V_{OX} is approximately zero. We will call this the *on* state of the controlled sink. The region between the off and on states will be called the *transition region*. The transfer curve in Fig. 6.1-4*a* is arbitrary because we have not used the actual relationships expressed by Eq. 6.1-1 for the controlled sink. It should be noted that the curve does not necessarily go through the origin, as implied in Fig. 6.1-4*a*.

Identical considerations hold for the sourcing inverter of Fig. 6.1-3*b*. In this case, when V_{IN} is at V_N, the controlled source is in the on state, where V_{XO} is approximately zero and the current through the load is limited. Therefore, V_{OUT} is approximately equal to V_P. At some point as V_{IN} is increased, the voltage V_{XO} will start to increase, causing V_{OUT} to decrease. When V_{XI} is equal to V_{TH} ($V_{IN} = V_P - V_{TH}$), I_O is zero and the voltage across the load is zero, causing V_{OUT} to be approximately V_N. The region between the on and off states of the controlled source is, again, the transition region. As with Fig. 6.1-4*a*, the transfer curve in the transition region is arbitrary because the exact relationship of Eq. 6.1-2 is not known. Again, the curve does not necessarily go through the origin as implied by Fig. 6.1-4b.

The general transfer curve for the push-pull inverter of Fig. 6.1-3*c* can be determined in a similar manner. It will be helpful to assume that a load resistor of large value is connected from the output to ground. When V_{IN} is at V_N, G1 is off and G2 is on. Because I_{O1} is zero, I_{O2} flowing through the load resistor will cause V_{OUT} to be at V_P. As V_{IN} increases from its value of V_N, V_{IX1} will equal V_{TH1} ($V_{IN} = V_N + V_{TH1}$) and the current I_{O1} begins to flow, causing the current in the load resistor to decrease and resulting in a decrease in V_{OUT}. At some point in the further increase of V_{IN}, $I_{O2} = I_{O1}$ and V_{OUT} is

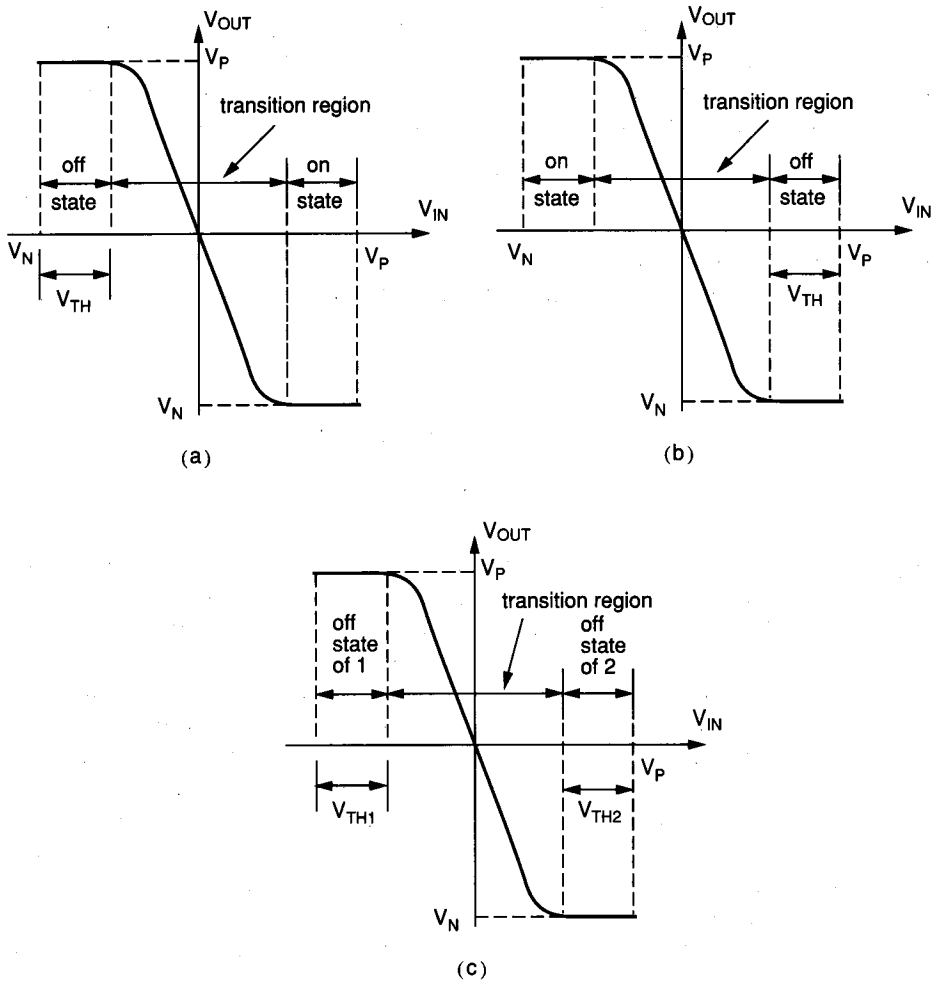


FIGURE 6.1-4
Typical voltage transfer functions for the inverters of Fig. 6.1-3: (*a*) Sinking inverter, (*b*) Sourcing inverter, (*c*) Push-pull inverter.

zero. Further increasing V_{IN} causes $I_{O1} > I_{O2}$, and V_{OUT} becomes negative and approaches V_N. When $V_{XI2} = V_{TH2}(V_{IN} = V_P - V_{TH2})$, G2 turns off and V_{OUT} is at V_N. The external load resistance used for this analysis turns out to be the output resistances associated with the controlled current sinks/sources. V_{OUT} is not necessarily zero at $V_{IN} = 0$ as implied by Fig. 6.1-4c.

The small signal voltage gain of the inverter can be related to the voltage transfer characteristics of Fig. 6.1-4 by the following definition.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\partial V_{OUT}}{\partial V_{IN}}\bigg|_{Q\text{-point}} \tag{6.1-3}$$

where the Q-point refers to a given value of the input or output voltage. Therefore, we see that the slope of the voltage transfer function of the inverter determines its gain. Obviously, the desired Q-point for a high-gain inverting amplifier is in the transition regions of Fig. 6.1-4, where the slope is the steepest. This will simplify our considerations because we can ignore the regions of operation outside of the transition region. This represents a major distinction between digital and analog circuits. In digital applications, the inverter will be operated from one extreme to the other. The two quiescent operating states of digital circuits will be in the flat portions of the voltage transfer curves of Fig. 6.1-4.

When the inverting amplifier is biased at a Q-point in the transition region, the next step is to linearize the circuit. This is done by expanding Eqs. 6.1-1 and 6.1-2 about a Q-point. While the formal mathematical characterization uses a multivariable series expansion, we shall approximate the result with only the first-order terms. Consider the approximation of Eq. 6.1-1, given as

$$I_O = g_{sink}(V_{IX}, V_{OX}) \approx I_o + \left.\frac{\partial I_O}{\partial V_{IX}}\right|_Q \Delta V_{IX} + \left.\frac{\partial I_O}{\partial V_{OX}}\right|_Q \Delta V_{OX} \quad (6.1\text{-}4)$$

where Q indicates operation at the dc bias point. Noting that the ac output current, i_o, is defined as $I_O - I_o$ allows us to express Eq. 6.1-4 as

$$i_o = I_O - I_o = \left.\frac{\partial I_O}{\partial V_{IX}}\right|_Q \Delta V_{IX} + \left.\frac{\partial I_O}{\partial V_{OX}}\right|_Q \Delta V_{OX} \approx g_m v_{ix} + g_o v_{ox} \quad (6.1\text{-}5)$$

where the signal swings are small enough so that the ac voltages v_{ix} and v_{ox} can be closely approximated by ΔV_{IX} and ΔV_{OX}, respectively. The notations g_m and g followed by other subscripts are used to relate the current dependence on a voltage at different terminals and voltage at the same terminals, respectively. g_m is called *transconductance* and g is called *conductance*. In a similar manner, the ac current of the voltage-controlled current source of Eq. 6.1-2 can be expressed as

$$i_o \approx g_m v_{xi} + g_o v_{xo} \quad (6.1\text{-}6)$$

In some of the practical voltage-controlled current sinks/sources, there may be an input current caused by the controlling voltage. This leads to two more expressions necessary to characterize the voltage-controlled current sink/source in addition to Eqs. 6.1-1 and 6.1-2. These general expressions are

$$I_I = g'_{sink}(V_{IX}) \quad (6.1\text{-}7)$$

and

$$I_I = g'_{source}(V_{XI}) \quad (6.1\text{-}8)$$

Repeating the considerations of Eqs. 6.1-1 and 6.1-2 for Eqs. 6.1-7 and 6.1-8 results in the following relationship for the voltage-controlled current sink:

$$i_i \approx g_i v_{ix} \quad (6.1\text{-}9)$$

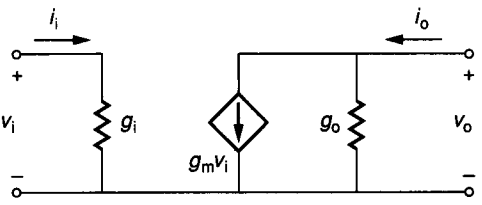


FIGURE 6.1-5
Small signal model for a voltage-controlled current sink/source.

and for the voltage-controlled current source:

$$i_i \approx g_i v_{xi} \tag{6.1-10}$$

g_i is called the input conductance and denotes the change of the input current due to a change in the input voltage.

Both Eqs. 6.1-5 and 6.1-9 or 6.1-6 and 6.1-10 can be modeled schematically as illustrated in Fig. 6.1-5. The small signal model for the voltage-controlled current sink and voltage-controlled current source are identical because small ac changes are insensitive to dc polarities. An ac model for the inverters of Fig. 6.1-3*a* and *b* can thus be obtained by adding the resistance (r_l) or a conductance (g_l) in parallel with the output of the circuit of Fig. 6.1-5, resulting in the complete model shown in Fig. 6.1-6. The value r_l was typically designated as r_o for the loads discussed in Chapter 5. Alternately, r_l could be derived by a development similar to that used in obtaining Eqs. 6.1-7 through 6.1-10.

The small signal ac performance of the sinking and sourcing inverters can be easily analyzed from the circuit of Fig. 6.1-6. It can be seen that the ac gain, the input resistance, and the output resistance are as follows.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m}{g_o + g_l} = -g_m r_{out} \tag{6.1-11}$$

$$r_{in} = r_i = \frac{1}{g_i} \tag{6.1-12}$$

and

$$r_{out} = \frac{r_o r_l}{r_o + r_l} = \frac{1}{g_o + g_l} \tag{6.1-13}$$

The small signal model for the push-pull inverter is obtained by connecting two of the models in Fig. 6.1-5 in parallel, resulting in the model of Fig. 6.1-7.

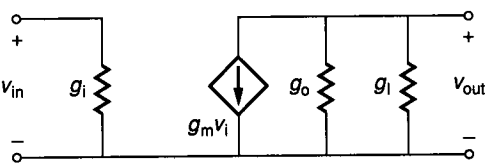


FIGURE 6.1-6
Small signal model for the inverters of Fig. 6.1-3*a* and *b*.

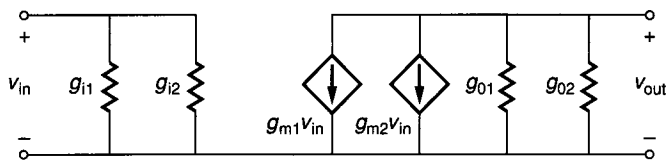


FIGURE 6.1-7
Small signal model for the push-pull inverter of Fig. 6.1-3*c*.

In this case, the ac gain, the input resistance, and the output resistance are given as follows.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{o1} + g_{o2}} = -(g_{m1} + g_{m2})r_{out} \tag{6.1-14}$$

$$r_{in} = \frac{r_{i1}r_{i2}}{r_{i1} + r_{i2}} = \frac{1}{g_{i1} + g_{i2}} \tag{6.1-15}$$

and

$$r_{out} = \frac{r_{o1}r_{o2}}{r_{o1} + r_{o2}} = \frac{1}{g_{o1} + g_{o2}} \tag{6.1-16}$$

Except for the sum of the transconductances in the numerator of A_v and the paralleling of the input resistances, the ac model for the push-pull inverter is similar to the ac model for the sinking and sourcing inverters.

In order to consider the frequency response, it is necessary to introduce parasitic capacitances into the ac models of Figs. 6.1-6 and 6.1-7. As was discussed in Chapter 3, parasitic capacitances are always present in any device and are due to actual capacitance or to the finite time required for carriers to move from one point to another. Figure 6.1-8 shows a model that is suitable for the ac frequency analysis of all three inverter architectures. r_1 is equal to r_{in}, r_2 is equal to r_{out}, and g_m is equal to g_{m1} or g_{m2} for the sinking or sourcing inverters and to $g_{m1} + g_{m2}$ for the push-pull inverter. C_1 and C_2 represent all parasitic capacitors associated with the input and output nodes, respectively. C_3 represents all capacitors connected between the input and output. Depending upon

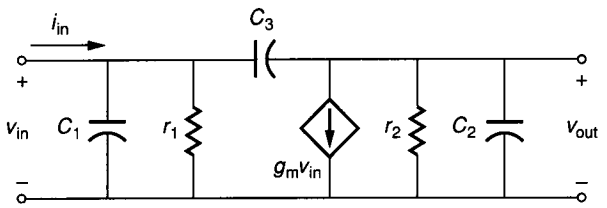


FIGURE 6.1-8
Small signal model including capacitances for the three inverter architectures of Fig. 6.1-3.

the technology used to implement the inverters, these capacitors could have values ranging from 5 fF to 5 pF.

We will consider the frequency response of Fig. 6.1-8 for two cases. The first is when the input source is a voltage, v_{in}, and the second is when the input source is a current, i_{in}. If the input source is a voltage, then the currents can be summed at the output node to give

$$V_{out}(s)(g_2 + sC_2) + sC_3[V_{out}(s) - V_{in}(s)] + g_m V_{in}(s) = 0 \tag{6.1-17}$$

In Eq. 6.1-17, s is the complex frequency variable. Solving for the complex frequency transfer function $V_{out}(s)/V_{in}(s)$ gives

$$A_v(s) = \frac{-g_m[1 - s(C_3/g_m)]}{g_2\{1 + s[(C_2 + C_3)/g_2]\}} = A_{v0}\frac{(1 - s/z_1)}{(1 + s/p_1)} \tag{6.1-18}$$

where the midband gain, A_{v0}, the zero, z_1, and the pole, p_1, are given as

$$A_{v0} = \frac{-g_m}{g_2} \tag{6.1-19}$$

$$z_1 = \frac{g_m}{C_3} \tag{6.1-20}$$

and

$$p_1 = \frac{-g_2}{C_2 + C_3} \tag{6.1-21}$$

It is seen that the voltage-driven inverter has a first-order transfer function with a midband voltage gain corresponding to the ac voltage gains of Eq. 6.1-11 or 6.1-14, a zero in the right-half complex frequency plane, and a pole in the left-half complex frequency plane. Generally, the value of g_m is much greater than g_2 so that the zero has little influence upon the frequency response. In this case, the ω_{-3dB} frequency would be given as

$$\omega_{-3dB} = \frac{g_2}{C_2 + C_3} \tag{6.1-22}$$

In some technologies, the value of g_m may not be sufficiently greater than g_2 so that the zero must be considered. The influence of the right-half plane zero has two important effects. The most obvious effect is to boost the magnitude of the frequency response. The less obvious effect is to cause a phase *lag* similar to a pole. If negative feedback is placed around such an inverter, it will have very poor stability characteristics. A typical frequency response for a voltage-driven inverter is shown in Fig. 6.1-9.

If the inverter of Fig. 6.1-8 is current-driven, then an equation in addition to Eq. 6.1-17 is required. This equation is found by summing currents at the input node and is given as

$$I_{in} = -(g_1 + sC_1)V_{in}(s) + sC_3[V_{in}(s) - V_{out}(s)] \tag{6.1-23}$$

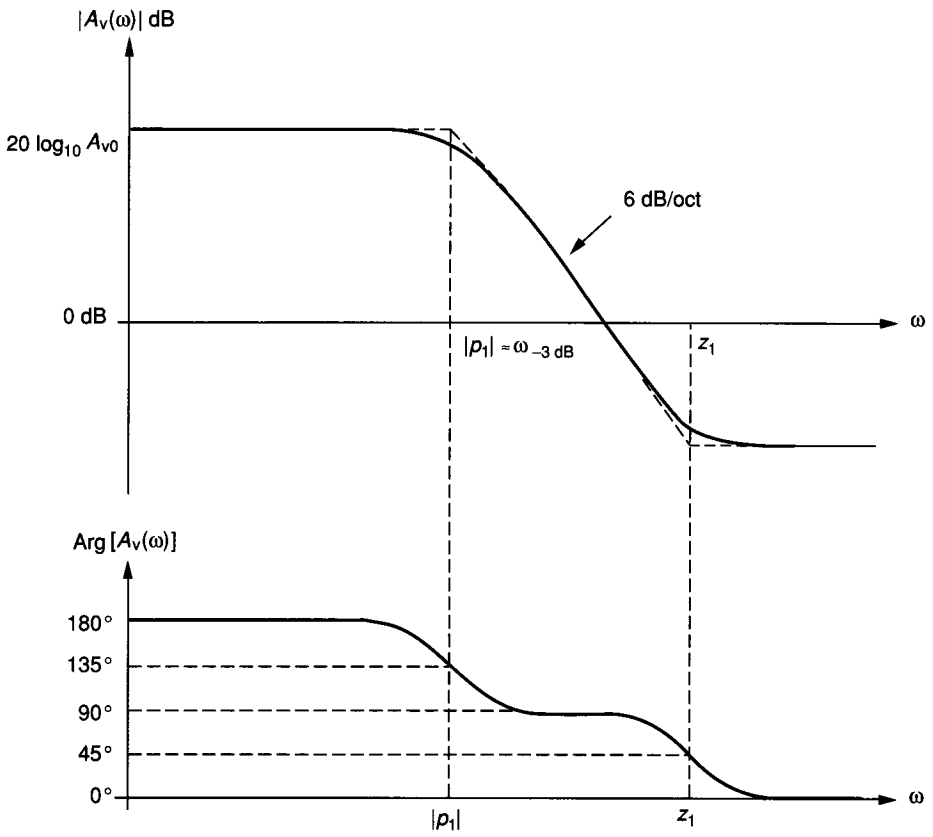


FIGURE 6.1-9
Typical frequency response for a voltage-driven inverter.

Simultaneously solving Eqs. 6.1-17 and 6.1-23 for the transfer function $V_{out}(s)/I_{in}(s)$ results in the following.

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{-g_m[1 - s(C_3/g_m)]}{g_1g_2 + s[g_1(C_2 + C_3) + g_2(C_1 + C_3) + g_mC_3] + s^2(C_1C_2 + C_1C_3 + C_2C_3)} \tag{6.1-24}$$

Equation 6.1-24 can be rewritten as

$$\frac{V_{out}(s)}{I_{in}(s)} = \left(\frac{-g_m}{g_1g_2}\right)[1 - s(C_3/g_m)] \Big/ \{1 + s[(C_2 + C_3)/g_2 + (C_1 + C_3)/g_1 + (g_mC_3)/(g_1g_2)] + s^2(C_1C_2 + C_1C_3 + C_2C_3)/(g_1g_2)\} \tag{6.1-25}$$

The frequency response of the current-driven inverter is seen to have two poles, p_1 and p_2. In most inverters, the magnitude of one of the poles is much

less than the magnitude of the other; in other words, $|p_2| \ll |p_1|$. In this case, we are able to find the pole locations in terms of the model parameters by the following method. Assume that the denominator of Eq. 6.1-25, $D(s)$, can be written as

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{6.1-26}$$

where $|p_1| >> |p_2|$. Equating the denominator of Eq. 6.1-25 to Eq. 6.1-26 results in the approximate pole locations expressed as

$$p_1 = -\left(\frac{C_2 + C_3}{g_1} + \frac{C_1 + C_3}{g_2} + \frac{g_m C_3}{g_1 g_2}\right)^{-1} \approx -\frac{g_1 g_2}{g_m C_3} \tag{6.1-27}$$

and

$$p_2 = \frac{-g_m C_3}{C_1 C_2 + C_1 C_3 + C_2 C_3} \tag{6.1-28}$$

Assuming that C_1, C_2, and C_3 are all about the same value and that g_m is much greater than g_1 or g_2 leads to the conclusion that ω_{-3dB} is approximately given by

$$\omega_{-3dB} \approx \frac{g_1 g_2}{g_m C_3} \tag{6.1-29}$$

Comparing Eqs. 6.1-22 and 6.1-29 shows that the bandwidth of the current driven inverter is approximately A_{v0} $(= g_m/g_2)$ less than that of the voltage-driven inverter. The reason for the decrease in bandwidth is the influence of the gain of the amplifier on the capacitor C_3. Because this capacitor is connected between the input and output, it has the voltage gain of the inverter across it. When viewed from the input, this makes the C_3 capacitor look $1 + A_{v0}$ larger than it really is. This effect is called the *Miller effect*. When the input is current-driven, the large Miller capacitance can create a dominant pole at the input as just shown. Figure 6.1-10 shows the typical frequency response for a current-driven inverter.

The last small signal characteristic we will examine is noise. Unfortunately, the noise models are sufficiently technology-dependent that it is more suitable to introduce the noise analysis after the technology has been selected.

In this subsection the inverter has been introduced from a generic viewpoint. The various types of inverter architectures were discussed and analyzed from both a large signal and a small signal viewpoint. In the following subsections, we will apply these ideas to inverters using MOS and BJT technologies.

6.1.2 MOS INVERTING AMPLIFIERS

The general concepts of inverting amplifiers will now be applied to MOS technology. The possible MOS implementations of the sinking inverter architecture of Fig. 6.1-3*a* are shown in Fig. 6.1-11. Each of the lower blocks is a realization of the voltage-controlled current sink using an n-channel transistor. Each of the upper blocks represents a realization of the load connected between

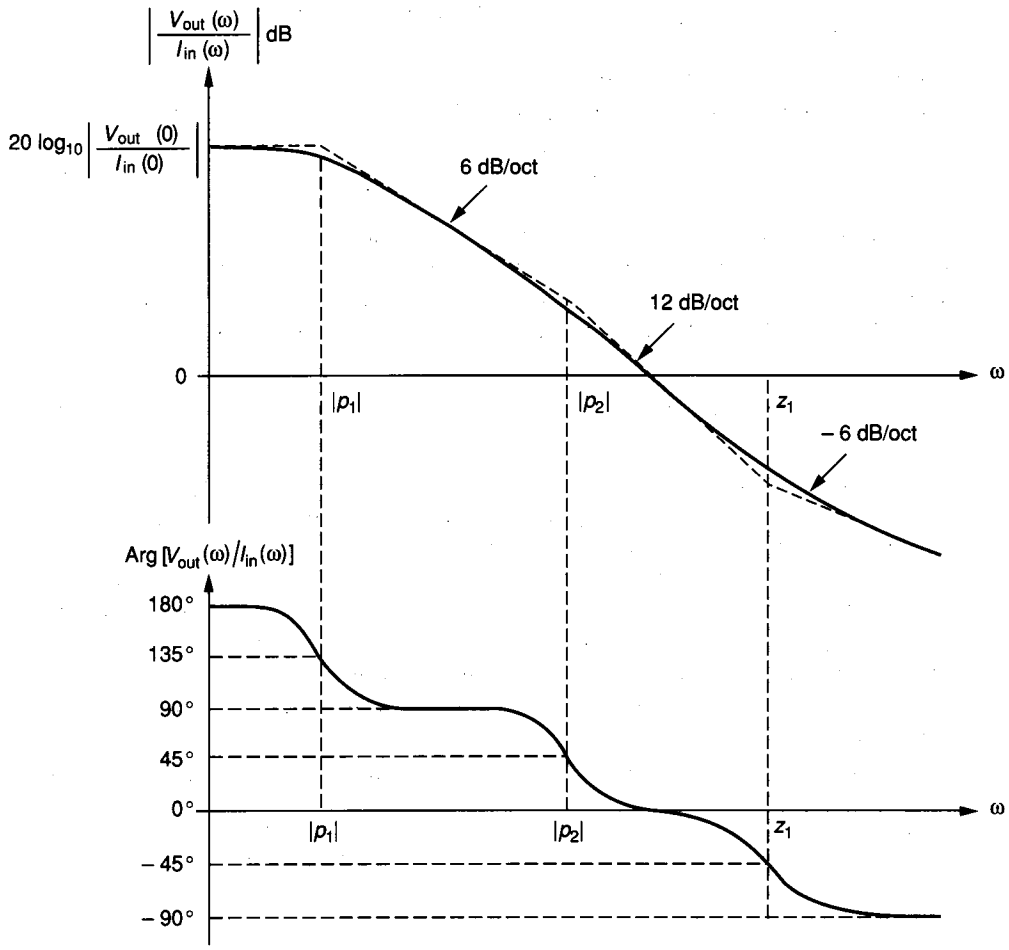


FIGURE 6.1-10
Typical frequency response for a current-driven inverter.

the output of the voltage-controlled current sink and V_{DD}. A CMOS technology having a depletion transistor capability is able to implement all of the inverters of Fig. 6.1-11. If the CMOS technology does not have a depletion transistor capability, then only the inverters of Fig. 6.1-11*a*, *b*, and *c* can be realized. An NMOS technology with a depletion transistor capability can realize the inverters of Fig. 6.1-11*c* or *d*. An NMOS technology that does not have a depletion transistor capability can realize only the inverter of Fig. 6.1-11*c*.

The voltage transfer function of the MOS inverters of Fig. 6.1-11 can be found using the approach demonstrated in Fig. 6.1-4. When V_{IN} of Fig. 6.1-11*a* is at V_{SS}, the drain current in M1 is zero. Because M2 has its drain and gate connected, it is always in the saturation region. Therefore, Eq. 9 of Table 3.1-1 shows that for zero current, the value of $V_{GS2}(V_{DS2})$ is equal to V_{T2}. Therefore, the value of V_{OUT} is $V_{DD} - V_{T2}$ until V_{IN} increases from V_{SS} to V_{T1}, where M1 turns on. At this point the output voltage starts to drop as in Fig. 6.1-4*a*.

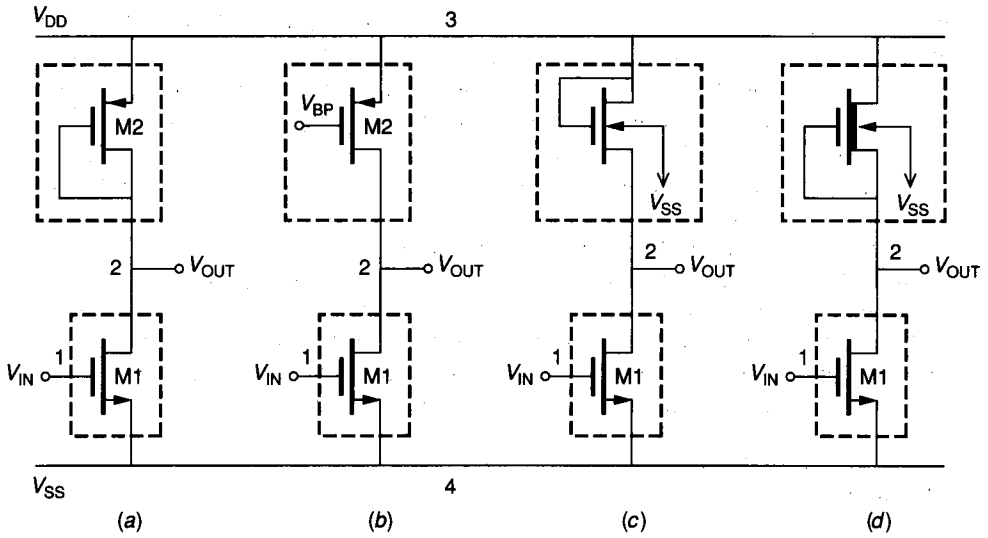


FIGURE 6.1-11
Possible realizations of the sinking inverter for Fig. 6.1-3*a*: (*a*) Active p-channel load, (*b*) Current source load, (*c*) Active n-channel load, (*d*) Depletion n-channel load. All potentials are with respect to ground.

Unlike the ciruit of Fig. 6.1-4*a*, however, the output voltage of Fig. 6.1-11*a* never reaches V_{SS}.

As the current in M1 and M2 increases because V_{IN} is approaching V_{DD}, the voltage across M1 only increases by the square root of the current. Figure 6.1-12 shows the resulting voltage transfer curve for the inverter of Fig. 6.1-11*a* when $W_1 = 15\ \mu, L_1 = 10\ \mu, W_2 = 5\ \mu, L_2 = 10\ \mu, V_{DD} = -V_{SS} = 5$ V, for a CMOS technology corresponding to the parameters in Table 3.1-2. The SPICE input file necessary to generate this plot is included in the figure.

It is of interest to identify in Fig. 6.1-12 the regions where M1 is off, ohmic, and saturated. M1 is off when $V_{IN} < V_{SS} + V_{T1} = -4.25$ V. M1 is saturated when

$$V_{DS1} > V_{GS1} - V_{T1} \Rightarrow V_{OUT} - V_{SS} > V_{IN} - V_{SS} - V_{T1} \Rightarrow V_{OUT} > V_{IN} - V_{T1} \tag{6.1-30}$$

The various regions of M1 are shown in Fig. 6.1-12. This information is important because now we know that the transition region corresponds (for the most part) to M1 operating in the saturation region. The large signal equation that governs the operation of both devices in the transition region is from Eq. 3.1-4

$$I_D \approx \frac{K'W}{2L}(V_{GS} - V_T)^2 \tag{6.1-31}$$

where we have neglected the channel modulation effect (λ). Equating I_{D1} to I_{D2} results in the following relationship.

$$\frac{K_1'W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2 = \frac{K_2'W_2}{2L_2}(V_{DD} - V_{OUT} - V_{T2})^2 \tag{6.1-32}$$

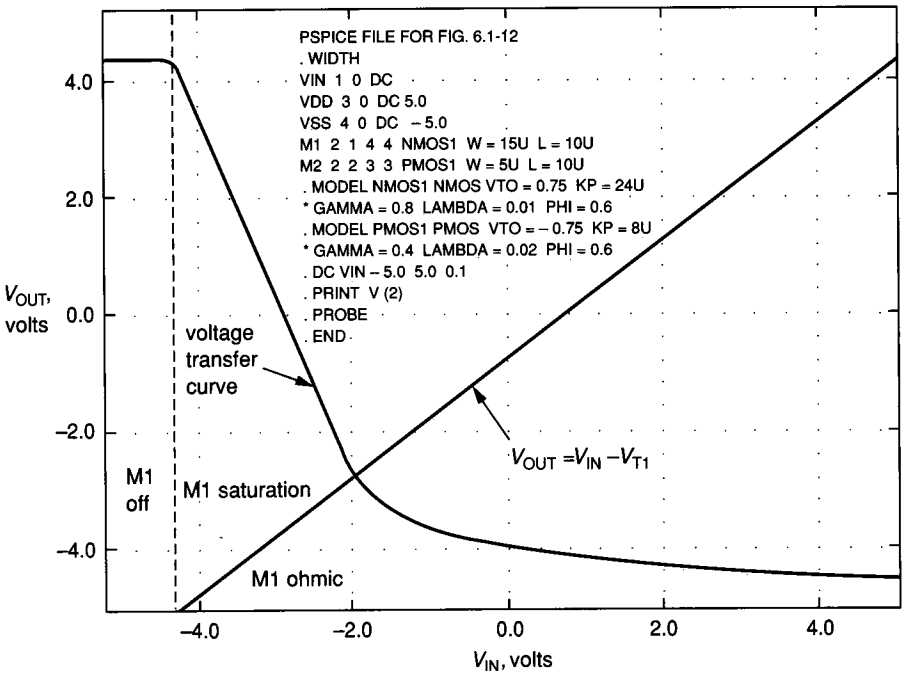


FIGURE 6.1-12
VTC of sinking inverter with active load.

If the inverter of Fig. 6.1-11*a* is biased in the transition region, then Eq. 6.1-3 can be used to find the small signal ac voltage gain. Applying Eq. 6.1-3 to Eq. 6.1-32 results in

$$A_v = \frac{v_{out}}{v_{in}} = \left.\frac{\partial V_{OUT}}{\partial V_{IN}}\right|_Q = -\left(\frac{K_1' W_1 L_2}{K_2' L_1 W_2}\right)^{0.5} \tag{6.1-33}$$

We can also use the small signal model of Fig. 6.1-6 to calculate A_v. From Chapter 3, we know that $g_i = 0$, $g_m = g_{m1}$, $g_o = g_{ds1}$, and $g_1 = g_{m2} + g_{ds2} \approx g_{m2}$. Eq. 6.1-11 and Eq. 3.1-11 give the small signal voltage gain as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{m2} + g_{ds2}} \approx -\frac{g_{m1}}{g_{m2}} = -\left[\frac{K_1'(W_1/L_1)}{K_2'(W_2/L_2)}\right]^{0.5} \tag{6.1-34}$$

The two approaches to finding A_v are seen to agree as expected. Using the small signal model, we can find the input and output resistances as

$$r_{in} = \infty \tag{6.1-35}$$

and

$$r_{out} = \frac{1}{g_{ds2} + g_{m2}} \approx \frac{1}{g_{m2}} \tag{6.1-36}$$

The frequency response of the inverter of Fig. 6.1-11*a* can be found by inserting the transistor capacitors used in Ex. 3.1-5 into the circuit of Fig. 6.1-11*a*

and comparing the result with Fig. 6.1-8. C_1, C_2, and C_3 of the circuit of Fig. 6.1-8 become

$$C_1 = C_{GS1} + C_{GB1} \tag{6.1-37}$$

$$C_2 = C_{BD1} + C_{GS2} + C_{BD2} + C_{GB2} \tag{6.1-38}$$

and

$$C_3 = C_{GD1} \tag{6.1-39}$$

Therefore, the upper -3 dB frequency for the voltage-driven inverter of Fig. 6.1-11*a* is found from Eq. 6.1-22 as

$$\omega_{-3dB} = \frac{g_{m2} + g_{ds1} + g_{ds1}}{C_{BD1} + C_{GS2} + C_{BD2} + C_{GD1} + C_{GB2}} \tag{6.1-40}$$

The noise of an inverter is also one of the small signal performance characteristics of interest when inverters are used as small signal amplifiers. Noise is a phenomenon caused by small fluctuations of the analog signal within the components themselves. Noise results from the fact that electrical current is not continuous but the result of quantized behavior and is associated with fundamental processes in a semiconductor component. Common types of noise for semiconductor devices are thermal and $1/f$ noise.

Regardless of the type of noise, the model always can be characterized by an independent voltage or current source. In general, noise is expressed in terms of its mean-square value $[V(\text{rms})^2]$. Noise spectral density is the noise mean-square value per Hertz of bandwidth $[V(\text{rms})^2/\text{Hz}]$. The model for noise in an MOS device can be modeled as an independent voltage in series with the gate as shown in Fig. 3.1-30*b*. Figure 6.1-13 shows the noise models added to the active-load sinking inverter of Fig. 6.1-11*a*. $\overline{V}_{n1}^2$ and $\overline{V}_{n2}^2$ are the mean-square

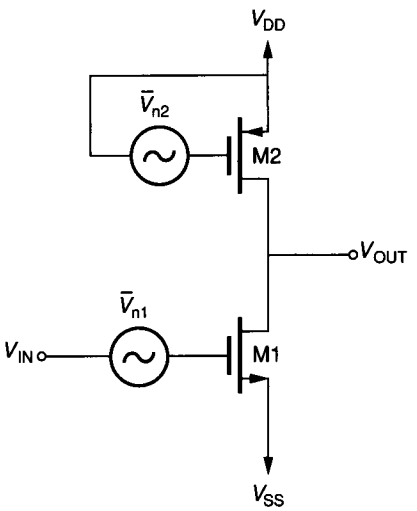


FIGURE 6.1-13
Noise model of Fig. 6.1-11*a*.

noise voltages of M1 and M2 modeled at the input (gate) of each device. Since $\overline{V}_{n1}$ and $\overline{V}_{n2}$ are uncorrelated, the output mean-square noise voltage can be calculated using superposition. The part of the output due to $\overline{V}_{n1}^2$ is

$$\overline{V}_{o1}^2 = \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{V}_{n1}^2 \tag{6.1-41}$$

The part of the output due to $\overline{V}_{n2}^2$ is

$$\overline{V}_{o2}^2 = \overline{V}_{n2}^2 \tag{6.1-42}$$

It should be noted that all gains between the input and output are positive and squared. Also, the value of output due to $\overline{V}_{n2}^2$ is equal to $\overline{V}_{n2}^2$ because the gate voltage of M2 is constant ($\overline{V}_{n2}^2$ only changes the drain voltage). Summing Eqs. 6.1-41 and 6.1-42 gives the total output mean-square noise voltage.

It is customary to reflect the output mean-square noise voltage to the input of the amplifier. This input referred noise voltage obtained by dividing the output noise voltage by the voltage gain is called the equivalent, input-referred, mean-square noise voltage of the amplifier and is given as

$$\overline{V}_{eq}^2 = \overline{V}_{n1}^2 + \left(\frac{g_{m2}}{g_{m1}}\right)^2 \overline{V}_{n2}^2 \tag{6.1-43}$$

$\overline{V}_{eq}$ is a frequency independent noise because we used the midband or frequency independent voltage gain. Equation 6.1-43 represents the equivalent input mean-square noise voltage of Fig. 6.1-11*a*. When the designer knows the form of the noise mean-square voltages, then Eq. 6.1-43 can be used to minimize the noise. For example, the $1/f$ noise of a MOSFET was given in Eq. 3.1-35 and can be expressed in terms of noise-voltage spectral density in a 1 Hz band as

$$S_{VN} = \frac{S_{IN}}{g_m^2} = \frac{B}{fWL}(V^2/\text{Hz}) \tag{6.1-44}$$

where B is a constant that is dependent on the technology. We note from Eq. 6.1-44 that the larger-area devices will have less $1/f$. It has also been empirically observed that B is less for p-channel than for n-channel devices, when everything else is equal. Substituting Eq. 6.1-44 into Eq. 6.1-43 gives

$$S_{eq(1/f)} = \left(\frac{B_N}{fW_1L_1}\right)\left[1 + \left(\frac{K_P'B_P}{K_N'B_N}\right)\left(\frac{L_1}{L_2}\right)^2\right](V^2/\text{Hz}) \tag{6.1-45}$$

If the length of M1 is much smaller than that of M2, the input $1/f$ noise will be dominated by that of M1. To minimize the $1/f$ contribution due to M1, its width must be increased as much as possible. Other types of noise substituted into Eq. 6.1-43 will provide other guidelines to reduce the noise of an amplifier. In general, the designer should try to make the gain of the first stage of an amplifier as large as possible to reduce the overall noise.

An example follows to illustrate the small signal performance of the active-load sinking inverter of Fig. 6.1-11*a*.

Example 6.1-1. AC performance of inverter of Fig. 6.1-11*a*. Determine the small signal performance of the inverter of Fig. 6.1-11*a* using the model parameters of Table 3.1-2, assuming that $W_1/L_1 = 15\ \mu/10\ \mu$ and $W_2/L_2 = 5\ \mu/10\ \mu$ and $V_{DD} = -V_{SS} = 5$ V. The drain and source area (periphery) of M1 and M2 are $150\mu^2(50\mu)$ and $50\mu^2(30\mu)$, respectively. Assume that V_{out} is biased at 0 V. Also assume that the noise is white noise given in Eq. 3.1-34 and find the equivalent input-noise-voltage spectral density.

Solution. We begin the solution by finding the dc current in M1 and M2, calculating the value of V_{G1}, and determining the region of operation for M1. In these calculations we will ignore the influence of the channel modulation (λ). The dc quiescent current can be found from the voltage drop across M2 and is

$$I = \frac{K_P' W_2}{2L_2}(V_{DD} - V_{out} - V_{T2})^2 = \frac{8(5)}{2(10)}(5 - 0.75)^2\ \mu A = 36\ \mu A$$

Assume that M1 is saturated. The value of V_{gs1} that gives 36 μA is found as

$$V_{gs1} = V_{T1} + \left(\frac{2I L_1}{K_N' W_1}\right)^{0.5} = 0.75 + \left[\frac{(2)(36)(10)}{(24)(15)}\right]^{0.5} = 0.75 + 1.41 = 2.17\ V$$

Thus, M1 is in fact saturated and $V_{out} = 0$ V corresponds to $V_{in} = -2.83$ V, as seen in Fig. 6.1-12.

Next, we calculate the small signal parameters for M1 and M2. Using the formulas of Table 3.1-3 gives $g_{m1} = 50.91\mu S$, $g_{ds1} = 0.36\mu S$, $g_{m2} = 16.97\mu S$, and $g_{ds2} = 0.72\mu S$.

Equation 6.1-11 gives

$$A_v = \frac{-50.91}{16.97 + 0.36 + 0.72} = -2.82$$

Equation 6.1-13 gives

$$r_{out} = \frac{1}{(16.97 + 0.36 + 0.72)\mu S} = 55.4\ k\Omega$$

The capacitors of Eq. 6.1-40 are found using the formulas of Fig. 3.1-19*b* and the capacitances of Table 2B.4. In this example, we shall include the sidewall capacitances and will assume that the Value of n in Eq. 3. 1-14 is 0.5 for both the bottom and sidewall junction capacitances. The capacitors of Eq. 6.1-40 are

$$C_{BD1} = (0.33)(150)[1 + (5/.6)]^{-0.5} + (0.9)(50)[1 + (5/.6)]^{-0.5} =$$
$$16.20fF + 14.73fF = 30.93fF$$

$$C_{GS2} = (0.7)(5)(0.6) + (0.67)(50)(0.7) = 2.1fF + 23.33fF = 25.43fF$$

$$C_{BD2} = (0.38)(50)[1 + (5/.6)]^{-0.5} + (1)(30)[1 + (5/.6)]^{-0.5} =$$
$$6.22fF + 9.82fF = 16.04fF$$

$$C_{GD1} = (0.7)(15)(0.45) = 4.73fF$$

$$C_{GB2} = 0$$

Substituting the above values in Eq. 6.1-40 results in

$$\omega_{-3dB} = \frac{18.05\mu S}{30.93fF + 25.43fF + 16.04fF + 4.73fF} = 234Mrps = 37.2MHz$$

Dividing the spectral noise density of Eq. 3.1-34 by g_m^2 gives for M1

$$S_{VWN} = 2.17 \times 10^{-16} V^2/\text{Hz}$$

and for M2

$$S_{VWP} = 6.51 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density can be found from Eq. 6.1-43 by replacing each mean-square noise voltage by its noise voltage spectral density and is

$$S_{eq} = S_{VWN} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VWP} = 2.2 \times 10^{-16} + \left(\frac{16.97}{50.91}\right)^2 6.5 \times 10^{-16}$$

$$= 2.89 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density is equal to 17.0 $\text{nV}/\sqrt{\text{Hz}}$.

The performance of the inverter of this example is seen to have a low gain, a moderate output resistance (for MOS devices), a large bandwidth, and an input-referred noise that depends on the noise of the MOS devices. The performance of the active-load sinking inverter can be altered by changing the bias current or the W and L values of M1 and M2.

The voltage inverter of Fig. 6.1-11*c* will have characteristics similar to Fig. 6.1-11*a* with one exception. Because M2 is n-channel, it will experience bulk effects causing V_{T2} to increase as V_{OUT} increases. Consequently, the output high value of Fig. 6.1-11*c* will be less than that of Fig. 6.1-11*a*. In addition, the back-gate (bulk) transconductance (g_{mb2}) will cause the resistance of the load to be slightly less, resulting in less ac gain. If Fig. 6.1-11*c* is used in Example 6.1-1 with the same W/L values and current for M1 and M2, the ac gain is -1.56, the ac output resistance is 30.7 kΩ, the bandwidth is 42.8 MHz, and the equivalent input noise voltage spectral density is 17.3 $\text{nV}/\sqrt{\text{Hz}}$.

The ac voltage gains of the inverters of Fig. 6.1-11*a* and *c* are low because the resistance of the load device is low. The inverter of Fig. 6.1-11*b* uses a current source as its load and achieves a much higher gain. Figure 6.1-14 shows the voltage transfer curve of the current-source-load sinking inverter of Fig. 6.1-11*b* when V_{BP} is 2 V. When V_{IN} is at V_{SS}, M1 is off and the voltage across M2 is zero, causing V_{OUT} to be at V_{DD}. At some point when V_{IN} increases, M1 will begin to turn on, causing a current to flow in the inverter. This current flow causes a drop across M2 causing the output voltage to fall. As V_{IN} is increased past this point, all of $V_{DD} - V_{SS}$ is dropped across M2, causing M1 to be in the ohmic region with little voltage across it. In this condition, V_{OUT} is approximately V_{SS}.

The regions of operation can be found as before using the transition relationship between the ohmic and saturation regions. M2 is saturated when

$$V_{SD} > V_{SG} + |V_{T2}| \Rightarrow V_{DD} - V_{OUT} > V_{DD} - V_{BP} - |V_{T2}| \Rightarrow$$

$$V_{OUT} < V_{BP} - |V_{T2}| \quad (6.1\text{-}46)$$

The state of M1 is identified by Eq. 6.1-30. The various regions of operation of M1 and M2 are identified in Fig. 6.1-14. Again, we see that the desired ac operating region occurs in the transition region, where both M1 and M2 are

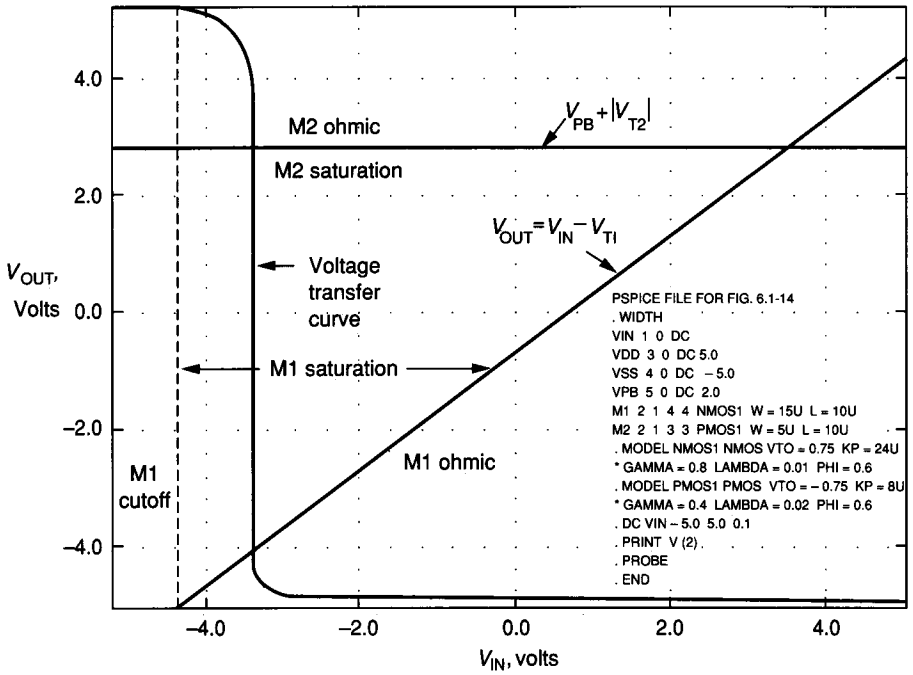


FIGURE 6.1-14
VTC of sinking inverter with current source load.

saturated. In the following discussion, we will assume that the inverter of Fig. 6.1-11*b* is biased with both M1 and M2 in the saturation region.

The operating point of the inverter of Fig. 6.1-11*b* can be found using the previous approach. This time, however, the channel modulation effects should be included in order to relate the drain-source voltage to the drain current. The relationship for M1 and M2 is given as

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{6.1-47}$$

Equating I_{D1} to I_{D2} results in the following relationship for the inverter of Fig. 6.1-11*b*.

$$\frac{K'_N W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2[1 + \lambda_N(V_{OUT} - V_{SS})] = \frac{K'_P W_2}{2L_2}(V_{DD} - V_{BP} - V_{T2})^2[1 + \lambda_P(V_{DD} - V_{OUT})] \tag{6.1-48}$$

Differentiating Eq. 6.1-48 with respect to V_{IN} results in the slope of the voltage transfer curve in the transition region. Applying Eq. 6.1-3 to Eq. 6.1-48 results in

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\partial V_{OUT}}{\partial V_{IN}}\bigg|_Q \approx -\frac{[2K'_N(W_1/L_1)I]^{0.5}}{\lambda_N I + \lambda_P I} = -\frac{[2K'_N(W_1/L_1)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \tag{6.1-49}$$

where the channel modulation effect of Eq. 6.1-47 has been ignored after differentiation and I is the dc current flowing through both M1 and M2.

We can also use the small signal model of Fig. 6.1-6 to calculate A_v. From Chapter 3, we know that $g_i = 0$, $g_m = g_{m1}$, $g_o = g_{ds1}$, and $g_l = g_{ds2}$. Equation 6.1-11 and Table 3.1-3 give the small signal voltage gain as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = -\frac{[2K'_N(W_1/L_1)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \tag{6.1-50}$$

As expected, the two approaches to finding A_v give identical results. Using the small signal model, we can find the input and output resistances as

$$r_{in} = \infty \tag{6.1-51}$$

and

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} \tag{6.1-52}$$

The current-source-load sinking inverter of Fig. 6.1-11*b* has a very unusual property. It is observed that in Eqs. 6.1-49 and 6.1-50 the dc current appears only in the denominator as the argument of the square root. This means that the ac gain is inversely proportional to the square root of the dc bias current. The reason for this can be seen from Table 3.1-3. The transconductance is proportional to the square root of the current, and the conductance is proportional to the current. This property of increasing ac gain as the dc current is reduced does not hold for the previous MOS inverters. When the dc current is reduced to subthreshold levels (~0.1 μA), the transconductance also becomes proportional to the dc current, and the ac gain is no longer dependent on the dc current.

The frequency response of the circuit of Fig. 6.1-11*b* can be found by inserting the transistor capacitors of Example 3.1-5 into the circuit of Fig. 6.1-11*b* and comparing the result with Fig. 6.1-8. C_1, C_2, and C_3 of Fig. 6.1-8 become

$$C_1 = C_{GS1} + C_{GB1} \tag{6.1-53}$$

$$C_2 = C_{BD1} + C_{GD2} + C_{BD2} \tag{6.1-54}$$

and

$$C_3 = C_{GD1} \tag{6.1-55}$$

Therefore, the upper -3 dB frequency for the voltage-driven inverter of Fig. 6.1-11*b* is found from Eq. 6.1-22 as

$$\omega_{-3dB} \approx \frac{g_{ds1} + g_{ds2}}{C_{BD1} + C_{GD2} + C_{BD2} + C_{GD1}} \tag{6.1-56}$$

The noise performance of the current-source-load sinking inverter of Fig. 6.1-11*b* can be investigated in a similar manner as before. It will be left until the problems to show that the noise performance expressed in Eq. 6.1-43 is also valid for the current-source-load sinking inverter. An example follows to illustrate the stated relationships for Fig. 6.1-11*b*.

Example 6.1-2. AC performance of the inverter of Fig. 6.1-11*b*. Determine the small signal performance of the inverter of Fig. 6.1-11*b* using the model parameters of Table 3.1-2 assuming that $W_1/L_1 = 15\ \mu/10\ \mu$, $W_2/L_2 = 5\ \mu/10\ \mu$, $V_{BP} = 2$ V, and $V_{DD} = -V_{SS} = 5$ V. The drain and source area (periphery) of M1 and M2 are $150\mu^2$ (50μ) and $50\mu^2$ (30μ), respectively. Follow the approach of Ex. 6.1-1 to calculate the capacitances. Assume that V_{out} is biased at 0 V. Also assume that the noise is white noise given in Eq. 3.1-34 and find the equivalent input-noise-voltage spectral density.

Solution. We begin by finding the dc current in M1 and M2, calculating the value of V_{G1}, and determining the region of operation for M1. From the given dc voltage, we know that M2 is saturated. The dc current can be found from the voltage drop across M2 and is

$$I = \frac{K_P' W_2}{2L_2}(V_{DD} - V_{BP} - |V_{T2}|)^2[1 + \lambda_P(V_{DD} - V_{out})] = \frac{8(5)}{2(10)}(3 - 0.75)^2(1 + 0.1)\ \mu A = 11.14\ \mu A$$

Assume that M1 is saturated. The value of V_{GS1} that gives 11.14 μA is found from the following equation ignoring channel modulation effects on M1.

$$V_{gs1} = V_{T1} + \left(\frac{2I L_1}{K_N' W_1}\right)^{0.5} = 0.75 + \left[\frac{(2)(11.14)(10)}{(24)(15)}\right]^{0.5} = 0.75 + 0.79 = 1.54\ V$$

Thus, M1 is in fact saturated and $V_{out} = 0$ V corresponds to $V_{in} = -3.46$ V, as seen in Fig. 6.1-14.

Next, we calculate the small signal parameters for M1 and M2. Using the formulas of Table 3.1-3 gives $g_{m1} = 28.32\mu S$, $g_{ds1} = 0.11\mu S$, $g_{m2} = 9.44\mu S$, and $g_{ds2} = 0.22\mu S$.
Equation 6.1-11 gives

$$A_v = \frac{-28.32}{0.11 + 0.22} = -84.74$$

Equation 6.1-13 gives

$$r_{out} = \frac{1}{(0.11 + 0.22)\mu S} = 2.99\ M\Omega$$

The capacitors of Eq. 6.1-56 are found using the formulas of Fig. 3.1-19*b* and the capacitances of Table 28.4. The value of n in Equation 3.1-14 will be 0.5 for both the bottom and sidewall junction capacitances. The capacitances of Eq. 6.1-56 are

$$C_{BD1} = (0.33)(150)[1 + (5/.6)]^{-0.5} + (0.9)(50)[1 + (5/.6)]^{-0.5} = 30.93fF$$

$$C_{GD2} = (0.7)(0.6)(5) = 2.1fF$$

$$C_{BD2} = (0.38)(50)[1 + (5/.6)]^{-0.5} + (1)(30)[1 + (5/.6)]^{-0.5} = 16.04fF$$

$$C_{GD1} = (0.7)(0.45)(15) = 4.73fF$$

Substituting the above values in Eq. 6.1-56 gives

$$\omega_{-3dB} = \frac{0.33\ \mu S}{30.93\ fF + 2.1\ fF + 16.04\ fF + 4.73\ fF} = 6.13\ Mrps$$
$$= 0.976\ MHz$$

Dividing the spectral noise density of Eq. 3.1-34 by g_m^2 gives for M1

$$S_{VWN} = 3.90 \times 10^{-16} V^2/\text{Hz}$$

and for M2

$$S_{VWP} = 11.70 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density can be found from Eq. 6.1-43 by replacing each mean-square noise voltage by its noise spectral density and is

$$S_{eq} = S_{VWN} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VWP} =$$

$$3.90 \times 10^{-16} + \left(\frac{9.44}{28.32}\right)^2 11.70 \times 10^{-16} = 5.20 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density is equal to 22.8 $\text{nV}/\sqrt{\text{Hz}}$.

The performance of the inverter of this example is seen to have a high gain, a high output resistance, a moderate bandwidth, and a noise primarily determined by that of the MOS devices rather than the inverter configuration. As before, the performance can be altered by changing the bias current or the W and L values of M1 and M2.

There is one important difference in the potential noise performance of this inverter compared with the previous ones. Assume that the inverter is used in the first stage of an amplifier. Even though the equivalent input noise levels of the inverters are approximately equal, the inverter of Fig. 6.1-11*b* would be a much better choice for lower noise performance because its gain can be higher, causing the noise of the following stages to have less effect on the overall noise of the amplifier.

The remaining sinking inverter of Fig. 6.1-11 is the depletion-load sinking inverter (Fig. 6.1-11*d*). This inverter requires the technology that offers the ability to make n-channel transistors with a negative threshold voltage. If the gate and source of a depletion transistor are connected, a well-defined drain current will flow if $V_{DS} > 0$. Unfortunately, the depletion n-channel transistor of Fig. 6.1-11*d* is susceptible to bulk effects because its source is not at V_{SS}. This causes the load resistance to be approximately g_{mb2}, which is an improvement over the active-load sinking inverter of Fig. 6.1-11*a* but not as high as the current-source-load sinking inverter. If the inverter of Fig. 6.1-11*d* is used in Example 6.1-1 with the same W/L values for M1 and M2, the ac gain is -15.89, the ac output resistance is 312 kΩ, the bandwidth is 6.83 MHz, and the equivalent input-referred noise-voltage spectral density is 17.3 $\text{nV}/\sqrt{\text{Hz}}$.

The preceding MOS inverter realizations all correspond to the sinking inverter architecture of Fig. 6.1-3*a*. MOS realizations of the sourcing inverter architecture of Fig. 6.1-3*b* can be found by simply taking the inverse of the realizations of Fig. 6.1-11. The *inverse* here means to interchange V_{DD} and V_{SS} and to interchange each p-channel and n-channel transistor. In the sourcing inverter architecture, all of the voltage-controlled current sources are p-channel devices. As a result, for the same W and L values and dc currents, the sinking inverters

will have a larger gain than the sourcing inverters because K'_N is greater than K'_P. The analysis of the sourcing inverters is left to the reader.

The remaining architecture of Fig. 6.1-3 that will be considered is the push-pull inverter of Fig. 6.1-3*c*. This inverter has only the CMOS realization shown in Fig. 6.1-15*a*. The voltage transfer curve can be found using the reasoning behind Fig. 6.1-4*c*. Figure 6.1-16 shows the resulting voltage transfer curve for the push-pull CMOS inverter when $W_1 = 5\ \mu$, $L_1 = 10\ \mu$, $W_2 = 15\ \mu$, $L_2 = 10\ \mu$, and $V_{DD} = -V_{SS} = 5$ V, using a CMOS technology corresponding to the parameters in Table 3.1-2. The SPICE input file necessary to generate this plot is included in the figure. Note that the W and L values have been changed in Fig. 6.1-16 so that the transition region is centered about $V_{IN} = 0$ V. The transition region of the push-pull CMOS inverter is much easier to design with respect to V_{IN} than any of the other inverters. The approach used in the design of the push-pull inverter of Fig. 6.1-16 is called *equal resistance*. If the product of K' and (W/L) are equal for both the n-channel and p-channel devices, then the design will have equal resistance or equal sinking and sourcing capability when V_{IN} is midway between the power supplies. An alternate approach is called *equal area* and uses equal values of W and L for both devices.

The regions of operation are identified in Fig. 6.1-16 using the previous methods. In the following analysis we will assume that both transistors are in the saturation mode, which corresponds to the steepest part of the transition region. Note that the current flowing through M1 and M2 is also plotted in Fig. 6.1-16. The scaling for the current is 20 μA = 1 V. It is seen that the current is highest in the transition region, reaching a peak value of approximately 115 μA.

The operating point of the inverter of Fig. 6.1-15*a* is difficult to calculate because both transistor drain currents are dependent on V_{IN}. The best way to

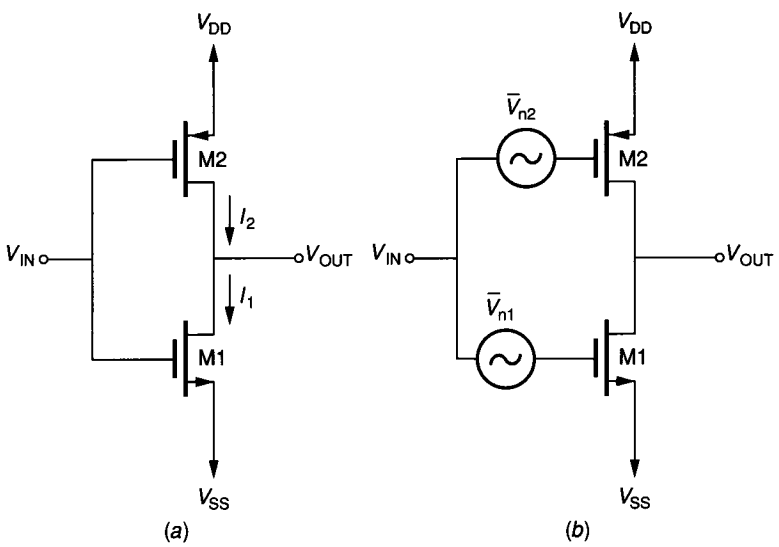


FIGURE 6.1-15
(*a*) Push-pull inverter, (*b*) Noise model of Fig. 6.1-15*a*.

design the operating point would be to use some form of negative dc feedback. For our consideration, we will assume the bias point has been established in the transition region, where both transistors are operating in saturation. Equating I_{D1} to I_{D2} results in the following relationship for Fig. 6.1-15*a*.

$$\frac{K'_N W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2[1 + \lambda_N(V_{OUT} - V_{SS})] = \frac{K'_P W_2}{2L_2}(V_{DD} - V_{IN} - V_{T2})^2[1 + \lambda_P(V_{DD} - V_{OUT})] \quad (6.1\text{-}57)$$

Differentiating Eq. 6.1-57 with respect to V_{IN} results in the slope of the voltage transfer curve in the transition region. Applying Eq. 6.1-3 to Eq. 6.1-57 results in

$$A_v = \frac{v_{out}}{v_{in}} = \frac{\partial V_{OUT}}{\partial V_{IN}}\bigg|_Q \approx -\frac{[2K'_N(W_1/L_1)I]^{0.5} + [2K'_P(W_2/L_2)I]^{0.5}}{\lambda_N I + \lambda_P I}$$

$$= -\frac{[2K'_N(W_1/L_1)]^{0.5} + [2K'_P(W_2/L_2)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \quad (6.1\text{-}58)$$

where channel modulation effects in Eq. 6.1-57 have been ignored after differentiation, and I is the dc current flowing through both M1 and M2.

The small signal model of the circuit of Fig. 6.1-6 can also be used to calculate A_v. From Chapter 3, we know that $g_i = 0$, $g_m = g_{m1} + g_{m2}$, and $g_o = g_{ds1} + g_{ds2}$. Equation 6.1-11 gives the small signal voltage gain as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}} = -\frac{[2K'_N(W_1/L_1)]^{0.5} + [2K'_P(W_2/L_2)]^{0.5}}{(\lambda_N + \lambda_P)(I)^{0.5}} \quad (6.1\text{-}59)$$

As expected, the two approaches to finding A_v give identical results. Using the small signal model, we can find the input and output resistances as

$$r_{in} = \infty \quad (6.1\text{-}60)$$

and

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} \quad (6.1\text{-}61)$$

The push-pull inverter of Fig. 6.1-15*a* also has the property that the ac gain is inversely proportional to the square root of the dc bias current.

The frequency response of the circuit of Fig. 6.1-15*a* can be found by inserting the transistor capacitors of Example 3.1-5 into the circuit of Fig. 6.1-15*a* and comparing it with Fig. 6.1-8. C_1, C_2, and C_3 of Fig. 6.1-8 become

$$C_1 = C_{GS1} + C_{GB1} + C_{GS2} + C_{GB2} \quad (6.1\text{-}62)$$

$$C_2 = C_{BD1} + C_{BD2} \quad (6.1\text{-}63)$$

and

$$C_3 = C_{GD1} + C_{GD2} \quad (6.1\text{-}64)$$

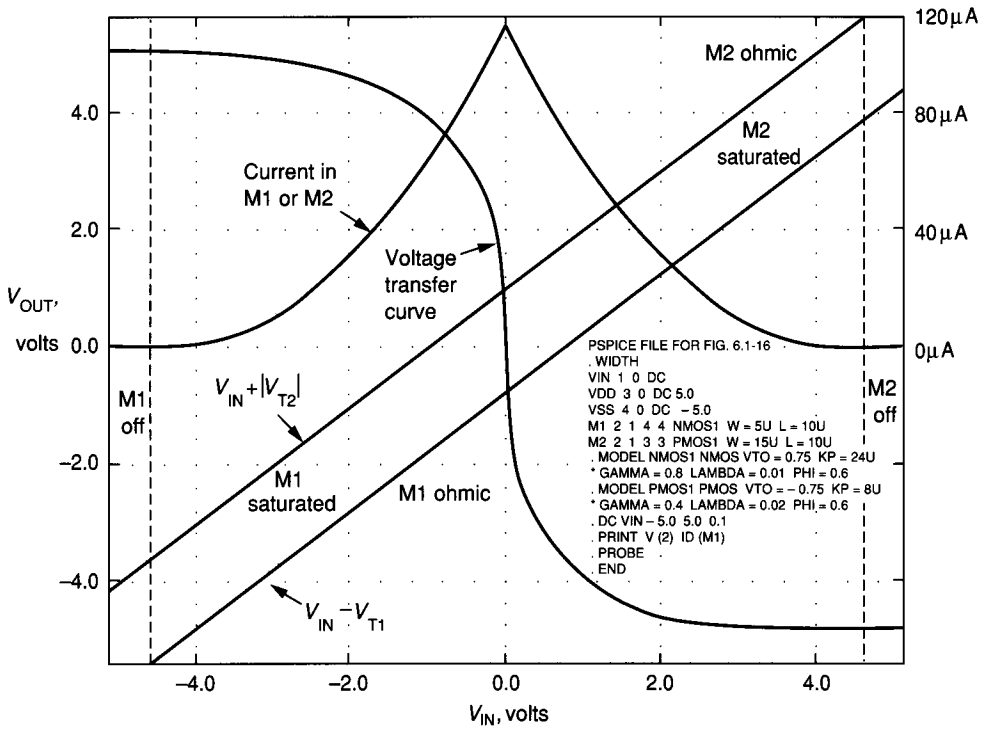


FIGURE 6.1-16
VTC of the push-pull CMOS inverter.

Therefore, the upper -3 dB frequency for the voltage-driven inverter of Fig. 6.1-15*a* is found from Eq. 6.1-22 as

$$\omega_{-3dB} \approx \frac{g_{ds1} + g_{ds2}}{C_{BD1} + C_{BD2} + C_{GD1} + C_{GD2}} \tag{6.1-65}$$

The noise of the push-pull inverter of Fig. 6.1-15*a* is modeled in Fig. 6.1-15*b*, where an input-noise-voltage spectral density source has been used to model the noise of each device. The noise spectral density at the output is

$$S_o = g_{m1}^2 (r_{out})^2 S_{VN1} + g_{m2}^2 (r_{out})^2 S_{VN2} \tag{6.1-66}$$

where r_{out} is given by Eq. 6.1-61. Dividing Eq. 6.1-66 by the square of the gain given in Eqs. 6.1-58 or 6.1-59 gives

$$S_{eq.} = \left[\frac{g_{m1}}{g_{m1} + g_{m2}}\right]^2 S_{VN1} + \left[\frac{g_{m2}}{g_{m1} + g_{m2}}\right]^2 S_{VN2} \tag{6.1-67}$$

If the transconductances are balanced ($g_{m1} = g_{m2}$), then the noise contribution of each device is 50% of the total if $S_{VN1} = S_{VN2}$. The total noise contribution can

be reduced only by reducing the noise contributed by each device. An example follows to illustrate these relationships for the CMOS push-pull inverter of Fig. 6.1-15*a*.

Example 6.1-3. AC performance of the inverter of Fig. 6.1-15. Determine the small signal performance of the inverter of Fig. 6.1-15 using the model parameters of Table 3.1-2 assuming that $W_1/L_1 = 5\ \mu/10\ \mu$, $W_2/L_2 = 15\ \mu/10\ \mu$, and $V_{DD} = -V_{SS} = 5$ V. The drain and source area (periphery) of M1 and M2 are 150 μ^2 (50 μ) and 50 μ^2 (30 μ), respectively. Assume that V_{out} is biased at 0 V. Also assume that the noise in each transistor is white noise given in Eq. 3.1-34 and find the equivalent input-noise-voltage spectral density.

Solution. The dc current in M1 and M2 can be written as

$$I_1 = \frac{K_N' W_1}{2L_1}(V_{IN} - V_{SS} - V_{T1})^2[1 + \lambda_N(V_{out} - V_{SS})]$$

$$I_2 = \frac{K_P' W_2}{2L_2}(V_{DD} - V_{IN} - |V_{T2}|)^2[1 + \lambda_P(V_{DD} - V_{out})]$$

Setting $I_1 = I_2$ and solving simultaneously (by iteration), we obtain $V_{IN} = 0.05$ V and $I_1 = I_2 = 116.4\mu$A. The value of V_{IN} when $V_{OUT} = 0$ is called the *systematic offset voltage*. This offset voltage should be distinguished from that due to mismatches in device model parameters.

Next we calculate the small signal parameters for M1 and M2. Using the formulas of Table 3.1-3 gives $g_{m1} = 52.88\ \mu$S, $g_{ds1} = 1.17\ \mu$S, $g_{m2} = 52.88\ \mu$S, and $g_{ds2} = 2.33\ \mu$S.

Equation 6.1-11 gives

$$A_v = \frac{-(52.88 + 52.88)}{1.17 + 2.33} = -30.3$$

Equation 6.1-13 gives

$$r_{out} = \frac{1}{(1.17 + 2.33)\mu\text{S}} = 285.7\ \text{k}\Omega$$

The capacitors of Eq. 6.1-65 are found using the formulas of Fig. 3.1-19b and the capacitances of Table 2B.4. The value of n in Eq. 3.1-14 will be 0.5 for both the bottom and sidewall junction capacitances. The capacitances of Eq. 6.1-65 are

$$C_{BD1} = (0.33)(150)[1 + (5/.6)]^{-0.5} + (0.9)(50)[1 + (5/.6)]^{-0.5} = 30.93\ \text{fF}$$

$$C_{BD2} = (0.38)(50)[1 + (5/.6)]^{-0.5} + (1)(30)[1 + (5/.6)]^{-0.5} = 16.04\ \text{fF}$$

$$C_{GD1} = (0.7)(0.45)(15) = 4.73\ \text{fF}$$

$$C_{GD2} = (0.7)(0.6)(5) = 2.10\ \text{fF}$$

Substituting the above values in Eq. 6.1-56 gives

$$\omega_{-3dB} = \frac{3.50\ \mu\text{S}}{30.93\ \text{fF} + 16.04\ \text{fF} + 2.10\ \text{fF} + 4.73\ \text{fF}} = 65.06\ \text{Mrps or } 10.35\ \text{MHz}$$

Because $S_{VWN} = S_{VWP} = S_{VW}$, equation 6.1-67 gives

$$S_{eq} = (0.25 + 0.25)S_{VW} = 1.045 \times 10^{-16} V^2/\text{Hz}$$

The equivalent input-noise-voltage spectral density is equal to 10.2 nV/$\sqrt{\text{Hz}}$

To compare the performance of the inverter of Example 6.1-3 with that of the previous inverters, it is necessary to have the same currents. Multiplying A_v of Ex. 6.1-3 by the square root of 116.4/11.14 gives a voltage gain of -98. With equal W/L values and dc current, the push-pull inverter will have the largest voltage gain. The push-pull inverter can both sink and source output current proportional to the input voltage, which is very useful in output amplifier applications.

The MOS inverters presented in this section represent the more useful realizations of the voltage inverter. The realizations include inverters with active loads, current sink/source loads, depletion transistor loads, and push-pull inverters. A physical layout for the inverters of Fig. 6.1-11*b*, *c*, and *d* and Fig. 6.1-15*a* is shown in Fig. 6.1-17. The technology for this layout is a p-well CMOS technology having the capability of depletion n-channel devices. The ac performance of the inverters discussed in the section is summarized in Table 6.1-1.

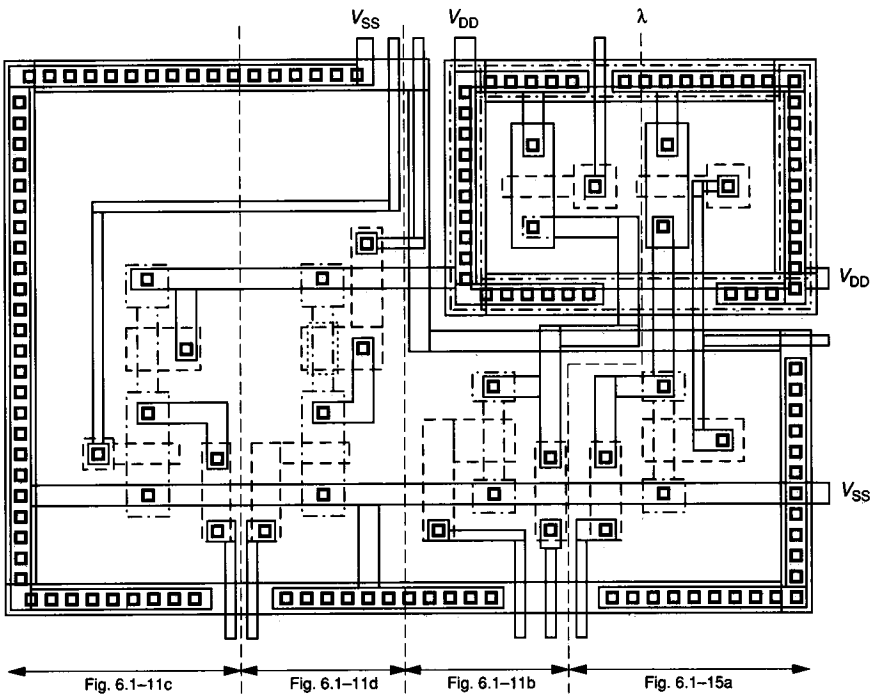


FIGURE 6.1-17
Physical layout of Fig. 6.1-11*b*, *c*, *d* and Fig. 6.1-15*a*.

TABLE 6.1-1
Comparison of the small signal performance of MOS inverters

Inverter	Figure	AC voltage gain	AC output resistance	Bandwidth ($C_{GB} = 0$)	Equivalent, input-referred, mean-square noise voltage
p-channel active load sinking inverter	6.1-11*a*	$\frac{-g_{m1}}{g_{m2}}$	$\frac{1}{g_{m2}}$	$\frac{g_{m2} + g_{mb2}}{C_{BD1} + C_{GD1} + C_{GS2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
n-channel active load sinking inverter	6.1-11*c*	$\frac{-g_{m1}}{g_{m2} + g_{mb2}}$	$\frac{1}{g_{m2} + g_{mb2}}$	$\frac{g_{m2} + g_{mb2}}{C_{BD1} + C_{GD1} + C_{GS2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
Current source load sinking inverter	6.1-11*b*	$\frac{-g_{m1}}{g_{ds1} + g_{ds2}}$	$\frac{1}{g_{ds1} + g_{ds2}}$	$\frac{g_{ds1} + g_{ds2}}{C_{BD1} + C_{GD1} + C_{GD2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
n-channel depletion load sinking inverter	6.1-11*d*	$\sim\frac{-g_{m1}}{g_{mb2}}$	$\frac{1}{g_{mb2} + g_{ds1} + g_{ds2}}$	$\frac{g_{mb1} + g_{ds1} + g_{ds2}}{C_{BD1} + C_{GD1} + C_{GD2} + C_{BD2}}$	$\overline{V}_{n1}^2 \left(\frac{g_{m1}}{g_{m2}}\right)^2 + \overline{V}_{n2}^2$
Push-pull inverter	6.1-15*a*	$\frac{-(g_{m1} + g_{m2})}{g_{ds1} + g_{ds2}}$	$\frac{1}{g_{ds1} + g_{ds2}}$	$\frac{g_{ds2} + g_{ds2}}{C_{BD1} + C_{GD1} + C_{GD2} + C_{BD2}}$	$\left(\frac{\overline{V}_{n1}^2 g_{m1}}{g_{m1} + g_{m2}}\right)^2 + \left(\frac{\overline{V}_{n2}^2 g_{m2}}{g_{m1} + g_{m2}}\right)^2$

6.1.3 BJT Inverting Amplifiers

The general concepts of inverting amplifiers can also be applied to BJT technology. However, the differences between BJT and MOS transistors reduces the number of practical BJT inverter realizations to one. This conclusion can be understood by examining the BJT active loads of Fig. 5.2-3. The voltage drop across the BJT active load is found to be limited to approximately 0.8 V in the forward-biased direction. The limitation is due to the exponential characteristic of the BJT and the fact that large forward-bias voltages will create extremely large currents. The result is that, unlike MOS active loads with their square law characteristic, BJT active loads are constrained to voltages less than 0.8 V. If a BJT active load is used in the generic inverter configuration of Fig. 6.1-3*a* and *b*, the output voltage would be limited to approximately 0.8 V below V_P or above V_N, respectively. The same reasoning applies to the push-pull inverter architecture of Fig. 6.1-3*c*. Therefore, the only practical inverter configurations for BJT technology are shown in Fig. 6.1-3*a* and *b* where the load is implemented by a current source or current sink, respectively.

Figure 6.1-18 shows the two possible configurations of the BJT inverting amplifier. The voltage transfer curve of the circuit of Fig. 6.1-18*a* can be found using the approach demonstrated in the circuit of Fig. 6.1-4 for the MOS inverting amplifiers. When V_{IN} is at V_{EE}, Q1 is off and no current is flowing in the inverter. Q2 is biased so that if current can flow, it will be determined by the difference between V_{CC} and V_{BB2} and the transistor characteristics of Q2. When V_{IN} is about 0.5 V above V_{EE}, Q1 begins to turn on and current starts to flow in the inverter. At the same time, the output voltage starts to make the transition from V_{CC} to V_{EE}. As V_{IN} approaches 0.6 to 0.7 V above V_{EE}, Q1 saturates and the output voltage is at V_{EE}. In the transition region, it follows from Eq. 3.3-20 that the current flowing in the inverter is given as

$$I_{C2} = I_{s2} \exp\left(\frac{V_{CC} - V_{BB2}}{V_t}\right)\left(1 + \frac{V_{CC} - V_{OUT}}{V_{AFP}}\right) \tag{6.1-68}$$

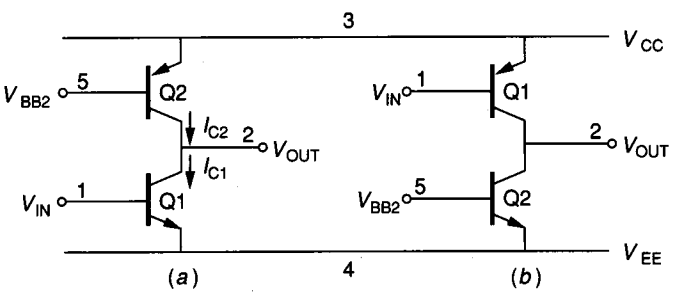


FIGURE 6.1-18
Practical BJT implementations of: (*a*) Sinking inverter, (*b*) Sourcing inverter.

Figure 6.1-19 shows the simulation of the circuit of Fig. 6.1-18*a* when $V_{CC} = -V_{EE} = 5$ V, $V_{BB2} = 4.25$ V, and the transistors have the parameters of Table 6.1-2. In the simulation both the pnp and npn transistors have an emitter area of 500 μ^2 and $V_t = 0.0259$ V. The current in the inverter is also shown in Fig. 6.1-19. Using the model parameters of Table 6.1-2 and assuming that V_{out} is -5 V gives $I_{c1} = 1.67$ mA, which is close to the 1.61 mA indicated in Fig. 6.1-19.

It should be noted that the transition region is very narrow and the slope is large, indicating a large small signal gain. The small signal voltage gain in the transition region can be found by equating the current in Q1 to the current in Q2, resulting in

$$I_{s1} \exp\left(\frac{V_{IN} - V_{EE}}{V_t}\right)\left(1 + \frac{V_{OUT} - V_{EE}}{V_{AFN}}\right) = I_{s2} \exp\left(\frac{V_{CC} - V_{BB2}}{V_t}\right)\left(1 + \frac{V_{CC} - V_{OUT}}{V_{AFP}}\right) \quad (6.1\text{-}69)$$

Differentiating Eq. 6.1-69 with respect to V_{IN} and using Eq. 6.1-3 gives the small signal voltage gain as

$$A_v = \left.\frac{\partial V_{OUT}}{\partial V_{IN}}\right|_Q = \frac{-(1/V_t)}{(1/V_{AFN}) + (1/V_{AFP})} \quad (6.1\text{-}70)$$

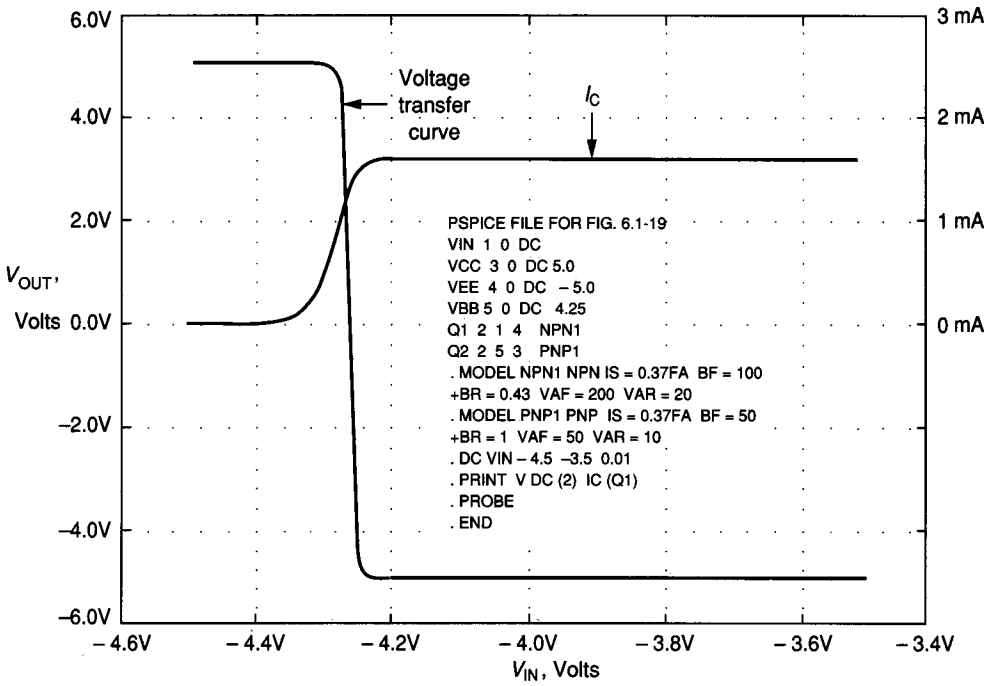


FIGURE 6.1-19
Voltage transfer curve of Fig. 6.1-18*a*.

TABLE 6.1-2
Typical BJT model parameters

Parameter	NPN	PNP	Units
J_s	6×10^{-16} 9.3×10^{-19}	6×10^{-16} 9.3×10^{-19}	A/mil^2 A/μ^2
I_s (Emitter area = 500 μ^2)	0.37	0.37	fA
β_F	100	50	A/A
β_R	0.43	1	A/A
V_{AF}	200	50	Volts
V_{AR}	20	10	Volts
τ_f	0.4	20	ns
C_{je0}	0.5	0.5	pF
C_{jc0}	0.5	0.5	pf
ϕ	0.55	0.55	Volts
$V_t = 0.0259$ V at room temperature ($300^\circ K$)			

Equation 6.1-70 shows that the voltage gain of the BJT inverter in Fig. 6.1-18 is large and is independent of bias current. Using the parameters of Table 6.1-2 gives a small signal voltage gain of -1544. The large gain is typical of BJT inverters using current sink/source loads.

The small signal model of the circuit of Fig. 6.1-18 is shown in Fig. 6.1-20. The small signal model parameters shown are related to the large signal model parameters in Table 3.2-4. The ac voltage gain can easily be shown to be

$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{o1} + g_{o2}} = \frac{-(I_{C1}/V_t)}{(I_{C1}/V_{AFN}) + (I_{C2}/V_{AFP})} = \frac{-(1/V_t)}{(1/V_{AFN}) + (1/V_{AFP})} \tag{6.1-71}$$

which is identical to Eq. 6.1-70 and where $I_{C1} = I_{C2} = I_{CQ}$. The principle that the gain can be calculated from the large signal or small signal model is again verified. In the case of the BJT inverter, the small signal input resistance is not infinity and is found as

$$r_{in} = r_{\pi 1} \tag{6.1-72}$$

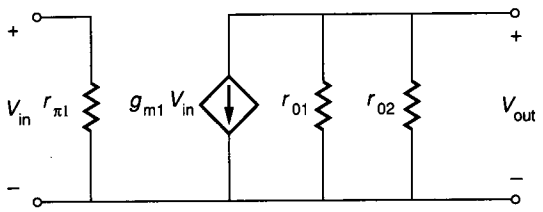


FIGURE 6.1-20
Small signal, midband model for Fig. 6.1-18 *a* or *b*.

The output resistance of Fig. 6.1-18 is

$$r_{out} = \frac{1}{g_{o1} + g_{o2}} = \frac{1}{I_{CQ}[(1/V_{AFN}) + (1/V_{AFP})]} \tag{6.1-73}$$

The frequency response of the voltage-driven BJT inverter can be found by inserting the parasitic capacitances of the BJT inverter in the small signal model of Fig. 6.1-8. Assume that Q1 is a vertical NPN and that Q2 is a lateral PNP. Fig. 3.3-11, Fig. 3.3-12, and Table 3.3-5 result in Fig. 6.1-21 where $C_{BE} + C_{AC} = C_\pi$ and $C_{CB} = C_\mu$. Therefore, the capacitances of Fig. 6.1-8 become

$$C_1 = C_{BE1} = C_{\pi 1} \tag{6.1-74}$$

$$C_2 = C_{CB2} + C_{CS1} = C_{\mu 2} + C_{CS1} \tag{6.1-75}$$

and

$$C_3 = C_{CB1} = C_{\mu 1} \tag{6.1-76}$$

The upper -3 dB frequency is given by Eq. 6.1-22 as

$$\omega_{-3dB} = \frac{g_{o1} + g_{o2}}{C_{\mu 2} + C_{\mu 1} + C_{CS1}} \tag{6.1-77}$$

The upper -3 dB frequency for a current-driven inverter is given by Eq. 6.1-29 as

$$\omega_{-3dB} \cong \frac{g_{\pi 1}(g_{o1} + g_{o2})}{g_{m1} C_{\mu 1}} \tag{6.1-78}$$

In many cases, the output of the inverter sees a load capacitance which must be incorporated into C_2 of Eq. 6.1-75.

The noise performance of the BJT inverter can be found in a similar manner as for the MOS inverters. Figure 6.1-22 shows a model suitable for calculating the noise. The noise sources will be assumed to be noise-voltage spectral density sources. The form of these sources is determined by the type of noise the designer is interested in analyzing. The noise spectral density of the output of Fig. 6.1-18 is found by superimposing the influence of S_{VN1} and S_{VN2} to get

$$S_{OUT} = S_{VN1} A_v^2 + S_{VN1} A_v^2 \left(\frac{S_{VN2}}{S_{VN1}} \right) \tag{6.1-79}$$

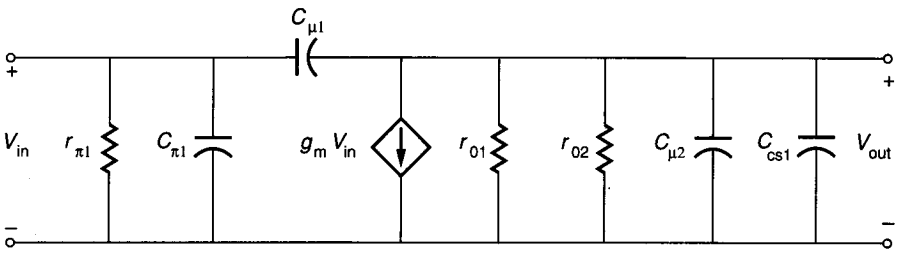


FIGURE 6.1-21
Small signal, high-frequency model for Fig. 6.1-18 *a* or *b*.

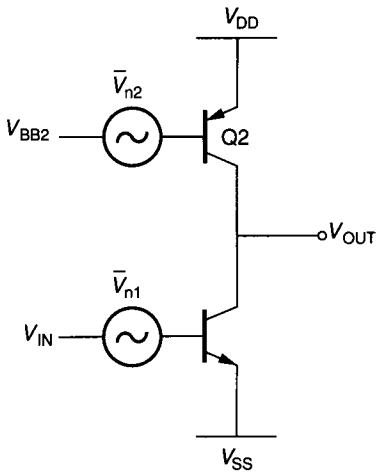


FIGURE 6.1-22
Model for noise calculations of Fig. 6.1-18*a*.

The equivalent noise-voltage spectral density at the input of the BJT can be found by dividing Eq. 6.1-79 by A_v^2. The result is

$$S_{eq} = S_{VN1}\left[1 + \left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{S_{VN2}}{S_{VN1}}\right)\right] \tag{6.1-80}$$

It is seen that the BJT inverter noise performance is the same form as that of the MOS inverter given by Eq. 6.1-43. When the form of the noise-voltage spectral density of the BJT is known, then Eq. 6.1-80 can be used to predict the noise performance. The current noise spectral densities of the BJT are given as

$$S_{IC} = 2qI_C \ (V^2/\text{Hz}) \tag{6.1-81}$$

and

$$S_{IB} = \left[2qI_B + \frac{K_F I_B^{AF}}{f}\right] (V^2/\text{Hz}) \tag{6.1-82}$$

where I_C and I_B are dc currents of the transistor, K_F is the $1/f$ noise constant, and AF is an exponent. Eq. 6.1-81 is the shot noise at the collector and Eq. 6.1-82 consists of both shot and 1/f noise at the base. These noise spectral densities are assumed to be uncorrelated.

The BJT inverters of Fig. 6.1-18 are identical in their small signal performance. An example follows to illustrate the small signal performance of the BJT inverter of Fig. 6.1-18.

Example 6.1-4. AC performance of the BJT inverter of Fig. 6.1-18*a*. Find the small signal performance of the BJT inverter of Fig. 6.1-18*a* using the model parameters of Table 6.1-2. Assume $V_{BB2} = 4.25$ V, $V_t = 25.9$ mV, $V_{CC} = -V_{EE} = 5V$, and that the inverter is biased so that V_{out} is at 0 V. Assume that the emitter

areas of both transistors are 500 μ^2 and the collector-substrate area of Q1 is 50 $\mu \times$ 100 μ. If the shot noise spectral density of Eq. 6.1-81 is dominant find the equivalent input-noise-voltage spectral density.

Solution. We begin by finding the dc current in Q1 and Q2. The dc current can be found from Eq. 6.1-68;

$$I_{C2} = (0.37\text{fA}) \left[\exp\left(\frac{0.75}{0.0259}\right)\right]\left(1 + \frac{5}{50}\right) = 1.53 \text{ mA}$$

Next we calculate the small signal parameters for Q1 and Q2. Using the formulas of Table 3.3-4 gives

$$g_{m1} = \frac{I_{C1}}{V_t} = \frac{1.53 \text{ mA}}{0.0259} = 0.059 \text{ S}$$

$$g_{o1} = \frac{I_{C1}}{V_{AFN}} = \frac{1.53 \text{ mA}}{200} = 7.67 \ \mu\text{S}$$

and

$$g_{o2} = \frac{I_{C2}}{V_{AFP}} = \frac{1.53 \text{ mA}}{50} = 30.7 \ \mu\text{S}$$

Equations 6.1-70 and 6.1-71 give

$$A_v = \frac{-0.059 \times 10^6}{7.67 + 30.7} = -1544$$

Equation 6.1-72 gives

$$r_{in} = r_{\pi 1} = \frac{\beta_F}{g_{m1}} = \frac{100}{0.059\text{S}} = 1.695 \ \Omega$$

Equation 6.1-73 gives

$$r_{out} = \frac{10^6}{7.67 + 30.7} = 26.06 \text{ k}\Omega$$

Next we must calculate the value of capacitances that determine the frequency behavior. Assuming V_{IN} is approximately 0.7 V gives $V_{CB1} = 4.3$ V. From Eq. 3.1-19 with $n = 0.5$, we find that $C_{CB1} = 0.168$ pF. Similarly, for Q2 we have $V_{CB2} = 4.25$ V, giving $C_{CB2} = 0.169$ pF. It is customary to estimate C_{BE1} of Table 3.3-5 as $2C_{je0}$, or 1 pF. With τ_f from Table 6.1-2 equal to 0.4 ns, Eq. 3.3-32 gives C_{AF1} as 23.6 pF. Table 2C.4 gives the zero-bias collector-substrate capacitance of 0.79 pF. Since the collector-substrate has a back bias of 5 V, $C_{CS1} = 0.335$ pF. Thus,

$$C_{\mu 1} = C_{CB1} = 0.168 \text{ pF}$$

$$C_{\pi 1} = C_{BE1} + C_{AF1} = 24.6 \text{ pF}$$

$$C_{CS1} = 0.335 \text{ pF}$$

and

$$C_{\mu 2} = C_{CB2} = 0.169 \text{ pF}$$

Equation 6.1-77 for the voltage driven inverter gives

$$\omega_{-3dB} = \frac{7.67 \ \mu\text{S} + 30.7 \ \mu\text{S}}{0.168 \text{ pF} + 0.169 \text{ pF} + 0.335 \text{ pF}} = 57.1 \text{ Mrps or } 9.09 \text{ MHz}$$

Equation 6.1-78 for the current driven inverter gives

$$\omega_{-3dB} = \frac{g_{\pi 1}(g_{o1} + g_{o2})}{g_{m1}C_{\mu 1}} = \frac{590\ \mu S(7.67 + 30.7)\ \mu S}{0.059(0.168\ pF)} = 2.28\ \text{Mrps} = 363\ \text{kHz}$$

From Eq. 6.1-81, the collector shot-noise spectral density is

$$S_{IC} = 4.9 \times 10^{-22}\ A^2/\text{Hz}$$

Dividing by g_m^2 gives the equivalent noise voltage spectral density at the base for both transistors as

$$S_{VB} = 4.9 \times 10^{-22}/0.059 = 1.405 \times 10^{-19}\ V^2/\text{Hz}$$

Eq. 6.1-80 gives the equivalent input noise voltage spectral density as 0.53 nV/$\sqrt{\text{Hz}}$.

The small signal analysis and design of inverting amplifiers has been addressed in Section 6.1. It was shown that these amplifiers consist of a voltage-controlled current sink/source and a load. In the case of the CMOS push-pull inverting amplifier, the load was also a voltage-controlled current source. It was seen that the voltage transfer curves of inverting amplifiers have three distinct operating regions. These regions are where the input is low and the output is high, where the input is high and the output low, and a region between these two called the transition region. Because the ac gain is proportional to the slope of the voltage transfer curve, the high gain inverting amplifier should be biased in the region with the steepest slope, which is the transition region. It was shown that in the transition region, the transistors are all operating in their normal regions of operation: the saturation region for the MOSFET and the forward-active region for the BJT. Therefore, the small signal model for the normal-region operation was used to predict the performance of the inverters considered in this section. The performance variables include the small signal voltage gain, the input resistance, the output resistance, the -3 dB bandwidth, and noise.

The inverter or inverting amplifier is a basic gain block and should be well understood before the following sections are studied. An example follows on how the designer approaches the implementation of an amplifier using an inverting amplifier. This example will show some of the tradeoffs that can be made based on the considerations presented in this section. It will also show some of the limitations of the inverter and why we must consider other types of amplifiers.

Example 6.1-5. Assume that you are to design an inverting amplifier with gain equal to or greater than -100, using power supplies of ± 2.5 V, having a power dissipation less than 1 mW, and using a dc value for both input and output voltages of 0 V. Select among the inverting amplifiers presented in this section. Assume that Tables 3.1-2 and 6.1-2 represent the model parameters of the MOS or BJT, respectively.

Solution. The first consideration is selection of one of the inverter architectures that have been discussed. From the specifications we note that the dc voltage across the voltage-controlled current sink/source will be 2.5 V. This is too much voltage to put across the base-emitter of a BJT, so we are restricted to MOS implementations.

Although only one of the MOS inverters was shown to have zero input dc voltage (the inverter of Fig. 6.1-15*a*), all could be biased with the input and output at 0 V if the *W/L* ratios were designed correctly. Thus, since the gain is large and we have no other specifications to suggest otherwise, let us select the CMOS push-pull inverter of Fig. 6.1-15*a* because it has the largest gain for similar dc current.

The dc current through the inverter will be selected to meet the power supply specification. It is seen that for power supplies of ±2.5 V, any current less than 200 μA will give a power dissipation less than 1 mW. Let us arbitrarily choose a dc current of 100 μA. The next step is to find the W_1/L_1 ratio that will give this current for a gate-source voltage of 2.5 V. Using the large signal equation in the saturation region, we get

$$\frac{W_1}{L_1} = \frac{2I_d}{K'_N(V_{gs1} - V_{TN})^2(1 + \lambda_N V_{ds1})} = \frac{2(100)}{(24)(1.75)^2(1.05)} = 2.59 \approx \frac{5}{2}$$

Solving for W_2/L_2 using the same approach gives

$$\frac{W_2}{L_2} = \frac{2I_d}{K'_P(V_{sg2} - |V_{TP}|)^2(1 + \lambda_P V_{sd2})} = \frac{2(100)}{(8)(1.75)^2(1.1)} = 7.42 \approx \frac{15}{2}$$

Putting these values into Eq. 6.1-59 gives a small signal voltage gain of −73.

Unfortunately, we now face the type of problem that a designer will encounter many times. The design meets two of the three specifications. If we are restricted to inverting amplifiers, what can be done to meet *all* of the specifications? One might be tempted to lower the current since it was shown that the ac gain was inversely proportional to the square of the dc current. However, this relationship only holds when everything else, such as *W/L* values, remains constant. If we attempt this approach, the requirement that $V_{GS1} = 2.5$ V will cause the *W/L* values to change, resulting in the same gain as before. If the preceding formulas for *W/L* are substituted into Eq. 6.1-59, it will be seen that V_{GS} must be changed to produce the correct gain. Unfortunately, this implies changing the power supplies, which is probably beyond the control of the designer. None of the other MOS configurations will meet all three specifications for the same reason that the push-pull CMOS inverter fails. One must turn to other architectures or change the specifications. This example will be reconsidered in the next section.

6.2 IMPROVING THE PERFORMANCE OF INVERTING AMPLIFIERS (CASCODE AMPLIFIERS)

A very useful amplifier called the inverting amplifier was introduced in Section 6.1. The inverting amplifier is intended to invert and amplify small signals. The objective of this section is to take a closer look at the performance of inverting amplifiers. By doing so, we will see areas where the small signal performance can be improved or design constraints eliminated. Some of the topics not addressed in the last section include controlling or designing the frequency response, achieving higher gain, and decoupling the ac and dc design constraints. These topics seriously limit the performance of the inverters of the previous section. For example, if the inverter is current-driven, the bandwidth is severely reduced from

the bandwidth of the voltage-driven inverter. In many of the MOS inverters, an ac gain larger than -100 would be difficult to achieve. Example 6.1-5 illustrated the problems that develop between ac and dc specifications. In that example, we saw that it was impossible to satisfy all the design requirements simultaneously.

Let us first examine how the designer can control the frequency response of an inverting amplifier. Assume that the source can be represented by a Thevenin or Norton form having a source resistance of R_s. If the voltage amplifier of Fig. 6.1-8 is voltage-driven, then $R_s = 0$ and the -3 dB bandwidth is given from Eq. 6.1-22 as

$$\omega_{-3dB}(R_s = 0) = \frac{g_2}{C_2 + C_3} \tag{6.2-1}$$

where R_s is the resistance of the input source. If R_s is large, then the amplifier is current-driven. If this amplifier is current-driven, we have shown in Eqs. 6.1-27 and 6.1-28 that the poles are widely spaced and the -3 dB bandwidth is from Eq. 6.1-29

$$\omega_{-3dB}(R_s \neq 0) \approx \frac{g_1 g_2}{g_m C_3} \tag{6.2-2}$$

Since g_m is typically much greater than g_1, the bandwidth of the current-driven inverter is less than the voltage-driven inverter. A useful heuristic viewpoint of the current-driven inverter is shown in Fig. 6.2-1 for the inverting amplifier of the circuit of Fig. 6.1-11*b*. In many circuits, the poles can be closely approximated by the reciprocal product of the resistance and capacitance to ground at a node. In this circuit there are two poles. p_1 is associated with the input and p_2 with the output of the inverter. Typically, R_s is the output of another inverter and is approximately equal to the r_o of a MOSFET. The resistances associated with each pole are approximately the same in most cases. However, because of the Miller effect, the C_{gd1} capacitance is reflected in parallel with the gate and source of M1, causing p_1 normally to be much less than p_2. The objective of the following discussion is to show how to obtain current-driven inverters that have bandwidths approximately equal to those of voltage-driven inverters.

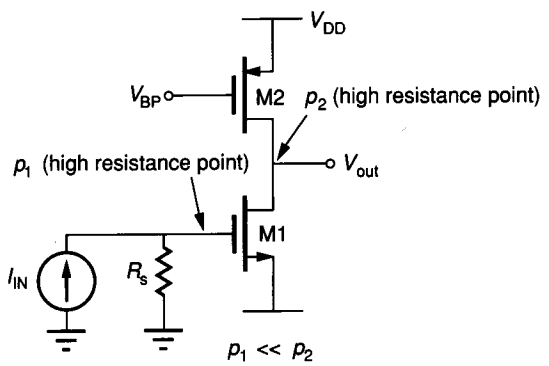


FIGURE 6.2-1
Current-driven CMOS inverter.

6.2.1 Current-Driven CMOS Cascode Amplifier

Consider Fig. 6.2-2, where the voltage-controlled current sink of Fig. 6.1-3*a* has been implemented by the architecture of Fig. 5.3-8*b* rather than the architecture of Fig. 5.3-5*a*. As in Sec. 6.1, the input is at the gate of M1. The gates of M2 and M3 are biased by the dc voltages V_{BP} and V_{BN}, respectively. M3 is called the *cascode transistor* and has a very important influence on the frequency performance. Figure 6.2-3*a* shows the small signal model for Fig. 6.2-2. Note that since the source of M3 is not on V_{SS}, bulk effects must be included. The small signal model can be redrawn as illustrated in Fig. 6.2-3*b*. An important observation is the influence of M3 on the resistance seen by the drain of M1. This resistance has been reduced from a level of $1/g_{ds}$ in the circuit of Fig. 6.1-11*b* to a level of less than $1/g'_{m3}$ (g'_{m3} refers to the sum of g_{m3} and g_{mb3}). The midband, small signal voltage gain from V_1 to V_2 is approximately $-g_{m1}/g'_{m3}$. Considerable mathematical manipulations can be avoided in finding the poles of the circuit of Fig. 6.2-2 if we assume that r_{ds3} is approximately infinity. This results in the approximate circuit shown in Fig. 6.2-3*c*, where the notation of Fig. 6.1-8 has been used for the left-hand part of the circuit. In this case, we can use Eqs. 6.1-27 and 6.1-28 to find the poles of the left-hand part of the circuit. Using the equivalent expressions given in Fig. 6.2-3*c* gives the poles of Fig. 6.2-2 as

$$p_1(\text{cascode}) = -\left[\frac{C_2 + C_3}{g_2} + \frac{C_1 + C_3}{g_1} + \frac{g_{m1}C_3}{g_1 g_2}\right]^{-1} \approx \frac{-g_1}{C_1 + C_3[1 + (g_{m1}/g'_{m3})]} \tag{6.2-3}$$

$$p_2(\text{cascode}) \approx \frac{-g'_{m3}[C_1 + C_3 + C_3(g_{m1}/g'_{m3})]}{C_1C_2 + C_1C_3 + C_2C_3} \tag{6.2-4}$$

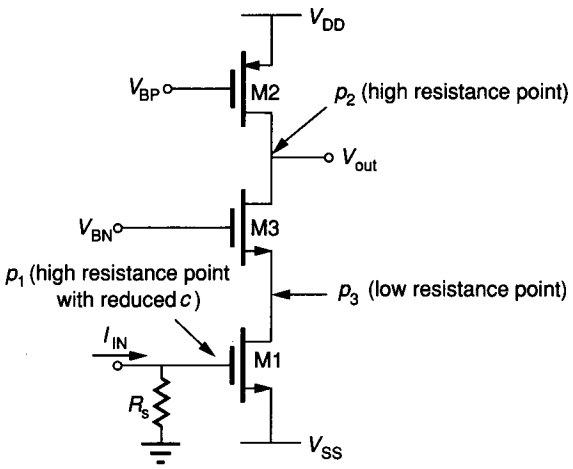


FIGURE 6.2-2
Current-driven cascode inverting amplifier ($V_{BS2} = 0$).

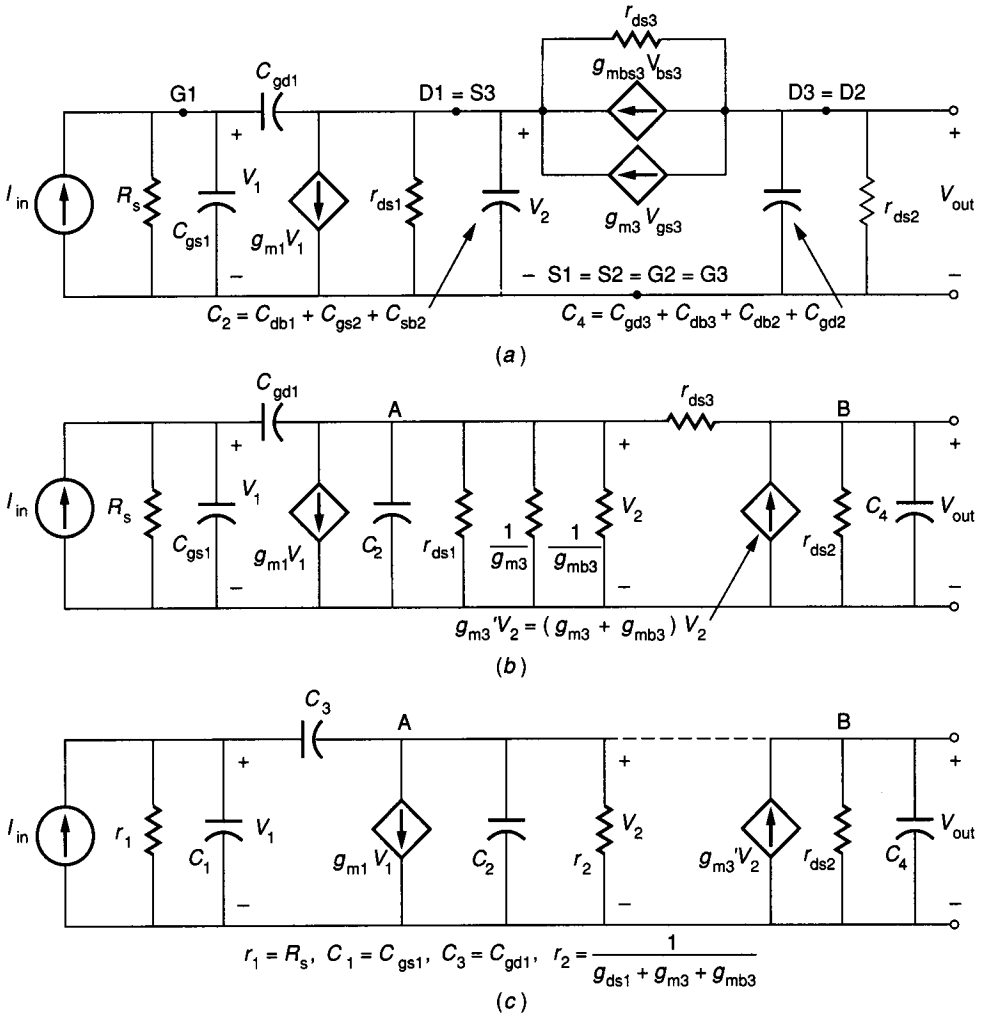


FIGURE 6.2-3
(*a*) Small signal model of Fig. 6.2-2, (*b*) Equivalent model of (*a*), (*c*) Model if r_{ds3} is assumed infinite.

The output pole associated with C_4 is

$$p_3(\text{cascode}) \approx \frac{-g_{o2}}{C_4} \tag{6.2-5}$$

Comparing Eqs. 6.2-3 and 6.2-4 with Eqs. 6.1-27 and 6.1-28 shows that the influence of the cascode transistor (M3) is to bring the input pole back to the value it would have if C_3 were zero ($-g_1/C_1$ as seen from Fig. 6.2-3*c*). The higher inverter pole corresponding to Eq. 6.1-28 and now given by Eq. 6.2-4, has not been influenced very much by the cascode transistor. Looking at

these results and assuming that all capacitors have approximately the same value within a factor of 5, that $g_{m1} \approx g'_{m3}$, and that R_s is less than or equal to r_o, we see that

$$| p_1(\text{cascode}) | \approx | p_3(\text{cascode}) | < | p_2(\text{cascode}) | \tag{6.2-6}$$

6.2.2 Voltage-Driven CMOS Cascode Amplifier

The low-frequency voltage gain of the voltage-driven cascode amplifier can be found from the equivalent circuit of Fig. 6.2-3, by replacing I_{in} with a voltage source and noting that $V_{in} \approx V_1$. The nodal equations at nodes A and B, disregarding the capacitors, can be found as

$$(g_{ds1} + g_{ds3} + g_{m3} + g_{mbs3})V_2 - g_{ds3}V_{out} = -g_{m1}V_1 \tag{6.2-7}$$

$$-(g_{ds3} + g_{m3} + g_{mbs3})V_2 + (g_{ds2} + g_{ds3})V_{out} = 0 \tag{6.2-8}$$

Solving for V_{out}/V_1 gives

$$\frac{V_{out}}{V_1} = \frac{V_{out}}{V_{in}} = \frac{g_{m1}(g_{m3} + g_{mbs3} + g_{ds3})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds2}(g_{m3} + g_{mbs3})} \approx -\frac{g_{m1}}{g_{ds2}} \tag{6.2-9}$$

This gain should be compared with that of Eq. 6.1-50 for the current-source-load sinking inverter of Fig. 6.1-11*b*. Because of the cascode influence of M3 on the output resistance of M1, $g_{ds1}(r_{ds1})$ is no longer important. Thus, under similar conditions, the cascode CMOS inverter should have an ac gain approximately twice that of the simple CMOS inverter of Fig. 6.1-11*b*.

Generally, with the addition of active devices, the equivalent input noise increases. It is of interest to determine the influence of M3 on the noise performance of the cascode CMOS inverter. Figure 6.2-4*a* shows a model appropriate for calculating the noise of the voltage-driven cascode CMOS inverter. Superposition is used to find the contribution of each noise source to the output. The contribution of $\overline{V}_{n3}$ requires particular attention. Figure 6.2-4*b* gives the small signal model that can be used to find the contribution of $\overline{V}_{n3}$. Writing nodal equations gives

$$(g_{ds1} + g_{ds3} + g_{m3} + g_{mb3})V_{s3} - g_{ds3}V_{out} = g_{m3}\overline{V}_{n3} \tag{6.2-10a}$$

$$-(g_{ds3} + g_{m3} + g_{mb3})V_{s3} + (g_{ds2} + g_{ds3})V_{out} = -\overline{V}_{n3} \tag{6.2-10b}$$

Solving for $\overline{V}_{out}/\overline{V}_{n3}$ gives

$$\frac{\overline{V}_{out}}{\overline{V}_{n3}} = \frac{-g_{ds1}g_{m3}}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{ds2}(g_{m3} + g_{mb3})} \cong \frac{-g_{ds1}g_{m3}}{g_{ds2}(g_{m3} + g_{mb3})} \tag{6.2-11}$$

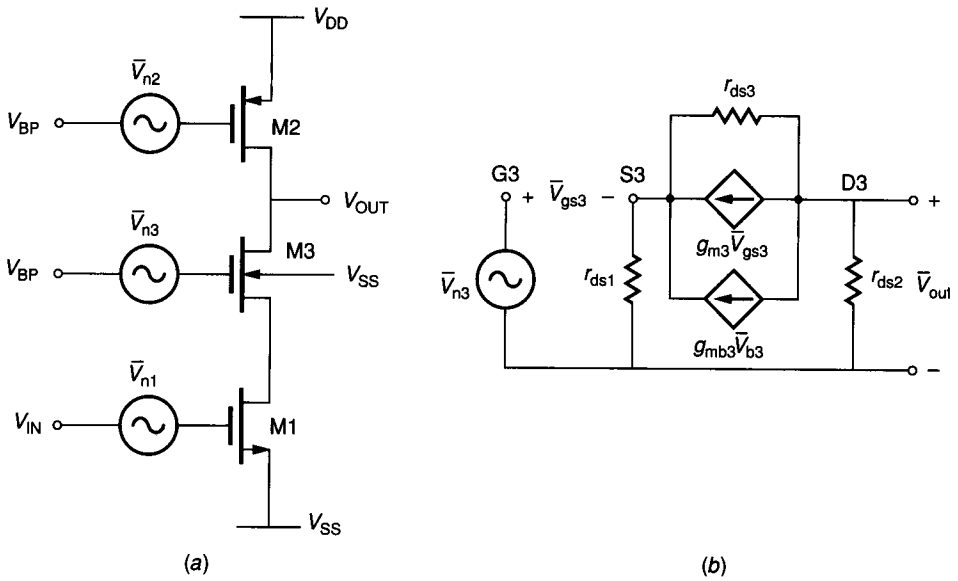


FIGURE 6.2-4
(*a*) Model for calculating the noise performance of the cascode CMOS inverter, (*b*) Model for calculating the noise of M3.

We note that under most normal circumstances, the gain of Eq. 6.2-11 will be less than unity. The reason for this is the large resistance (r_{ds1}) from the source to ground of M3. The total output-noise-voltage spectral density can be found as

$$S_{out} \approx \left(\frac{g_{m1}}{g_{ds2}}\right)^2 S_{VN1} + \left(\frac{g_{m2}}{g_{ds2}}\right)^2 S_{VN2} + S_{VN3} \tag{6.2-12}$$

The equivalent input-noise-voltage spectral density is found by dividing Eq. 6.2-12 by the square of the small signal, frequency independent voltage gain $(g_{m1}/g_{ds2})^2$ to get

$$S_{eq.} = S_{VN1} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VN2} + \left(\frac{g_{ds2}}{g_{m1}}\right)^2 S_{VN3} \approx S_{VN1} + \left(\frac{g_{m2}}{g_{m1}}\right)^2 S_{VN2} \tag{6.2-13}$$

It is of interest to note that for all practical purposes, the addition of the cascode transistor, M3, does not influence the noise performance.

6.2.3 Improving the Gain of the CMOS Cascode Amplifier

The second performance limitation that was found particularly in the MOS inverting amplifiers of Fig. 6.1-11 was a small voltage gain. The ac voltage gain of the inverting amplifier was found to be g_m times the output resistance of the amplifier. One can increase g_m or r_{out} to increase the gain. If one could increase

the current in the transconductance transistor but not in the load transistor, then the gain would increase by the square root of this current increase. Consider the cascode CMOS inverter illustrated in Fig. 6.2-5*a* where a dc current source of value I_o has been connected between V_{DD} and the drain of M1. Because of the low resistance at the point where the current source is attached between M1 and M3, the small signal voltage gain is still given by Eq. 6.2-9. The injection of I_o will increase only g_{m1}, as shown below.

$$A_v \approx \frac{-g_{m1}}{g_{ds2}} = \left(\frac{2K'_N W_1 I_{D1}}{L_1 I_{D2} \lambda_{P2}}\right)^{0.5} = \left(\frac{2K'_N W_1}{L_1 I_{D2} \lambda_{P2}}\right)^{0.5} \left(1 + \frac{I_o}{I_{D2}}\right)^{0.5} \tag{6.2-14}$$

The first product in the rightmost part of Eq. 6.2-14 is the normal gain of the cascode CMOS inverter. The second product in the rightmost part of Eq. 6.2-14 is the amount by which the gain is increased by the injection of the dc current I_o. If the value of I_o is 15 times I_{D2}, the gain enhancement is 4. Unfortunately, the square root factor restricts this method to small gain increases.

Fig. 6.2-5*b* shows a method of reducing the gain of the cascode CMOS inverter. It may seem strange to reduce the gain, but many times the gain needs to be reduced. In this case, Eq. 6.2-14 is written as

$$A_v \approx \frac{g_{m1}}{g_{ds2}} = \left[\frac{2K'_N W_1 I_{D1}}{L_1 I_{D2} \lambda_{P2}}\right]^{0.5} = \left[\frac{2K'_N W_1}{L_1 I_{D2} \lambda_{P2}}\right]^{0.5} \left[1 - \frac{I_o}{I_{D2}}\right]^{0.5} \tag{6.2-15}$$

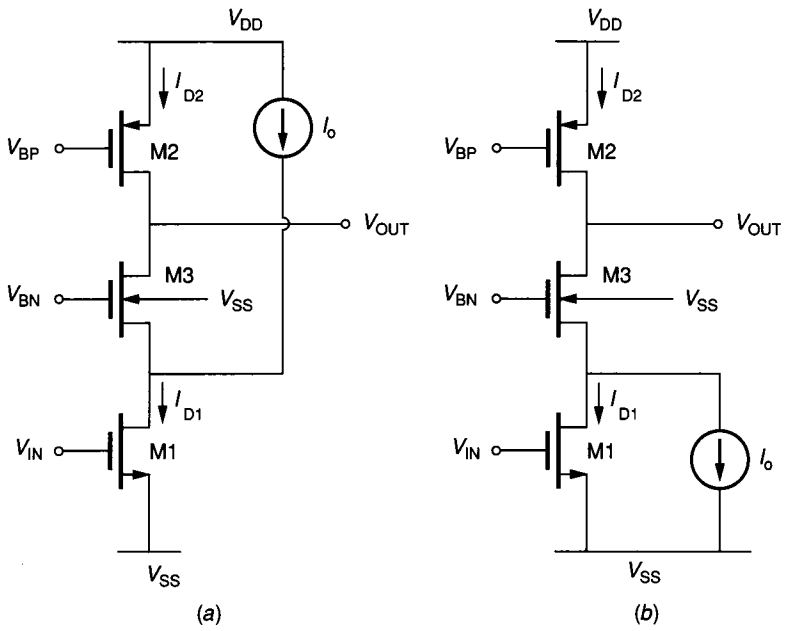


FIGURE 6.2-5
Modification of the ac gain by changing g_{m1}: (*a*) Gain enhancement, (*b*) Gain reduction.

We note that I_o cannot be larger than I_{D2}. The dc current control methods proposed in Fig. 6.2-5 for adjusting the dc gain of the CMOS inverter work primarily because of the low resistance seen at the source of M3.

The addition of a fourth transistor to achieve the cascode CMOS inverter of Fig. 6.2-6 is probably the best method of significantly increasing the ac gain of the CMOS current-source-load inverter. The effect of M4 is to cascode the current source M2 and to boost its output resistance seen by M1 and M3 by roughly a factor of $g_{m4}r_{ds4}$. This causes the output resistance of the inverter to increase the gain. An easy way to calculate the ac gain is to take advantage of previous work. The output resistance of the circuit of Fig. 6.2-6 can be calculated using the result of Eq. 5.3-10. This resistance is the parallel combination of two cascoded current sinks/sources and is expressed as

$$r_{out} = \frac{1}{(g_{ds1}g_{ds3})/(g_{ds1}+g_{ds3}+g_{m3}+g_{mb3})+(g_{ds2}g_{ds4})/(g_{ds2}+g_{ds4}+g_{m4}+g_{mb4})}$$

$$\approx \frac{1}{(g_{ds1}g_{ds3}/g_{m3})+(g_{ds2}g_{ds4}/g_{m4})} \qquad (6.2\text{-}16)$$

Multiplying r_{out} by $-g_{m1}$ gives the ac small signal voltage gain of the circuit of Fig. 6.2-6 as

$$A_v \approx \frac{-g_{m1}g_{m3}g_{m4}}{g_{ds1}g_{m4}g_{ds3}+g_{ds2}g_{m3}g_{ds4}} \qquad (6.2\text{-}17)$$

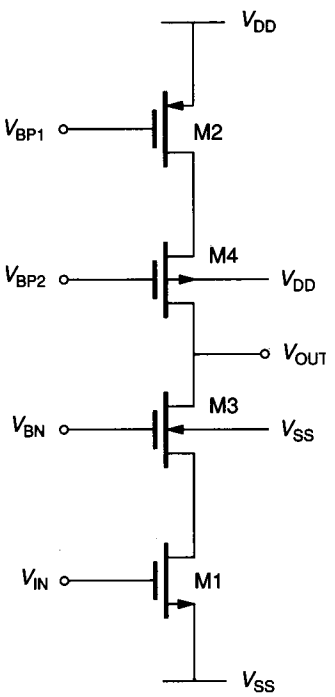


FIGURE 6.2-6
Fully cascoded current-sinking inverter.

It can be seen by comparing Eq. 6.1-50 with Eq. 6.2-17 that the ac voltage gain of the current-source-load inverter has been increased by a factor of approximately $g_m r_o/2$ assuming $g_{m3} \approx g_{m4}$ in Eq. 6.2-17. An example will illustrate some of the preceding concepts.

Example 6.2-1. Improving the performance of a CMOS inverting amplifier. Repeat Example 6.1-2 for the circuit of Fig. 6.2-6 with the following changes. Let all W/L ratios be 10 μ/10 μ and let $V_{BP1} = 3$ V, $V_{BP2} = 1$ V, and $V_{BN} = -1$ V. Assume that the values of capacitances still hold, although the widths of the transistors have changed.

Solution. The current can be found from knowing the voltages across M2. Ignore the drain voltage for the moment. The current is

$$I_{d2} \approx \frac{8}{2}(2 - 0.75)^2 = 6.25\ \mu\text{A}$$

Ignoring the bulk effects on M4 and equating drain currents, it follows that $V_{GS4} = V_{GS2}$. Therefore, the source of M4 or drain of M2 is at 3 V. Using the fact that $V_{sd2} = 2$ V allows the recalculation of I_{d2} including the channel modulation as

$$I_{d2} = 6.25\ \mu\text{A}[1 + (0.02)(2)] = 6.625\ \mu\text{A}$$

Assuming that $V_{sb4} \approx 2$ V gives V_{T4}:

$$V_{T4} \approx 0.75 + 0.4[(2.6) - 0.6]^{0.5} = 1.085\ \text{V}$$

This value of V_{T4} gives $V_{gs4} = 2.372$ V or $V_{sd2} \approx 1.628$ V. We could iterate toward a closer solution, but these results are sufficient. Assuming that the dc value of the output is at 0 V, both M2 and M4 are in saturation.

The dc value of V_{IN} can be found assuming $I_{d1} = 6.625\ \mu$A, to get

$$V_{gs1} = 0.75 + \left[\frac{2(6.625)}{24}\right]^{0.5} = 1.493\ \text{V}$$

Therefore, the quiescent value of V_{in} is -3.507 V. Ignoring the bulk effect on M3 gives $V_{gs3} = V_{gs1} = 1.493$ V so that $V_{d1} = V_{s3} \approx -2.493$ V. Using this value to calculate the threshold voltage of M3 including bulk effects gives

$$V_{T3} \approx 0.75 + 0.8(3.093 - 0.6)^{0.5} = 1.537\ \text{V}$$

This value of V_{T3} gives $V_{gs3} = 2.280$ V. Subtracting this value from -1 V gives $V_{d1} = -3.280$ V or $V_{ds1} = 1.720$ V. We see that both M1 and M3 are also in saturation. As above, we could continue to iterate, but these values are sufficient for this example.

The small signal parameters are found from Table 3.1-3 as

$$g_{m1} = g_{m3} = [2(24)(6.626)]^{0.5}\ \mu\text{S} = 17.83\ \mu\text{S}$$

$$g_{ds1} = g_{ds3} = 0.0663\ \mu\text{S}$$

$$g_{mb3} = \frac{0.8(17.83\ \mu\text{S})}{2(1.720 + 0.6)^{0.5}} = 4.683\ \mu\text{S}$$

$$g_{m2} = g_{m4} = [2(8)(6.626)]^{0.5}\ \mu\text{S} = 10.3\ \mu\text{S}$$

$$g_{ds2} = g_{ds4} = 0.1325\ \mu\text{S}$$

and

$$g_{mb4} = \frac{0.4(10.3\ \mu S)}{2(1.628 + 0.6)^{0.5}} = 1.380\ \mu S$$

Putting these values in Eq. 6.2-15 yields an output resistance of 601 MΩ. Multiplying by $-g_{m1}$ gives an ac voltage gain of −10,716. This gain has been increased over that of Example 6.1-2 for two reasons. The first is the addition of M3 and M4, and the second is the fact that the current is approximately one-half that of the previous example.

Assuming that the dominant pole is the one associated with the output, the −3 dB bandwidth can be found as

$$\omega_{-3dB} = \frac{1}{601\ M\Omega(C_{GD3} + C_{DB3} + C_{GD4} + C_{DB4})} =$$

$$\frac{1}{601\ M\Omega(4.73 + 30.93 + 2.1 + 16.04)pF} = 30.93 \text{ rps or } 4.92 KHz$$

This extremely low bandwidth is a consequence of the high output resistance. The noise-voltage spectral density of the inverter in Fig. 6.2-6 can be found as

$$S_{eq.} \approx \left(100\ nV/\sqrt{Hz}\right)[1 + (10.31/17.83)2]^{0.5} = 115.5\ nV/\sqrt{Hz}$$

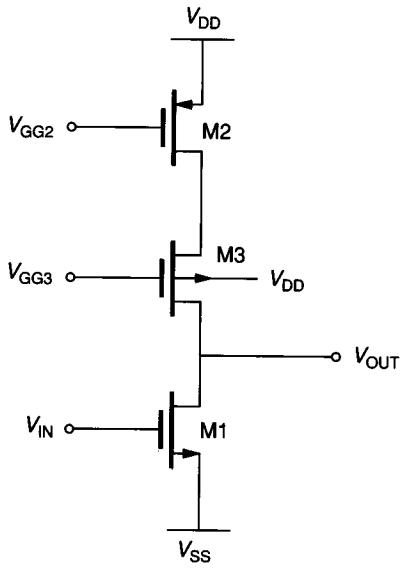
The noise performance is seen to be essentially identical to that of the CMOS inverting amplifier of Example 6.1-2.

One of the purposes of this section is to expand the degrees of design freedom for the inverting voltage amplifier. Example 6.1-5 of the preceding section depicted a case where not all of the design specifications could be met. It is appropriate to reconsider this example to show how the ideas of this section permit the specifications of Example 6.1-5 to be satisfied. The following example gives the details.

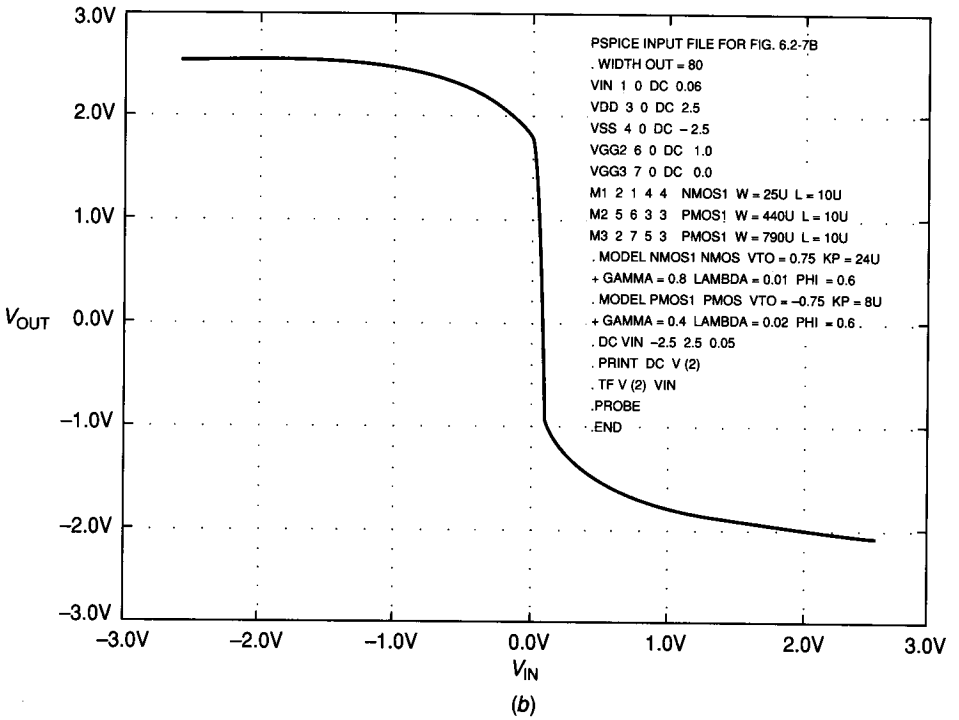
Example 6.2-2. The objective of this example is to show how to meet all of the specifications of Example 6.1-5 using the information introduced in this section. Recall that the design was to achieve a small signal voltage gain greater than −100 using ±2.5 V power supplies and a dissipation less than 1 mW. The amplifier is also to be designed so that the dc value of input and output is 0 V.

Solutions. It was seen in Example 6.1-5 that MOS devices had to be used in order to allow a 2.5 V drop on the input device between the gate (base) and source (emitter). Unfortunately, the dc voltages defined the *W/L* ratios, resulting in a voltage gain of −73.

We will again choose MOS devices for the same reason. If we insert cascode devices in the design of Example 6.1-5, two problems will result. The first is that very little output voltage swing is possible if all transistors are to be kept in saturation. The second is that the gain will be much larger than −100. A better compromise is shown in Fig. 6.2-7*a*. A single n-channel transistor serves as the voltage-controlled current sink (M1) which is the input device and a cascoded current source (M2 and M3) is the load. It is important for the reader to understand the motivation for this choice. If we assume the same dc current level as in Example



(*a*)



(*b*)

FIGURE 6.2-7
(*a*) Circuit for Example 6.2-2, (*b*) Simulation results.

6.1-5, then an inverter such as that of Fig. 6.1-11*b* would have a gain of $-g_{m1}/(g_{ds1} + g_{ds2})$, which for 100 μA of bias current gives

$$A_v \approx \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \frac{-109.5\ \mu S}{1\ \mu S + 2\ \mu S} = -36.5$$

Because we are not using the push-pull configuration, the gain is one-half of -73. Next, we note that if we can use a cascode (M3) in the load, then the effective g_{ds2} in this expression becomes much less than g_{ds1}. Thus, the ac gain will be approximately -109.5, which exceeds the -100 gain specification. Note that this would not have worked if the input device (M1) were p-channel and the load devices (M2 and M3) were n-channel. Because the gate voltage of M2 is under our control (not required to be 0 V), we can carefully design the dc voltages associated with M2 and M3 to provide as much signal swing as possible and still keep these devices in saturation.

Although we are not yet really concerned with signal swing, let us attempt to bias M2 and M3 to achieve a good result. We begin by picking the voltage across the source-drain of M2 as 1 V. The gate voltage is selected to keep M2 in saturation using the following relationship.

$$V_{SD2} > V_{SG2} - |V_{TP}| \rightarrow V_{SG2} < V_{SD2} + |V_{TP}| = 1.75\ \text{V}$$

If we pick V_{GG2} as 1 V, V_{sg2} is 1.5 V, which satisfies the constraint. Assuming the dc current is 100 μA gives W_2/L_2 as

$$\frac{W_2}{L_2} = \frac{2I_D}{K_P'(V_{sg2} - |V_{TP}|)^2(1 + \lambda_P V_{ds2})} = \frac{2(100)}{8(0.75)^2(1.02)} = 43.6 \approx \frac{44}{1}$$

The large value of W/L is due to the choices of dc voltages.

With $V_{bs3} = -2.5$ V, we calculate $|V_{T3}|$ as 1.144 V due to bulk effects. For M3 to remain in saturation, $V_{SG3} < V_{SD3} + |V_{T3}|$ or $V_{DG3} < |V_{T3}|$. Therefore, selecting $V_{GG3} = 0$ V gives a maximum positive output voltage of $|V_{T3}|$ or 1.144 V. This could be increased by increasing V_{GG3}, however with $V_{GG3} = 0$ V no additional bias supply is required. The negative swing can be found by noting that

$$V_{DS1} > V_{GS1} - V_{TN} = 1.75\ \text{V}$$

Therefore, the negative swing is limited to 0.75 V. The value of W_3/L_3 is found from

$$\frac{W_3}{L_3} = \frac{2I_D}{K_P'(V_{sg3} - |V_{T3}|)^2(1 + \lambda_P V_{DS3})} = \frac{2(100)}{8(1.50 - 0.946)^2(1.03)} = 79.11 \approx \frac{79}{1}$$

Again, this large value of W/L is due to the small dc voltage drop associated with M3. If $V_{GG3} > 0$ V, then W_3/L_3 would be even larger, but the positive signal swing would be increased. Since the output signal swing was not a specification, we will leave the design as it is. With the given values, the ac resistance of M2 and M3 seen by M1 is approximately 89 MΩ. The ac gain turns out to be approximately -108, which meets the specification of Example 6.1-5. Figure 6.2-7*b* shows the simulation results of this example. The simulation output file shows that the ac gain is -112.5 and the power dissipation is 0.5 mW. The positive output voltage swing is higher than anticipated because the gain is not influenced significantly when M3 is in the triode region. The value of the output is not 0 V when $V_{in} = 0$ V because the gain is too high and the W/L values have not been precisely chosen. It is not worthwhile

to go back and make this adjustment because the values of the model parameters are not that well known. The best approach is to get as close as possible (as illustrated) and assume that external negative feedback will be used to achieve the desired voltage levels.

6.2.4 The BJT Cascode Amplifier

The principles of increasing the performance of MOS inverting amplifiers covered in this section can also be applied to BJT inverting amplifiers. In the case of the BJT, it is not so important to increase the gain. Therefore, we will focus on the control of the frequency performance of the BJT inverting amplifier. Figure 6.2-8 shows the use of a cascode BJT (Q3) to reduce the Miller effect of the capacitance $C_{\mu 1}$ of Q1 when the amplifier is driven by a high-resistance source (current driver). The circuit of Fig. 6.2-9*a* shows the small signal model of Fig. 6.2-8. We assume initially that the input to the circuit is a current source I_{in}. Figure 6.2-9*b* shows the circuit after rearranging the $g_{m3}V_2$ transconductance source. If we assume that r_{o3} can be ignored, then Fig. 6.2-9*c* results. This simplified small signal model allows us to take advantage of the previous results. The previous development for the MOS version can be used for the BJT. The equations equivalent to Eqs. 6.2-3 through 6.2-5 for the BJT are

$$p_1(\text{cascode}) = -\left[\frac{C_2 + C_3}{g_2} + \frac{C_1 + C_3}{g_1} + \frac{g_{m1}C_3}{g_1 g_2}\right]^{-1} \approx \frac{-g_1}{C_1 + C_3[1 + (g_{m1}/g'_{m3})]} = \frac{-g_{\pi 1}}{C_{\pi 1} + C_{\mu 1}[1 + (g_{m1}/g_{m3})]} \tag{6.2-18}$$

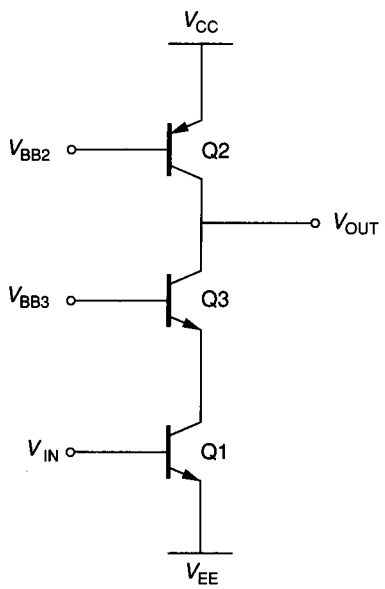


FIGURE 6.2-8
BJT cascoded inverting amplifier.

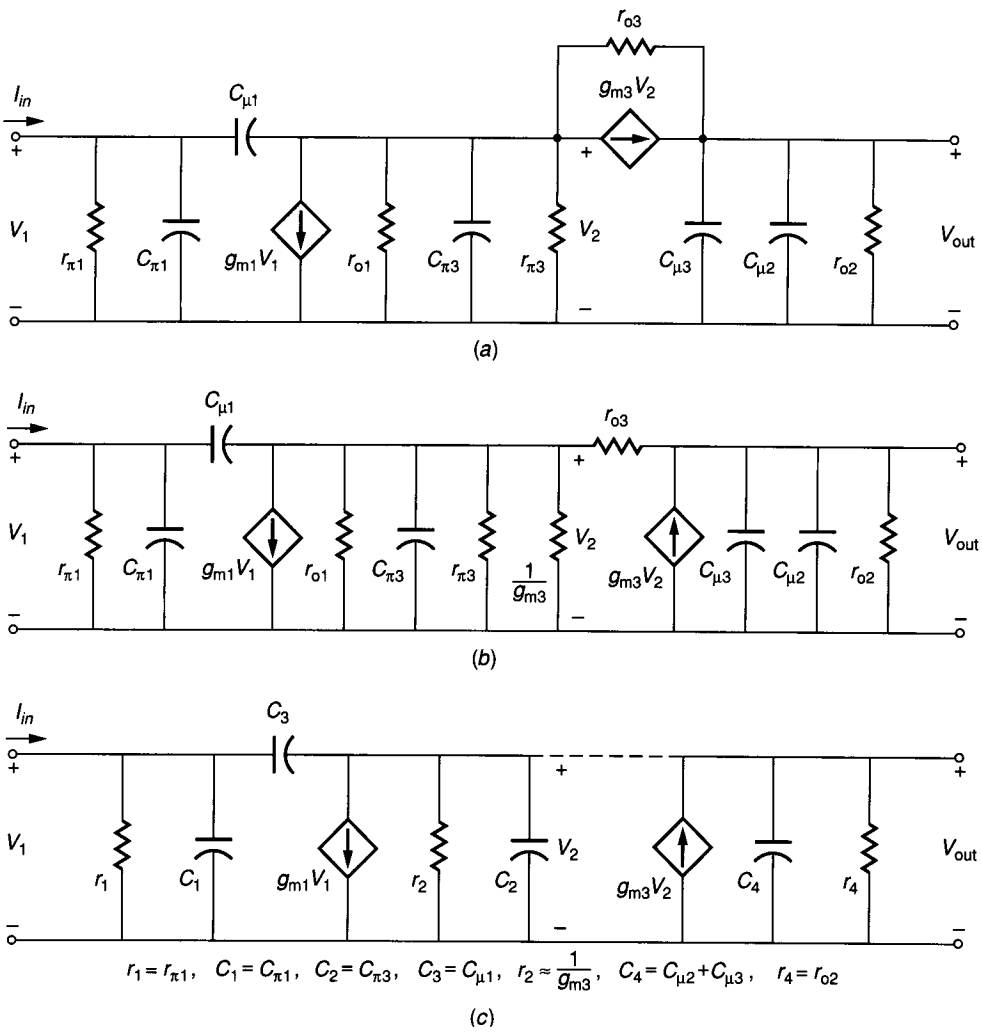


FIGURE 6.2-9
(*a*) Small signal model for Fig. 6.1-8, (*b*) Equivalent model, (*c*) Simplified model.

$$p_2(\text{cascode}) \approx \frac{-g_{m3}[C_1 + C_3 + C_3(g_{m1}/g_{m3})]}{C_1C_2 + C_1C_3 + C_2C_3} =$$

$$\frac{-g_{m3}[C_{\pi 1} + C_{\mu 1} + C_{\mu 1}(g_{m1}/g_{m3})]}{C_{\pi 1}C_{\pi 3} + C_{\pi 1}C_{\mu 1} + C_{\pi 3}C_{\mu 1}} \qquad (6.2\text{-}19)$$

The output pole associated with C_4 is

$$p_3(\text{cascode}) \approx \frac{-g_4}{C_4} = \frac{-g_{o2}}{C_{\mu 2} + C_{\mu 3}} \qquad (6.2\text{-}20)$$

Normally, C_π is greater than C_μ, so the results simplify to

$$p_1(\text{cascode}) \approx \frac{-g_{\pi 1}}{C_{\pi 1}} \tag{6.2-21}$$

and

$$p_2(\text{cascode}) \approx \frac{-g_{m3}}{C_{\pi 3}} \tag{6.3-22}$$

From Eqs. 6.2-20 through 6.2-22, we see that

$$p_3(\text{cascode}) < p_1(\text{cascode}) < p_2(\text{cascode}) \tag{6.2-23}$$

The result is similar to the MOS cascode amplifier. The dominant pole has now been shifted to the output of the amplifier. Note that the p_1 pole of the BJT cascode amplifier is not as sensitive to the source resistance as was the MOS cascode amplifier because of the presence of $r_{\pi 1}$.

The low-frequency gain of the voltage-driven cascode BJT amplifier can also be found from Fig. 6.2-3 using the proper substitutions for the elements, which are obtained by comparing Fig. 6.2-3*a* with Fig. 6.2-9*a*:

$$\frac{V_{\text{out (o)}}}{V_{\text{in (o)}}} = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{v_{\text{out}}}{v_1} = \frac{-g_{m1}(g_{m3} + g_{o3})}{g_{o1}g_{o2} + g_{o1}g_{o3} + g_{o2}g_{o3} + g_{o2}g_{m3}} \approx \frac{-g_{m1}}{g_{o2}} \tag{6.2-24}$$

Comparing this result with Eq. 6.1-71 shows that the influence of the output conductance of Q1 has been eliminated from the voltage gain. Therefore, by comparing Eq. 6.1-71 with Eq. 6.2-24 it follows that the small signal voltage gain of the cascode BJT inverting amplifier should be greater than the gain of a BJT current sink inverting amplifier of Fig. 6.1-8 by approximately a factor of 2 if $|V_{\text{AFN}}| \approx |V_{\text{AFP}}|$. The output resistance is found by the reciprocal sum of the output conductances of Q3 and Q1. From Eqs. 5.3-3 and 5.3-9, the output resistance of Fig. 6.2-8 is

$$r_{\text{out}} = r_{o2} \| r_{o3}[1 + (g_{m3} + g_{o3})(r_{\pi 3} \| r_{o1})] \approx r_{o2} = \frac{I_1}{V_{\text{AFP}}} \tag{6.2-25}$$

Comparing Fig. 6.2-9*c* with Fig. 6.2-3*c* and assuming that the dominant pole is equal to p_3(cascode), then Eq. 6.2-5 gives the -3 dB bandwidth as

$$\omega_{-3\text{dB}} \approx \frac{g_4}{C_4} = \frac{g_{o2}}{C_{\mu 2} + C_{\mu 3}} \tag{6.2-26}$$

Any capacitance at the output of the BJT cascode inverting amplifier must be added to C_4 in Eq. 6.2-26. The noise performance of the BJT cascode inverting amplifier is characterized by the previous analysis for the CMOS cascode inverter amplifier. It can be shown that Eqs. 6.2-12 and 6.2-13 also hold for the BJT cascode inverting amplifier of Fig. 6.2-8.

Example 6.2-3. Repeat Example 6.1-4 for the BJT cascode inverting amplifier of Fig. 6.2-8. Assume that V_{BB3} is -2 V.

Solutions. Using the results of Example 6.1-4, the current in all transistors is seen to be approximately 1.53 mA. Using the values calculated in Example 6.1-4 gives the small signal voltage gain as

$$A_v \approx \frac{-g_{m1}}{g_{o2}} = -\frac{0.059 \text{ S}}{30.7}\ \mu\text{S} = -1928$$

The gain is not increased much due to the fact that g_{o2} is approximately four times g_{o1}. The input resistance is still 1659 Ω and the output resistance is 13 MΩ$\|$32.57 kΩ = 32.49 kΩ. The three poles of the current-driven amplifier are given from Eq. 6.2-20:

$$p_3(\text{cascode}) = 91.06 \text{ Mrps or } 14.5 \text{ MHz}$$

from Eq. 6.2-21:

$$p_1(\text{cascode}) \approx 23.98 \text{ Mrps} = 3.817 \text{ MHz}$$

and from Eq. 6.2-22:

$$p_2(\text{cascode}) \approx 2398 \text{ Mrps} = 381 \text{ MHz}$$

We see that the inequalities of Eq. 6.2-23 are not satisfied in this case. The low output resistance and the high value of C_π compared with C_μ has caused p_1(cascode) to determine the bandwidth. If we assume a 10 pF load at the output, then p_3(cascode) becomes 2.977 Mrps or 0.474 MHz and p_3(cascode) determines the bandwidth. If the poles are closely grouped, then an approximation to the -3 dB bandwidth is given as

$$\omega_{-3\text{dB}} \approx [p_1^2 + p_2^2 + p_3^2]^{1/2}$$

It can be seen that the noise is the same as for Example 6.1-4 if we make the assumption that the contribution of Q3 is negligible. One of the largest differences between this example and Example 6.1-4 is that the -3dB bandwidth of the current-driven cascode is approximately 10 times larger.

One of the reasons for introducing the cascode transistors was to enable a boosting or reduction in gain by current injection or removal from the circuit of Fig. 6.2-8. Because of the high gain available from BJT amplifiers, these techniques are less important and will not be considered. We will complete this section by considering the tremendous gain that can be achieved from the fully cascoded current-sinking inverter of Fig. 6.2-10. This inverter has an output resistance given as

$$r_{\text{out}} = \{r_{o3}[1 + (g_{m3} + g_{o3})(r_{\pi 3}\|r_{o1})]\}\|\{r_{o4}[1 + (g_{m4} + g_{o4})(r_{\pi 4}\|r_{o2})]\}$$

$$\approx r_{o3}(1 + \beta_{FN})\|r_{o4}(1 + \beta_{FP}) = \frac{1}{I_{C3}/[V_{AFN}(1 + \beta_{FN})] + I_{C4}/[V_{AFP}(1 + \beta_{FP})]} \tag{6.2-27}$$

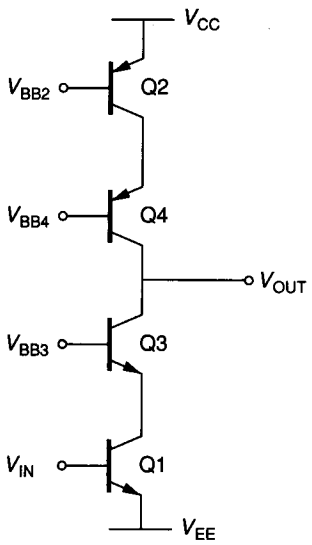


FIGURE 6.2-10
Fully cascoded BJT push-pull inverting amplifier.

The small signal voltage gain of the circuit of Fig. 6.2-10 is given as

$$A_v = -g_{m1}r_{out} = \frac{-I_{C1}/V_t}{I_{C3}/[V_{AFN}(1 + \beta_{BN})] + I_{C4}/[V_{AFP}(1 + \beta_{FP})]} \tag{6.2-28}$$

Normally $I_{C1} = I_{C3} = I_{C4}$ so Eq. 6.2-28 can be written as

$$A_v = -g_{m1}r_{out} = \frac{-1/V_t}{1/[V_{AFN}(1 + \beta_{FN})] + 1/[V_{AFP}(1 + \beta_{FP})]} \tag{6.2-29}$$

Note that the small signal gain of Eq. 6.2-29 is dependent only on the parameters of the BJT models and therefore is the maximum achievable gain given the BJT model parameters. If we assume the values given in Table 6.1-2, the voltage gain of the circuit of Fig. 6.2-10 is −87,420. The reason the gain is so large is that the output resistance is equal to 2.264 MΩ if the dc currents are 1 mA. This high output resistance also causes a low bandwidth. If $C_{\mu 3} = C_{\mu 4} = 0.2$ pF, the −3 dB bandwidth is 1.104 Mrps or 175 kHz if the output resistance is 2.264 MΩ. Typically, the capacitance at the output is more on the order of 10 pF (an oscilloscope probe is typically 14 pF). This causes the −3 dB bandwidth to be 6.81 kHz.

It has been shown how the use of additional devices can improve the small signal performance of the inverting amplifiers covered in Sec. 6.1. The bandwidth is extended in the case of the current-driven inverter. In addition, the gain is increased by two means. The first is the injection of dc current into the transistor acting as a voltage-controlled current sink (or source), and the second is the use of the cascode configuration to increase the ac output resistance.

The additional devices also give an extra degree of design freedom. The techniques presented in this section will be useful in improving or modifying the performance of more complex amplifiers containing inverting amplifiers.

6.3 DIFFERENTIAL AMPLIFIERS

The differential amplifier has become a very useful circuit because of its compatibility with integrated circuit technology, in addition to its ability to amplify differential signals. Any two signals can be decomposed into a *difference-mode* signal, V_D, and a *common-mode* signal, V_C. This is illustrated by the following relations, where V_1 and V_2 are two arbitrary input signals.

$$V_1 = \frac{V_D}{2} + V_C \tag{6.3-1}$$

$$V_2 = -\frac{V_D}{2} + V_C \tag{6.3-2}$$

It is easy to see that V_D and V_C are defined as

$$V_D = V_1 - V_2 \tag{6.3-3}$$

and

$$V_C = \frac{V_1 + V_2}{2} \tag{6.3-4}$$

The objective of the differential amplifier is to amplify only the difference between two input signals, regardless of the level of the common-mode signal.

The differential amplifier is characterized by its differential-mode gain and its common-mode gain. The ratio of the differential-mode gain to the common-mode gain is called the *common-mode rejection ratio (CMRR)*. Ideally, the CMRR should be as large as possible. This normally means that the common-mode gain should be as small as possible. Another characteristic of the differential amplifier is the *input common-mode signal range*, which specifies the range of common-mode values over which the differential amplifier continues to sense and amplify the differential-mode signal. Yet another characteristic that affects the performance of the differential amplifier is offset. When the input differential voltage or the input differential current is zero the output of the differential amplifier may not be zero. *Input offset voltage*, V_{OS}, is the magnitude of a voltage source connected between the inputs of a differential amplifier that would make the output equal to zero. Typically, the common-mode input voltage is also given, since the input offset voltage or current may be dependent on its value. V_{OS} should be treated as a random variable. The *input offset current*, I_{OS}, is the difference between two current sources applied to the inputs of the differential amplifier that is required to make the output equal to zero. I_{OS} should also be treated as a random variable. Both V_{OS} and I_{OS} are dependent on temperature in most differential amplifiers.

6.3.1 CMOS Differential Amplifiers

Figure 6.3-1 shows the circuit of a general MOS differential amplifier. The blocks labeled *active load* can consist of any of the circuits previously discussed that will replace resistances. The key aspect of the differential amplifier is the input source-coupled pair, M1 and M2.

We will first examine the large signal characteristics of the circuit of Fig. 6.3-1. Assume that M1 and M2 are in saturation. Neglecting channel modulation and assuming $V_{T1} = V_{T2}$, it follows that the pertinent relationship describing the large signal behavior is given as

$$V_{ID} = V_{G1} - V_{G2} = V_{GS1} - V_{GS2} = \left[\frac{2I_{D1}}{\beta_1}\right]^{1/2} - \left[\frac{2I_{D2}}{\beta_2}\right]^{1/2} \tag{6.3-5}$$

and

$$I_{SS} = I_{D1} + I_{D2} \tag{6.3-6}$$

where $\beta = K'(W/L)$. Assuming that $\beta_1 = \beta_2 = \beta$, substituting Eq. 6.3-6 into Eq. 6.3-5 and forming a quadratic allows the solution for I_{D1} and I_{D2} as

$$I_{D1} = \frac{I_{SS}}{2} + \frac{I_{SS}}{2}\left[\frac{\beta V_{ID}^2}{I_{SS}} - \frac{\beta^2 V_{ID}^4}{4I_{SS}^2}\right]^{1/2} \tag{6.3-7}$$

and

$$I_{D2} = \frac{I_{SS}}{2} - \frac{I_{SS}}{2}\left[\frac{\beta V_{ID}^2}{I_{SS}} - \frac{\beta^2 V_{ID}^4}{4I_{SS}^2}\right]^{1/2} \tag{6.3-8}$$

These relationships are valid only for

$$|V_{ID}| \leq \left[\frac{2I_{SS}}{\beta}\right]^{1/2} \tag{6.3-9}$$

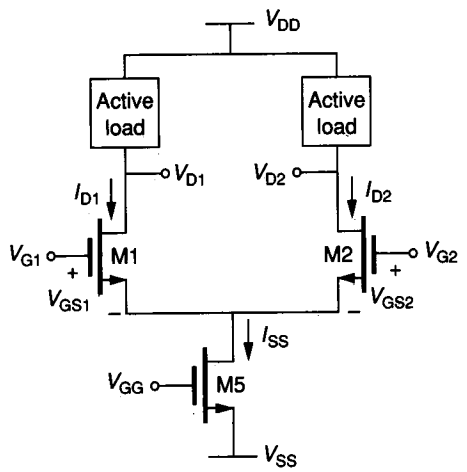


FIGURE 6.3-1
A general MOS differential amplifier configuration. $V_{BS1} = V_{BS2} = 0$.

and for M1 and M2 in saturation. Figure 6.3-2 shows a plot of the normalized drain current of M1 versus the normalized differential input voltage. The large signal voltage transfer characteristics of the differential amplifier can be found by using the results of Eqs. 6.3-7 and 6.3-8 along with the voltage-current characteristics of the active-load devices.

It is of interest to find the regions where M1 and M2 are in saturation. These regions can be found by using the definition in Eq. 6.3-3, rewritten as

$$V_{ID} = V_{G1} - V_{G2} \tag{6.3-10}$$

If we assume symmetry and no common mode excitation, then

$$V_{G1} = \frac{V_{ID}}{2} \tag{6.3-11}$$

and

$$V_{G2} = -\frac{V_{ID}}{2} \tag{6.3-12}$$

Therefore, M1 is in saturation if

$$V_{D1} \geq V_{G1} - V_{TN} = \frac{V_{ID}}{2} - V_{TN} \tag{6.3-13}$$

and M2 is in saturation if

$$V_{D2} \geq -\frac{V_{ID}}{2} - V_{TN} \tag{6.3-14}$$

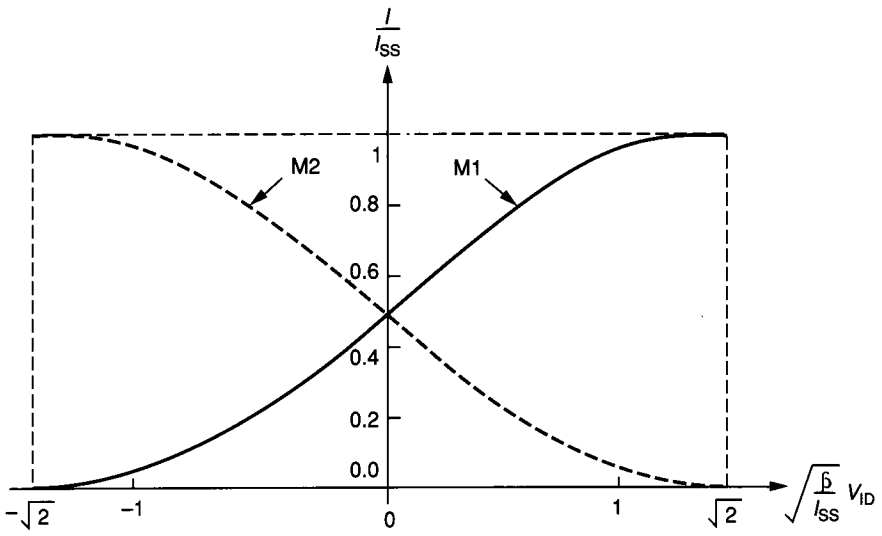


FIGURE 6.3-2
Large signal transconductance characteristic of the MOS differential amplifier.

One way to illustrate these constraints is to plot V_{D1} or V_{D2} as a function of V_{ID}. Assume that the loads of the circuit of Fig. 6.3-1 are resistors of value R_L. Figure 6.3-3 shows a plot of V_{D1} and V_{D2} for an arbitrary value of R_L. Equations 6.3-13 and 6.3-14 are plotted in Fig. 6.3-3 to show the regions where M1 and M2 are saturated. It is seen that the value of R_L will determine how much of the transfer characteristic is in the saturated region. For example, if $I_{SS}R_L \approx V_{DD}$, most of the transfer characteristic of M1 and M2 will be in the saturation region.

It is of interest to find an expression for the large signal transconductance of Fig. 6.3-1. Differentiating Eq. 6.3-7 with respect to V_{ID} and setting the quiescent value of V_{ID} equal to zero gives the differential transconductance of Fig. 6.3-1 as

$$g_m = \left.\frac{\partial I_{D1}}{\partial V_{ID}}\right|_{V_{ID}=0} = \left(\frac{\beta_1 I_{SS}}{4}\right)^{1/2} = \left(\frac{K' I_{SS} W_1}{4L_1}\right)^{1/2} = \left(\frac{K' I_{D1} W_1}{2L_1}\right)^{1/2} \tag{6.3-15}$$

Comparing this result with the expression for g_m of a single transistor (see Table 3.1-3) shows that a difference of 2 exists. The reason for this difference is that only half of the input voltage is applied to M1 or M2 of Fig. 6.3-1, resulting in half the output current. Correspondingly, the transconductance of Eq. 6.3-15 is called the *differential-in, single-ended output transconductance*. The *differential-out transconductance* (g_{md}), can be found by defining a differential output current I_{OD} as

$$I_{OD} = I_{D1} - I_{D2} \tag{6.3-16}$$

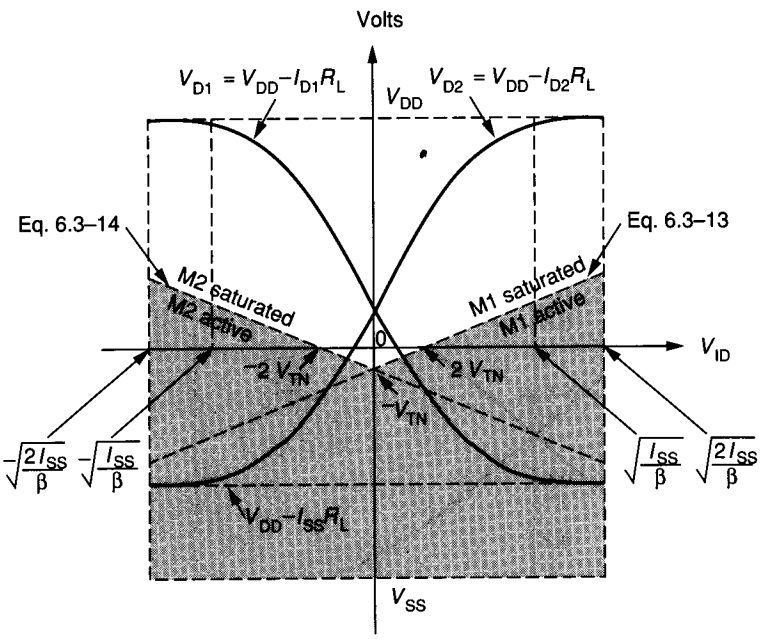


FIGURE 6.3-3
Voltage transfer characteristics of the differential amplifier.

g_{md} can be written as

$$g_{md} = \left.\frac{\partial I_{OD}}{\partial V_{ID}}\right|_{V_{ID}=0} = (\beta_1 I_{SS})^{1/2} = \left(\frac{K' I_{SS} W_1}{L_1}\right)^{1/2} = \left(\frac{2K' I_{D1} W_1}{L_1}\right)^{1/2} \quad (6.3\text{-}17)$$

This transconductance is exactly equal to the transconductance of the common-source transistor if I_D is half of I_{SS}. The presence of I_{SS} in Eqs. 6.3-15 and 6.3-16 illustrates once more the important property that the dc performance is controlled by the dc variables.

The output voltage of the differential amplifier depends on how the active loads of Fig. 6.3-1 are implemented. Assume for the moment that the active loads are replaced by the n-channel enhancement active resistor of Fig. 5.2-2*a*, resulting in the circuit of Fig. 6.3-4*a*. The single-ended output voltages V_{D1} and V_{D2} are given as

$$V_{D1} = V_{DD} - V_{T3} - \left(\frac{2I_{D1}}{\beta_3}\right)^{1/2} \quad (6.3\text{-}18)$$

and

$$V_{D2} = V_{DD} - V_{T4} - \left(\frac{2I_{D2}}{\beta_4}\right)^{1/2} \quad (6.3\text{-}19)$$

where M3 and M4 are saturated. Equations 6.3-7 and 6.3-8 could be substituted into Eqs. 6.3-18 and 6.3-19 to achieve expressions for the drain voltages of M1 and M2 as a function of V_{ID}. These expressions, however, are complex and will be reserved for the problems. Instead, the large signal, differential to single-ended voltage gain will be evaluated at $V_{ID} = 0$ V. Differentiating Eq. 6.3-18 with respect to V_{ID} and multiplying by Eq. 6.3-17 gives

$$A_{vds} = \left(\frac{\partial V_{D1}}{\partial I_{D1}}\right)\left(\left.\frac{\partial I_{D1}}{\partial V_{ID}}\right|_{V_{ID}=0}\right) = -\left(\frac{1}{\beta_3 I_{SS}}\right)^{1/2}\left(\frac{\beta_1 I_{SS}}{4}\right)^{1/2} = -\frac{1}{2}\left(\frac{\beta_1}{\beta_3}\right)^{1/2} \quad (6.3\text{-}20)$$

This gain should be half that of the MOS inverter in Fig. 6.1-11*c* since only half of the input is applied to M1. Comparing Eq. 6.3-20 with Eq. 6.1-34 shows that this relationship holds if the bulk effects, which have been neglected here, are ignored. The differential-in to differential-out voltage gain, A_{vdd}, is equal to the voltage difference between the drains of M1 and M2 divided by V_{ID}. This gain is twice A_{vds} and thus equal to that of an inverter with an enhancement active-load resistor (see Eq. 6.1-33 or 6.1-34).

The ac small signal model of the circuit of Fig. 6.3-4*a* is shown in Fig. 6.3-5*a*. It has been assumed under differential mode excitation that half of v_{id} is applied to the input of each transistor according to the relationship

$$v_{gs1} = -v_{gs2} = \frac{v_{id}}{2} \quad (6.3\text{-}21)$$

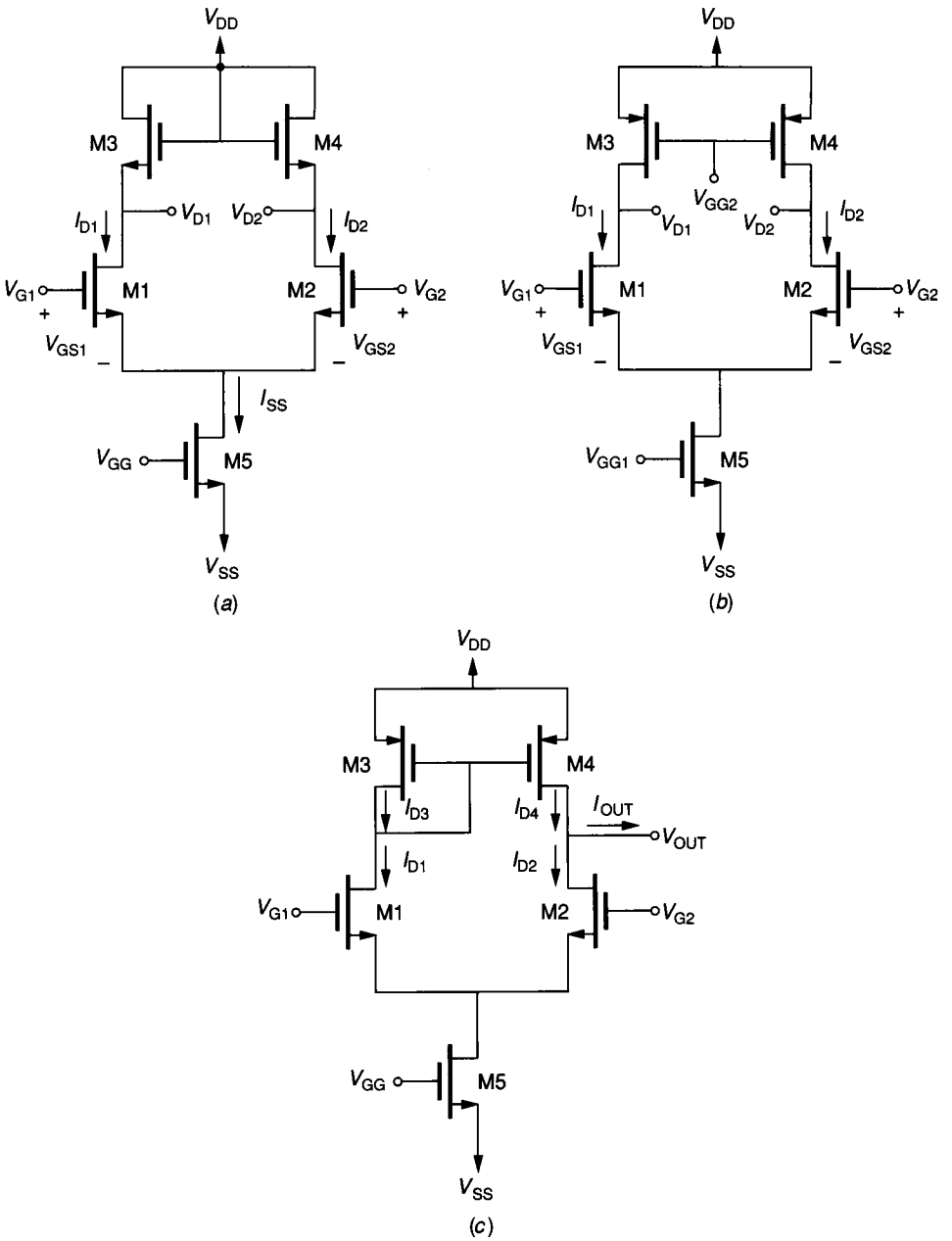


FIGURE 6.3-4
MOS differential amplifiers: (*a*) Enhancement active loads, (*b*) Current source loads, (*c*) Current mirror load.

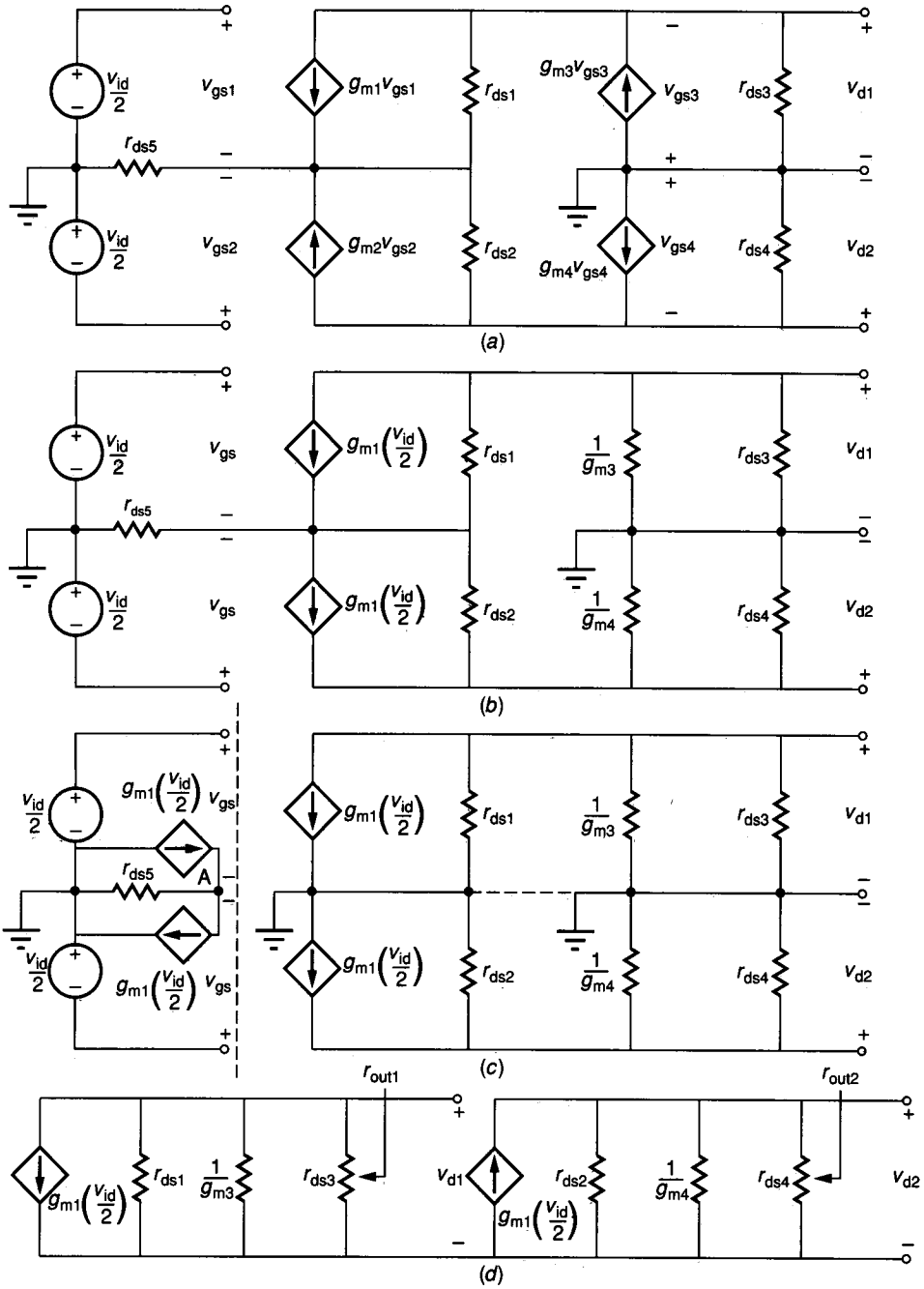


FIGURE 6.3-5
(*a*) Small signal model for differential amplifier of Fig. 6.3-4*a*, (*b*) Use of symmetry to simplify the input circuit, (*c*) Simplification by rerouting the controlled sources $g_{m1}v_{id}/2$, (*d*) Final small signal model.

Figure 6.3-5*a* is simplified in Fig. 6.3-5*b*, where symmetry between M1 and M2 has been assumed, which implies $g_{m1} = g_{m2}$ and $v_{gs1} = -v_{gs2} = v_{gs}$. Also the controlled sources, $g_{m3}v_{gs3}$ and $g_{m4}v_{gs4}$, have been replaced with their equivalent resistances of $1/g_{m3}$ and $1/g_{m4}$, respectively. If the current contributions of r_{ds1} and r_{ds2} to the sources of M1 and M2 and the drain of M5 can be ignored, then the controlled sources, $g_{m1}v_{id}/2$, can be rerouted in the model of Fig. 6.3-5*c* to show that point A is in fact an ac ground. Therefore, all the model to the left of the vertical dotted line can be ignored. The final form of the small signal model is shown in Fig. 6.3-5*d*. The calculations for v_{d1} and v_{d2} are independent of each other and are given as

$$A_{v1} = \frac{v_{d1}}{v_{id}} = \frac{-g_{m1}}{2(g_{m3} + g_{ds1} + g_{ds3})} \approx \frac{-g_{m1}}{2g_{m3}} = \frac{-1}{2}\left[\frac{K'_N(W_1/L_1)}{K'_P(W_3/L_3)}\right]^{1/2} \tag{6.3-22}$$

and

$$A_{v2} = \frac{v_{d2}}{v_{id}} = \frac{g_{m1}}{2(g_{m4} + g_{ds2} + g_{ds4})} \approx \frac{g_{m1}}{2g_{m4}} = \frac{1}{2}\left[\frac{K'_N(W_1/L_1)}{K'_P(W_4/L_4)}\right]^{1/2} \tag{6.3-23}$$

Comparing Eq. 6.3-22 or 6.3-23 with Eq. 6.3-20 shows that the small signal analysis agrees with the large signal analysis. The differential voltage gain is given as

$$A_{vdd} = \frac{v_{od}}{v_{id}} = \frac{v_{d1} - v_{d2}}{v_{id}} = -\frac{g_{m1}}{2g_{m3}} - \frac{g_{m1}}{2g_{m4}} = -\frac{g_{m1}}{g_{m3}} \tag{6.3-24}$$

if M3 and M4 are also matched so that $g_{m3} = g_{m4}$.

The dc differential input resistance, r_{id}, is that resistance seen by the input voltage source, v_{id}. In this case, r_{id} is infinite. The single-ended output resistance comprises those resistances seen looking back into the output terminals of Fig. 6.3-5*d*. These resistances are

$$r_{out1} = \frac{1}{g_{m3} + g_{ds1} + g_{ds3}} \approx \frac{1}{g_{m3}} \tag{6.3-25}$$

and

$$r_{out2} = \frac{1}{g_{m4} + g_{ds2} + g_{ds4}} \approx \frac{1}{g_{m4}} \tag{6.3-26}$$

The differential output resistance, r_{od}, is equal to the ac resistance seen between the drains of M1 and M2 and can be written as

$$r_{od} = r_{out1} + r_{out2} \approx \frac{1}{g_{m3}} + \frac{1}{g_{m4}} \approx \frac{2}{g_{m3}} \tag{6.3-27}$$

It is assumed in the above calculations that all the transistors of the differential amplifier are operating in the saturation region. We shall shortly examine the voltage ranges at the input and output over which this condition holds.

The voltage gain of the differential amplifier considered in Fig. 6.3-4*a* can be increased using current sources as loads. This differential amplifier is shown in Fig. 6.3-4*b*. The previous small signal analysis holds if we let $g_{m3} = g_{m4} = 0$. The small signal performance is summarized as

$$A_{vds1} = A_{v1} = \frac{v_{d1}}{v_{id}} = \frac{-g_{m1}}{2(g_{ds1} + g_{ds3})} \tag{6.3-28}$$

$$A_{vds2} = A_{v2} = \frac{v_{d2}}{v_{id}} = \frac{g_{m1}}{2(g_{ds2} + g_{ds4})} \tag{6.3-29}$$

$$A_{vdd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m1}}{g_{ds1} + g_{ds3}} = \frac{-g_{m2}}{g_{ds2} + g_{ds4}} \tag{6.3-30}$$

$$r_{out1} = \frac{1}{g_{ds1} + g_{ds3}} \tag{6.3-31}$$

$$r_{out2} = \frac{1}{g_{ds2} + g_{ds4}} \tag{6.3-32}$$

and

$$r_{od} \cong \frac{2}{g_{ds1} + g_{ds3}} \tag{6.3-33}$$

It is seen that this differential amplifier has a performance that is identical to the current-source-load sinking inverter of Fig. 6.1-11*b*.

Another configuration of the load for a differential amplifier is shown in Fig. 6.3-4*c*. This method uses a current mirror to form the load devices. The advantage of this configuration is that the differential output signal is converted to a single-ended output signal with no extra components required. In this circuit, the output voltage or current is taken from the drains of M2 and M4. The operation of this circuit is as follows. If a differential voltage, V_{ID}, is applied between the gates as defined in Eq. 6.3-21, then half is applied to the gate-source of M1 and half to the gate-source of M2. The result is to increase I_{D1} and decrease I_{D2} by equal increments, ΔI. The ΔI increase I_{D1} is mirrored through M3-M4 as an increase in I_{D4} of ΔI. As a consequence of the ΔI increase in I_{D4} and the ΔI decrease in I_{D2}, the output must sink a current of $2\Delta I$. Therefore, the transconductance of the circuit of Fig. 6.3-4*c*, I_{out}/V_{id}, is equal to that of a single transistor. This differential amplifier is a very useful circuit and will be used further in analog integrated circuit design.

The small signal analysis of the circuit of Fig. 6.3-4*c* requires a modification of the model of Fig. 6.3-5. The model suitable for small signal analysis of the circuit of Fig. 6.3-4*c* is shown in Fig. 6.3-6. The small signal, differential-in, differential-out voltage gain (A_{vdd}) is

$$\frac{v_{out}}{v_{id}} = A_{vdd} = \frac{1}{2}\left(g_{m1} + \frac{g_{m1}g_{m4}}{g_{ds1} + g_{m3} + g_{ds3}}\right)\left(\frac{1}{g_{ds2} + g_{ds4}}\right) \tag{6.3-34}$$

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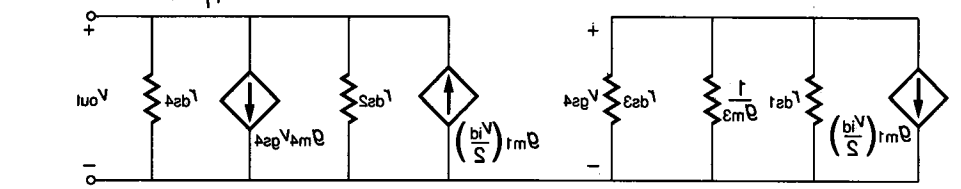


FIGURE 6.3-6
Small signal model for Fig. 6.3-4*c*.

If we assume that M3 and M4 are matched, then $g_{m3} = g_{m4}$, and since g_{m3} is much larger than either g_{ds1} or g_{ds3}, Eq. 6.3-34 can be simplified to

$$A_{vdd} \simeq \frac{g_{m1}}{g_{ds2} + g_{ds4}} \tag{6.3-35}$$

Substituting for the small signal parameters of Eq. 6.3-35 with the relationships specified in Table 3.1-3 gives

$$A_{vdd} = \frac{2(K'I_{SS}W_1/L_1)^{1/2}}{(\lambda_2 + \lambda_4)I_{SS}} = \frac{2}{(\lambda_2 + \lambda_4)}\left(\frac{K'W_1}{I_{SS}L_1}\right)^{1/2} \tag{6.3-36}$$

Again we note the dependence of the small signal performance on $I_{SS}^{-1/2}$ similar to that of the inverter. Assuming that $W_1/L_1 = 1$ and that $I_{SS} = 10\ \mu$A, the small signal, differential-in, differential-out voltage gain of the circuit of Fig. 6.3-4*c* is 103. The differential-in, single-ended out voltage gain is equal to half the value of Eq. 6.3-36, although in the case of Fig. 6.3-4*c* this voltage is not available as it would be for the differential amplifiers of Fig. 6.3-4*a* and *b*. The small signal output resistance is found from Fig. 6.3-6 as

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{SS}} \simeq \frac{1}{\lambda I_{SS}} \tag{6.3-37}$$

Of course, the small signal, low-frequency input resistance of the MOSFET differential amplifier is infinity.

Another important characteristic of the MOS differential amplifier is the input common-mode voltage range, defined earlier. For our purposes, we will assume that the input common-mode range is defined by the input voltage range over which both M1 and M2 remain in saturation. Let us consider the input common-mode voltage range of Fig. 6.3-4*c*. Assume that $V_{G1} = V_{G2}$ and that M1 is on the threshold of saturation when $V_{DG1} = V_{T1}$. We may write V_{DG1} as

$$V_{DG1} = V_{DD} - V_{SD3} - V_{G1} = V_{DD} - V_{SG3} - V_{G1} \tag{6.3-38}$$

or

$$V_{DG1} = V_{DD} - \left(\frac{2I_{D3}}{\beta_3}\right)^{1/2} - |V_{TO3}| - V_{G1} \tag{6.3-39}$$

where V_{TO3} implies that M3 is unaffected by the bulk potential. If V_{DG1} is set equal to $-V_{T1}$, then we can solve for the maximum input voltage, $V_{G1}(\max)$, as

$$V_{G1}(\max) = V_{DD} - \left(\frac{I_{SS}}{\beta_3}\right)^{1/2} - |V_{TO3}| + V_{T1} \tag{6.3-40}$$

As V_{G1} approaches V_{SS}, M1 will be in the saturation region and close to cutoff. Therefore, it makes more sense to relate $V_{G1}(\min)$ to V_{GG} when M5 is no longer in saturation. Solving for the drain-gate voltage of M5 gives

$$V_{DG5} = V_{G1} - V_{GS1} - V_{GG} \tag{6.3-41}$$

Set $V_{DG5} = -V_{TO5}$ to get

$$V_{G1}(\min) \cong V_{GG} + \left(\frac{2I_{SS}}{\beta_1}\right)^{\frac{1}{2}} + V_{TO1} - V_{TO5} \tag{6.3-42}$$

The large signal swing limitations of the output are also of interest. In this case, the swing limitations will be based on keeping both M2 and M4 in saturation. When V_{G1} is taken above V_{G2}, the output voltage, V_{OUT}, increases. The drain-gate voltage of M4 is given as

$$V_{DG4} = V_{DD} - V_{SD3} - V_{OUT} = V_{DD} - V_{SG3} - V_{OUT} \tag{6.3-43}$$

M4 is at the edge of saturation when $V_{DG4} = -|V_{TO4}|$. Using this relationship and the value for V_{SD3} used in Eqs. 6.3-38 and 6.3-39 gives the maximum output voltage as

$$V_{OUT}(\max) = V_{DD} - \left(\frac{I_{SS}}{\beta_3}\right)^{1/2} - |V_{TO3}| + |V_{TO4}| \cong V_{DD} - \left(\frac{2I_{SS}}{\beta_3}\right)^{1/2} \tag{6.3-44}$$

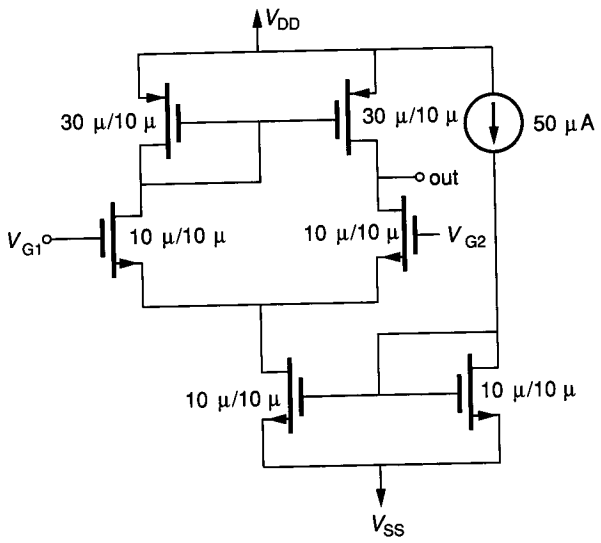
The minimum output voltage is found by determining when M2 is at the edge of saturation. The minimum output voltage for Fig. 6.3-4*c* is

$$V_{OUT}(\min) = V_{G2} - V_{T2} \tag{6.3-45}$$

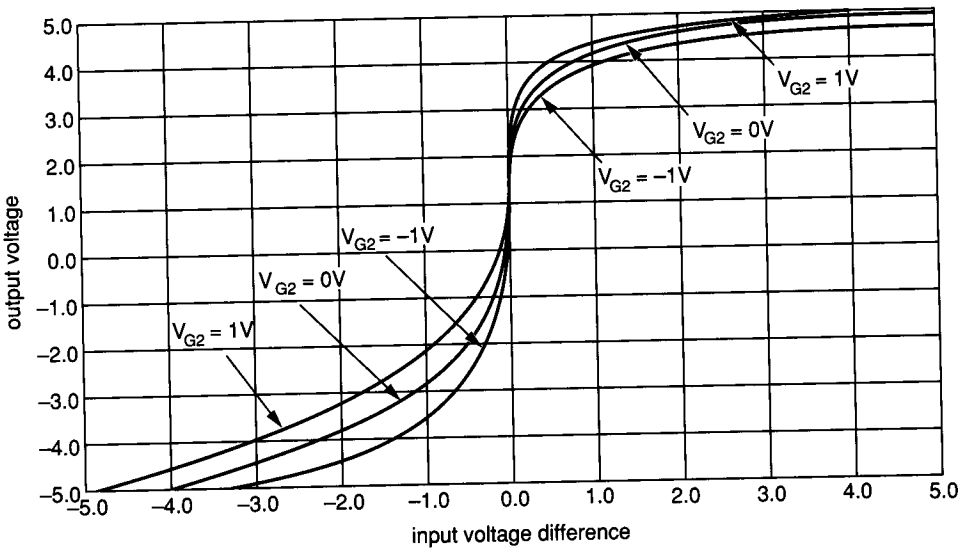
Figure 6.3-7*a* shows a differential amplifier similar to Fig. 6.3-4*c*. The simulated voltage transfer characteristic corresponding to the *W/L* values given in the schematic is shown in Fig. 6.3-7*b*. The influence of V_{G2} upon V_{OUT} (min) is illustrated in this figure. The input and output signal limits of the differential amplifiers in Fig. 6.3-4*a* and *b* can be found in a similar manner.

The small signal common-mode gain of the differential amplifier can be found by connecting both inputs together and applying a single-ended input voltage. The small signal model for the differential amplifier of Fig. 6.3-4*b* is shown in Fig. 6.3-8*a*. If we assume that M1 and M2 are matched, then the model simplifies to that shown in Fig. 6.3-8*b*. To find the common-mode gain, we wish to solve for v_{d2} in terms of v_c. If the current contribution through r_{ds1} and r_{ds2} can be neglected, then the voltage across r_{ds5} can be written as

$$v_s \approx 2g_{m1}r_{ds5}v_c \tag{6.3-46}$$



(*a*)



(*b*)

FIGURE 6.3-7
(*a*) n-channel input differential amplifier, (*b*) Simulation of voltage transfer curve for $V_{G2} = -1$, 0, and 1 V ($V_{DD} = 5$ V, $V_{SS} = -5$ V, $K'_N = 2K'_P = 28$ μA/V, $V_T = \pm 0.7$ V, and $\lambda_N = \lambda_P = 0.01\ V^{-1}$).

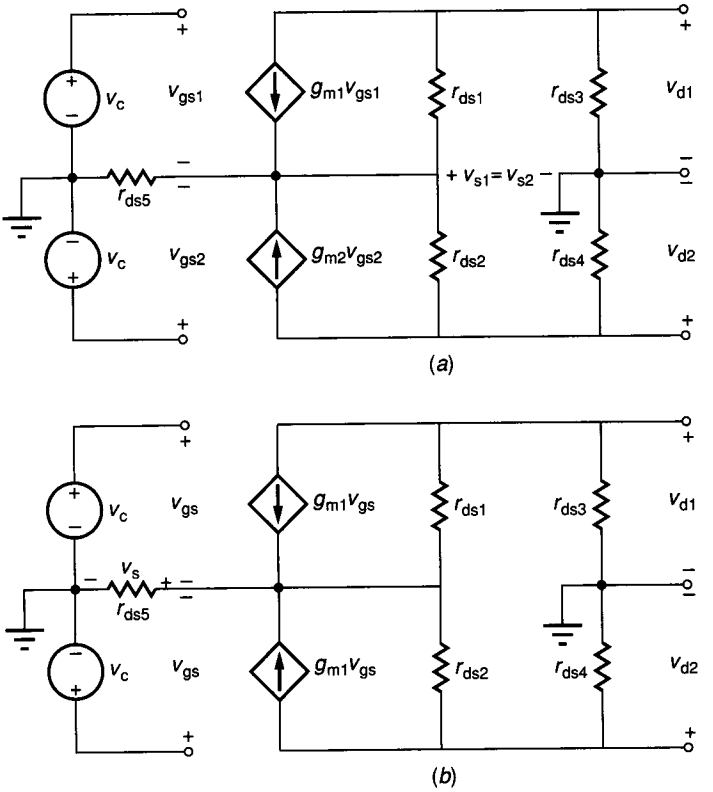


FIGURE 6.3-8
(*a*) Small signal model of Fig. 6.3-4*b* for common mode operation, (*b*) Simplified version of (*a*).

Using the relationship that $v_{gs} = v_g - v_s$, we may write

$$v_{gs} = \frac{1}{1 + 2g_{m1}r_{ds5}} v_c \tag{6.3-47}$$

The voltage, v_{d2}, can be found by the superposition of the two sources, v_{gs}. The problem is considerably simplified if we ignore r_{ds1} and r_{ds2}. Therefore, the voltage gain, v_{d2}/v_c, can be expressed as

$$\frac{v_{d2}}{v_c} = A_{vc} \simeq \frac{-g_{m1}r_{ds3}}{1 + 2g_{m1}r_{ds5}} \tag{6.3-48}$$

The common-mode voltage gain of the circuit of Fig. 6.3-4*a* can be found in a similar manner. However, the preceding method does not work for the differential amplifier of Fig. 6.3-4*c* because there is no point at which the single-ended output is available. In practice, Fig. 6.3-4*c* will exhibit a nonzero common-mode gain because of the fact that M1 and M2, and M3 and M4 are not perfectly matched. The mismatch effect for the differential amplifiers of Fig. 6.3-4*a* and Fig. 6.3-4*b* may dominate the actual common-mode gain.

The common-mode rejection ratio can be found by using the definition given earlier in this section. For the differential amplifier of Fig. 6.3-4*b*, the CMRR is found to be

$$\text{CMRR} = \frac{|A_{vds}|}{|A_{vc}|} = \frac{g_{ds3}(1 + 2g_{m1}r_{ds5})}{g_{ds2} + g_{ds4}} \tag{6.3-49}$$

If $g_{ds2} \simeq g_{ds3} \simeq g_{ds4}$, then the CMRR of Fig. 6.3-4*b* becomes approximately equal to $g_{m1}r_{ds5}$. It is desirable to have the CMRR as large as possible, which suggests that if r_{ds5} or g_{m1} can be increased, the differential amplifier will have a greater ability to reject the common-mode signal in favor of the differential-mode signal.

6.3.2 BJT Differential Amplifiers

The preceding concepts concerning the differential amplifier can also be applied to bipolar technology. Figure 6.3-9 shows a general bipolar differential amplifier configuration similar to that of Fig. 6.3-1 for MOS technology. We will briefly illustrate some of the large signal and small signal properties of the BJT differential amplifier. Under the assumption that Q1 and Q2 are operating in the forward active region and that the Early voltage effects are negligible, it follows from Eqs. 3.3-10 and 3.3-11 that the large signal characteristics can be found from the following relationships:

$$V_{ID} = V_{B1} - V_{B2} = V_{BE1} - V_{BE2} = V_t \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_t \ln\left(\frac{I_{C2}}{I_{S2}}\right) = V_t \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{6.3-50}$$

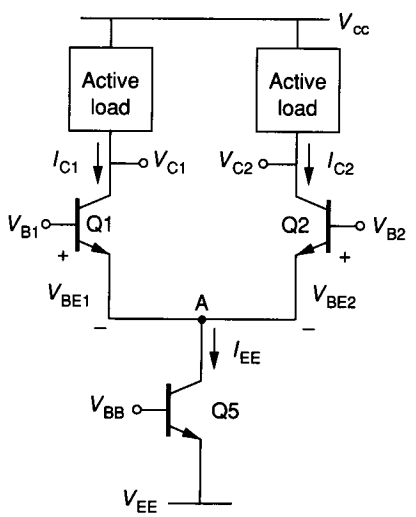


FIGURE 6.3-9
A general configuration for a BJT differential amplifier.

$$I_{EE} = \frac{I_{C1}}{\alpha_F} + \frac{I_{C2}}{\alpha_F} \tag{6.3-51}$$

where we have assumed that Q1 and Q2 are matched ($I_{S1} = I_{S2}$ and $\alpha_{F1} = \alpha_{F2} = \alpha_F$), and $V_t = kT/q$. Solving for I_{C1} and I_{C2} results in the following.

$$I_{C1} = \frac{\alpha_F I_{EE}}{1 + \exp(-V_{ID}/V_t)} \tag{6.3-52}$$

$$I_{C2} = \frac{\alpha_F I_{EE}}{1 + \exp(V_{ID}/V_t)} \tag{6.3-53}$$

From these two equations, it follows as in the MOS case that I_{C1} and I_{C2} are independent of the common mode excitation and the characteristics of the active load. Figure 6.3-10 shows a plot of the normalized collector current of Q1 and Q2 as a function of V_{ID}/V_t. The range of linear operation is seen to be limited to $|V_{ID}| \leq 2V_t$, or approximately ± 50 mV at room temperature.

Differentiating Eq. 6.3-52 gives the differential-in, single-ended transconductance as

$$g_m = -\frac{\alpha_F I_{EE}}{2V_t}\left[\frac{1}{1 + \cosh(V_{ID}/V_t)}\right] \tag{6.3-54}$$

If V_{ID} is set to zero, we obtain

$$g_m(V_{ID} = 0) = \frac{-\alpha_F I_{EE}}{4V_t} \tag{6.3-55}$$

The differential-in, differential-out transconductance (g_{md}) is found by multiplying the expressions given in Eqs. 6.3-54 and 6.3-55 by 2.

The large signal limits for the input and output of the BJT differential amplifier are found in a similar manner as for the MOS differential amplifier. The

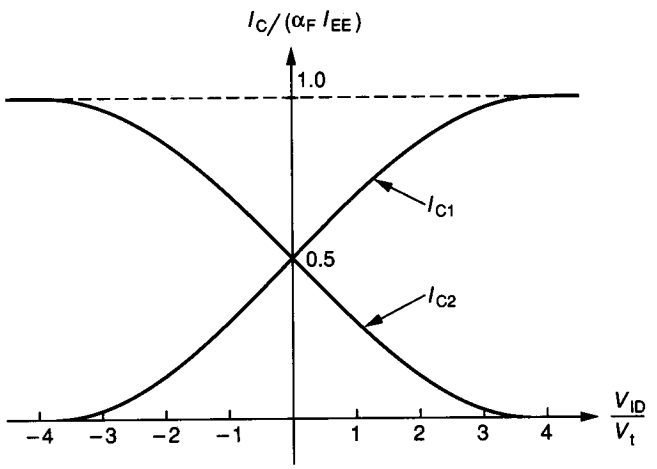


FIGURE 6.3-10
Large signal transconductance characteristics of the BJT differential amplifier.

objective again is to keep the BJT devices in the forward active region of operation, that is, the BE junction forward-biased and the BC junction reverse-biased.

Figure 6.3-11 shows the BJT differential amplifier that is topologically identical to the MOS differential amplifier of Fig. 6.3-4*c*. Assume that $V_{B1} = V_{B2}$. The highest value of V_{B1} is equal to

$$V_{B1}(\max) \simeq V_{CC} - V_{BE3} - V_{CE2}(\text{sat}) + V_{BE2} = V_{CC} - 0.2 \text{ V} \quad (6.3\text{-}56)$$

This relationship was developed under the conditions where Q1 is saturated. The lowest value of V_{B1} is given by

$$V_{B1}(\min) \simeq V_{BE1} + V_{CE5}(\text{sat}) + V_{EE} = V_{EE} + 0.8 \text{ V} \quad (6.3\text{-}57)$$

The output voltage of the circuit of Fig. 6.3-11 is limited to the range between

$$V_O(\max) \simeq V_{CC} - V_{CE4}(\text{sat}) = V_{CC} - 0.2 \text{ V} \quad (6.3\text{-}58)$$

and

$$V_O(\min) \simeq V_{B2} - 0.5\ V \quad (6.3\text{-}59)$$

where V_{B2} is the dc potential connected to the base of Q2.

Figure 6.3-12*a* shows a model suitable for small signal differential input excitation of the circuit of Fig. 6.3-11 neglecting r_μ and the frequency-dependent parameters of the model. If Q1 and Q2 are matched, we can assume that $r_{\pi 1} = r_{\pi 2} = r_\pi$, $g_{m1} = g_{m2}$, and $v_{be1} = -v_{be2}$. Neglecting the contribution of current through r_{o1} and r_{o2} into their common node allows the simplification of the small signal model to that shown in Fig. 6.3-12*b*. Since there is no ac current flowing through r_{o5}, it may be neglected. Also, we have replaced the current source, $g_{m3}v_{be3}$, by a resistor of $1/g_{m3}$ since v_{be3} is the voltage across this source. The final simplified small signal model for the BJT differential amplifier shown in Fig. 6.3-11 is given in Fig. 6.3-12*c*. The differential-out, differential-in voltage gain is

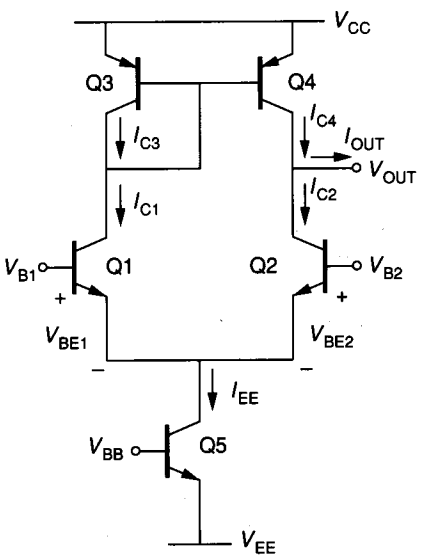


FIGURE 6.3-11
Practical version of the BJT differential amplifier.

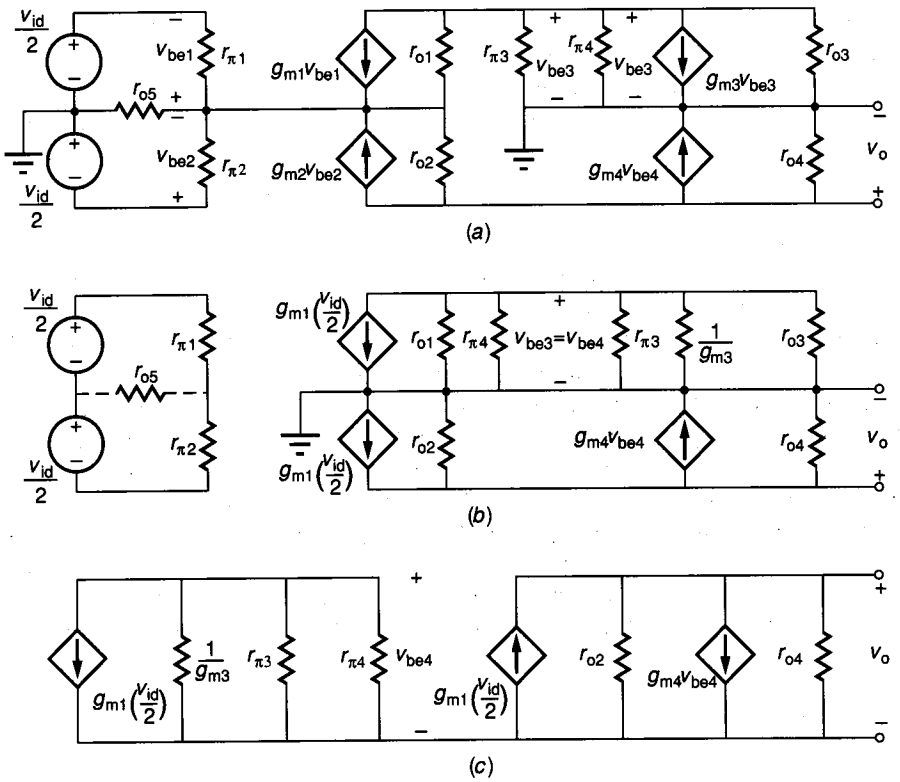


FIGURE 6.3-12
Small signal model for the BJT differential amplifier of Fig. 6.3-11: (*a*) Complete small signal model, (*b*) Simplification of (*a*), (*c*) Final small signal model.

$$\frac{v_o}{v_{id}} = A_{vdd} = \frac{1}{2}\left[g_{m1} + \frac{g_{m1}g_{m4}}{g_{m3} + g_{\pi 3} + g_{\pi 4}}\right]\left[\frac{1}{g_{o2} + g_{o4}}\right] \tag{6.3-60}$$

If we assume that Q3 and Q4 are matched, then $g_{m3} = g_{m4}$, and since g_{m3} is larger than $g_{\pi 3}$ or $g_{\pi 4}$, Eq. 6.3-60 can be simplified to

$$A_{vdd} \simeq \frac{g_{m1}}{g_{o2} + g_{o4}} = \frac{1}{(V_t/V_{AFN}) + (V_t/V_{AFP})} \tag{6.3-61}$$

where V_{AN} and V_{AP} are the Early voltages defined for the npn and pnp bipolar junction transistors. The small signal, differential-in, differential-out voltage gain of Fig. 6.3-11 is seen to be equal in magnitude to the BJT inverter of Sec. 6.1 (see Eq. 6.1-71). The small signal output resistance of the circuit of Fig. 6.3-11 is found as

$$r_{out} = \frac{1}{g_{o2} + g_{o4}} = \frac{1}{(I_{C2}/V_{AFN}) + (I_{C4}/V_{AFP})} = \frac{2V_{AFN}V_{AFP}}{I_{EE}(V_{AFN} + V_{AFP})} \tag{6.3-62}$$

The differential input resistance of the circuit of Fig. 6.3-11 can be expressed as

$$r_{id} = 2r_{\pi 1} = \frac{\beta_F V_t}{I_{C1}} = \frac{2\beta_F V_t}{I_{EE}} \tag{6.3-63}$$

A BJT differential amplifier topologically identical to the MOS differential amplifier of Fig. 6.3-4*b* is shown in the circuit of Fig. 6.3-13. A biasing scheme using Q6, R_{BIAS}, and Q7 is illustrated. It can be shown that the differential-in, single-ended-out voltage gain is given by

$$A_{vds} = \frac{v_{c1}}{v_{id}} = \frac{-g_{m1}r_{o1}r_{o3}}{r_{o1} + r_{o3}} \tag{6.3-64}$$

The common-mode voltage gain of Fig. 6.3-13 can be found by use of the small signal model shown in Fig. 6.3-14*a*. If we assume that Q1 and Q2 are matched and neglect the contribution of currents through r_{o1} and r_{o2}, we obtain the following relationships between v_c and v_{be}.

$$v_{be} = \frac{v_c}{1 + 2(g_{m1} + g_{\pi 1})r_{o5}} \tag{6.3-65}$$

The voltage at the collector of Q1 may be written as

$$v_{c1} \simeq -g_{m1}r_{o3} \tag{6.3-66}$$

where we have neglected r_{o1} and r_{o2}. Combining Eqs. 6.3-65 and 6.3-66 gives the common-mode voltage gain, A_{vc}, for Fig. 6.3-13 as follows.

$$A_{vc} = \frac{-g_{m1}r_{o3}}{1 + 2(g_{m1} + g_{\pi 1})r_{o5}} \simeq \frac{-g_{m1}r_{o3}}{1 + 2g_{m1}r_{o5}} \tag{6.3-67}$$

The common-mode gain for the BJT differential amplifier of Fig. 6.3-11 is theoretically zero because the only output node is differential, similar to Fig. 6.3-4*c*. Mismatch effects will the common-mode gain to be nonzero.

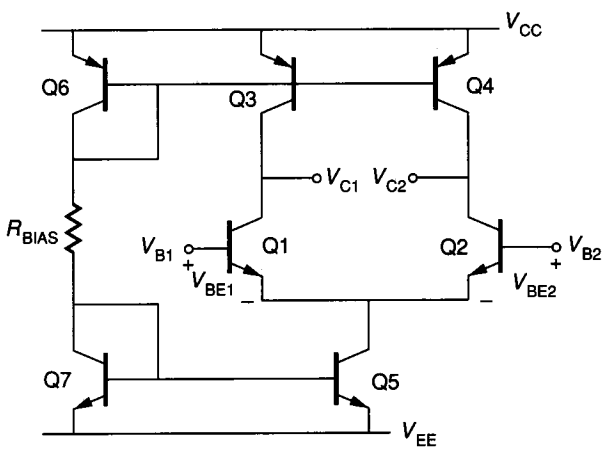


FIGURE 6.3-13
BJT differential amplifier using current-source active loads and illustrating one possible bias method.

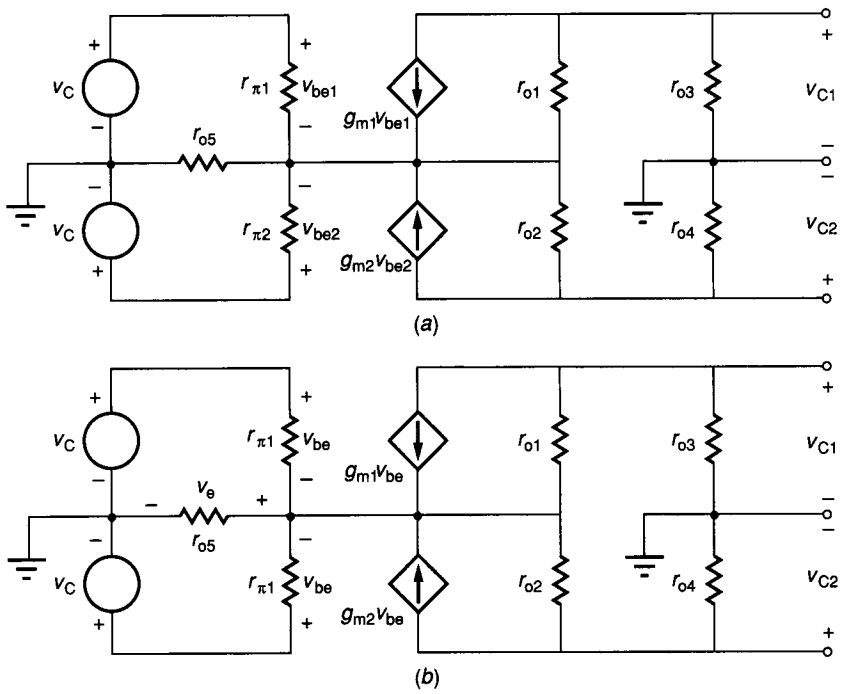


FIGURE 6.3-14
(*a*) Small signal model of Fig. 6.3-13 for common-mode operation, (*b*) Simplified version of (*a*).

The low-frequency CMRR for Fig. 6.3-13 can be found from Eqs. 6.3-64 and 6.3-67 and is expressed as

$$\text{CMRR} = \frac{|A_{vds}|}{|A_{vc}|} \simeq \frac{r_{o1}(1 + g_{m1}r_{o5})}{2(r_{o1} + r_{o3})} \simeq \frac{1 + g_{m1}r_{o5}}{4} \tag{6.3-68}$$

It is seen that as g_{m1} or r_{o5} increases, the CMRR will increase. The CMRR can be increased using a current sink with an output resistance greater than r_{o5}.

6.3.3 Frequency Response of Differential Amplifiers

The next subject of this section will be the frequency response of the differential amplifier. Figure 6.3-15*a* shows a frequency-dependent model of the differential-mode operation of either the MOS or BJT differential amplifier shown in Fig. 6.3-4*b* or 6.3-13, respectively. This model is suitable for finding v_{d1}/v_{id} or v_{d2}/v_{id}. For the MOS differential amplifier of Fig. 6.3-4*b*, R_1 is given in terms of Fig. 6.3-4*b* as

$$R_1 = r_{ds1} || r_{ds3} \tag{6.3-69}$$

and C_1 is given by

$$C_1 = C_{gd1} + C_{gd3} + C_{db1} + C_{db3} + C_L \tag{6.3-70}$$

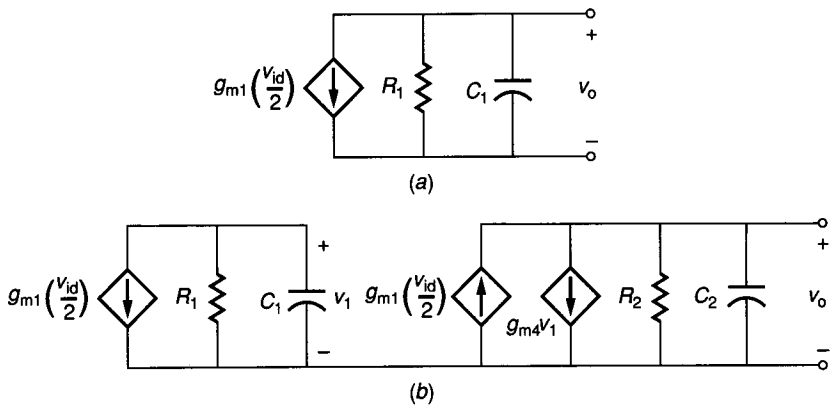


FIGURE 6.3-15
Frequency-dependent models for: (*a*) Differential amplifiers of Fig. 6.3-4*b* and Fig. 6.3-13, (*b*) Differential amplifiers of Fig. 6.3-4*c* and Fig. 6.3-11.

where C_L is the load capacitance attached to the junction of the drains of M1 and M3. If the output voltage is taken at v_{d2}, then the subscripts 1 and 3 of Eqs. 6.3-69 and 6.3-70 should be replaced by 2 and 4, respectively.

For the BJT differential amplifier of Fig. 6.3-13, the values of R_1 and C_1 are

$$R_1 = r_{o1} || r_{o3} \tag{6.3-71}$$

and

$$C_1 = C_{\mu 1} + C_{CS1} + C_{CS3} + C_{\mu 3} + C_L \tag{6.3-72}$$

The same comment regarding subscript interchange holds for the BJT differential amplifier of Fig. 6.3-13.

The differential-mode frequency response of the circuit of Fig. 6.3-15*a* can be written as

$$A_{vds}(s) = \frac{A_{vds}(0)\omega_1}{s + \omega_1} = \frac{A_{vds0}\omega_1}{s + \omega_1} \tag{6.3-73}$$

where

$$A_{vds0} = -g_{m1}R_1 \tag{6.3-74}$$

and

$$\omega_1 = \frac{1}{R_1 C_1} \tag{6.3-75}$$

For a MOS differential amplifier with $I_{SS} = 100\ \mu A$, $\lambda = 0.01\ V^{-1}$, $C_{db} = 100$ fFg, $C_{gs} = 0.2$ pF, $C_{gd} = 50$ pF, and $C_L = 0.5$ pF, we find that $R_1 = 1\ M\Omega$ and $C_1 = 0.8$ pF. The -3 dB frequency of this MOS differential amplifier is 199 kHz. If $I_{EE} = 100\ \mu A$, $V_{AFN} = 100$ V, $V_{AFP} = 50$ V, $C_\mu = 1$ pF, $C_{CS} = 1$ pF,

and $C_L = 5$ pF, then R_1 and C_1 are 0.667 MΩ and 9 pF, respectively. This gives a -3 dB frequency of 26.5 kHz for the BJT differential amplifier.

The differential-mode frequency response of the MOS differential amplifier of Fig. 6.3-4*c* and the BJT differential amplifier of Fig. 6.3-11 can be found from the small signal model given in Fig. 6.3-15*b*. For the MOS version, R_1, R_2, C_1, and C_2 can be written as

$$R_1 = \frac{1}{g_{m3}} || r_{ds1} || r_{ds3} \simeq \frac{1}{g_{m3}} \tag{6.3-76}$$

$$R_2 = r_{ds2} || r_{ds4} \tag{6.3-77}$$

$$C_1 = C_{gd1} + C_{gs3} + C_{gs4} + C_{bd1} + C_{b23} \tag{6.3-78}$$

and

$$C_2 = C_{gd2} + C_{gd4} + C_{bd2} + C_{bd4} + C_L \tag{6.3-79}$$

For the BJT differential amplifier, R_1, R_2, C_1, and C_2 are

$$R_1 = \frac{1}{g_{m3}} || r_{o3} || r_{\pi 3} || r_{\pi 4} || r_{o1} \simeq \frac{1}{g_{m3}} \tag{6.3-80}$$

$$R_2 = r_{o2} || r_{o4} \tag{6.3-81}$$

$$C_1 = C_{\mu 1} + C_{CS1} + C_{\pi 3} + C_{\pi 4} + C_{CS3} \tag{6.3-82}$$

and

$$C_2 = C_{\mu 2} + C_{CS2} + C_{\mu 4} + C_{CS4} + C_L \tag{6.3-83}$$

The frequency response for Fig. 6.3-15*b* can be written as

$$A_{vds}(s) = \frac{v_o}{v_{id}} = \frac{-g_{m1}R_2\omega_2}{2(s + \omega_2)}\left[1 + \frac{g_{m4}R_1\omega_1}{s + \omega_1}\right] =$$

$$\frac{-g_{m1}R_2\omega_2[s + \omega_1(1 + g_{m4}R_1)]}{2(s + \omega_1)(s + \omega_2)} = \frac{A_{vds0}[(s/\omega_1') + 1]}{[(s/\omega_1 + 1)][(s/\omega_2) + 1]} \tag{6.3-84}$$

where

$$A_{vds0} = -0.5g_{m1}R_2(1 + g_{m4}R_1) \tag{6.3-85}$$

$$\omega_1 = \frac{1}{R_1C_1} \tag{6.3-86}$$

$$\omega_1' = (1 + g_{m4}R_1)\omega_1 \tag{6.3-87}$$

and

$$\omega_2 = \frac{1}{R_2C_2} \tag{6.3-88}$$

It is of interest to note that the configuration of Fig. 6.3-15*b* introduces an extra pole-zero pair. The zero is in the left-hand plane and is equal to $(1 + g_{m4}R_1)$ times the pole. Since R_1 is approximately equal to the value of $1/g_{m3}$, the value of the zero is approximately twice that of the pole (called a *doublet*). In most cases, the effect of ω_1 and ω_2' approximately cancel each other out. Assume that $K_N' = 2K_P' = 25\ \mu A/V^2$, all W/L ratios are unity $C_{gs} = 100$ fF, and $I_{SS} = 100\ \mu A$. The MOS parameters used earlier permit the calculation of R_1, R_2, C_1, and C_2 as 19.6 kΩ, 1 MΩ, 0.35 pF, and 0.8 pF, respectively. This leads to a low-frequency gain magnitude of 100 and a −3 dB frequency of 199 kHz. If the current gain of the BJTs is $\beta_F = 100$, $C_\pi = 5$ pF, and $I_{EE} = 100\ \mu A$, using the previous parameters permits the calculation of R_1, R_2, C_1, and C_2 for the BJT differential amplifier as 490 Ω, 0.67 MΩ, 13 pF, and 9 pF, respectively. This gives a low-frequency gain magnitude of 1340 and a −3 dB frequency of 26.4 kHz.

6.3.4 Noise Performance of Differential Amplifiers

The last consideration of this section deals with the noise performance of the differential amplifier. Because of the similarity in small signal performance between the differential amplifier and the inverting amplifier, we expect the noise performance to be similar. Let us consider the noise analysis of Fig. 6.3-4*c* and Fig. 6.3-11. The noise models for each of these circuits are shown in Fig. 6.3-16. The noise of I_{SS} and I_{EE} is neglected because they are common-mode inputs and have a much smaller influence on the output noise. A dc battery, V_{out}, has been connected to the output through which an output-noise-current spectral density flows. It can be shown for both amplifiers that

$$\overline{I}_{on}^2 = g_{m1}^2 \overline{V}_{n1}^2 + g_{m2}^2 \overline{V}_{n2}^2 + g_{m3}^2 \overline{V}_{n3}^2 + g_{m4}^2 \overline{V}_{n4}^2 \tag{6.3-89}$$

This result is developed by using superposition techniques. The equivalent input-noise-voltage spectral density can be found by dividing Eq. 6.3-89 by g_{m1}^2 to get

$$S_{eq} = S_{VN1} + S_{VN2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 (S_{VN3} + S_{VN4}) \tag{6.3-90}$$

where $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$ has been assumed. Assuming that $S_{VN1} = S_{VN2}$ and $S_{VN3} = S_{VN4}$ gives

$$S_{eq} = 2S_{VN1}\left[1 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{S_{VN3}}{S_{VN1}}\right)\right] \tag{6.3-91}$$

Although the type of noise has not been identified, in general the noise will be reduced if $g_{m3} \leq g_{m1}$.

The differential amplifier is a very useful building block which will be used in analog circuits that follow. The differential amplifier is an excellent choice as an input stage for several reasons. It allows the application of difference signals and rejects the common mode signals. This means that an unwanted singal

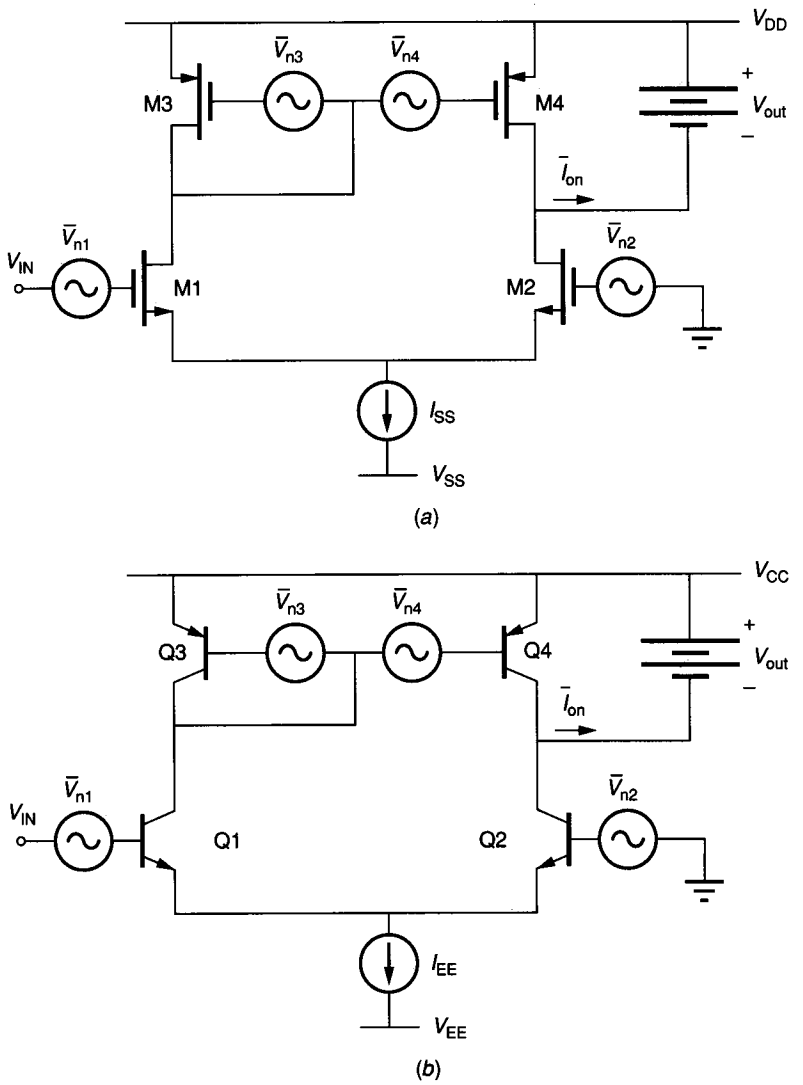


FIGURE 6.3-16
(*a*) Noise model for the CMOS differential amplifier of Fig. 6.3-4*c*. (*b*) Noise model for the BJT differential amplifier of Fig. 6.3-11.

present at both inputs will be rejected. The large input common-mode range allows the ac performance to be independent of the dc input voltage. A third advantage is that larger output signal swings can be obtained differentially. This is important as the trend to reduce power supplies makes it difficult to have sufficient dynamic range. Table 6.3-1 summarizes the performance of the differential amplifiers presented in this section.

TABLE 6.3-1
Comparison of small signal voltage gains for the differential amplifiers of Sec. 6.3

Differential amplifier	Figure	Differential-in, single-ended-out voltage gain, A_{vds}	Differential-in, differential-out voltage gain, A_{vdd}
MOS active load	6.3-4*a*	$\frac{g_{m1}}{2g_{m3}}$	$\frac{g_{m1}}{g_{m3}}$
MOS current source load	6.3-4*b*	$\frac{g_{m1}}{2(g_{ds2} + g_{ds4})}$	$\frac{g_{m1}}{g_{ds2} + g_{ds4}}$
MOS current mirror load	6.3-4*c*	$\frac{g_{m1}}{g_{ds2} + g_{ds4}}$	—
BJT current mirror load	6.3-11	$\frac{g_{m1}}{g_{o2} + g_{o4}}$	—
BJT current source load	6.3-13	$\frac{g_{m1}}{2(g_{o1} + g_{o3})}$	$\frac{g_{m1}}{g_{o1} + g_{o3}}$

6.4 OUTPUT AMPLIFIERS

In many applications, the output load of a circuit can significantly influence the performance of the circuit. The output load generally consists of a load resistor, R_L, in parallel with a load capacitor, C_L. If R_L is small or if C_L is large, the previous amplifiers may not be able to meet the output signal requirements. The objective of an output amplifier is to provide a large output voltage swing across the load. The requirements of the output amplifier can be divided into static requirements and dynamic requirements. The static requirement can be stated as the ability to maintain a dc voltage somewhere between the power supply limits across a specified load resistor. This implies that the output stage should have a low Thevenin output resistance and should be efficient in order to avoid large power dissipation in the amplifier. The dynamic requirement is the ability to charge or discharge a large capacitance at a specified voltage rate. This requirement is often associated with slew rate or the maximum output voltage rate of an analog circuit. The dynamic requirement does not require a low output resistance but does demand high currents to achieve the desired slew rate.

There are two distinct approaches to implementing output stages. These approaches depend on whether or not feedback is used. We will first consider the approach that does not use feedback. The first nonfeedback output amplifier type consists of the inverting amplifiers of Sec. 6.1. We will examine the large signal performance of these amplifiers to determine their suitability as output amplifiers. Figures 6.1-11*a*, 6.1-11*b*, 6.1-11*c*, and 6.1-18*a* represent the inverting amplifiers we will consider. In Sec. 6.1 we analyzed the small signal performance. Since the output amplifier is likely to have large output voltage swings, let us first consider the limitations of the output stage.

6.4.1 Output Amplifiers without Feedback

A conservative approach to characterize the output signal swings of MOS amplifiers is to assume that all devices must be in saturation. This constrains the operation to the transition region of the voltage transfer function of the amplifier. Figures 6.1-12 and 6.1-14 show that the resulting output range is not as large as that which could be achieved if some of the devices are allowed to operate in the active or ohmic region.

Consider the output swing limits of Fig. 6.1-11*a*. We assume that V_{IN} can have values between V_{DD} and V_{SS}. (This aggressive assumption partially compensates for the conservative approach of assuming all devices are saturated.) When $V_{IN} = V_{SS}$, M1 is off and the maximum output voltage is

$$V_{OUT}(\max) \approx V_{DD} - |V_{TP}| \tag{6.4-1}$$

When $V_{IN} = V_{DD}$, M1 is on and in fact is in the ohmic region because V_{DS1} will be small. The current in M2 which is in the saturation region is

$$I_{D2} = \frac{\beta_2}{2}(V_{SG2} - |V_{TP}|)^2 = \frac{\beta_2}{2}(V_{DD} - V_{OUT} - |V_{TP}|)^2 = \frac{\beta_2}{2}(V_{OUT} - V_{DD} + |V_{TP}|)^2 \tag{6.4-2}$$

The current in M1 is

$$\begin{aligned} I_{D1} &= \beta_1\left[(V_{GS1} - V_{TN})V_{DS1} - \frac{V_{DS1}^2}{2}\right] \\ &= \beta_1\left[(V_{DD} - V_{SS} - V_{TN})(V_{OUT} - V_{SS}) - \frac{(V_{OUT} - V_{SS})^2}{2}\right] \end{aligned} \tag{6.4-3}$$

Equating Eq. 6.4-2 to Eq. 6.4-3 and solving for V_{OUT} gives

$$V_{OUT}(\min) = V_{DD} - V_T - \frac{V_{DD} - V_{SS} - V_T}{\sqrt{1 + (\beta_2/\beta_1)}} \tag{6.4-4}$$

where it has been assumed that $V_T = V_{TN} = |V_{TP}|$. Using the model parameters and voltages specified in Fig. 6.1-12 the above equations give a $V_{OUT}(\max)$ of 4.25 V and a $V_{OUT}(\min)$ of -4.52 V. If we used the saturation constraint, the lower voltage limit would be higher (approximately -2.8 V).

The MOS inverting amplifier of Fig. 6.1-11*c* has approximately the same large signal behavior, with one exception. Because the source of M2 is not connected to the bulk, V_{T2} will be larger than normal, causing the maximum value of V_{OUT} to be less, as seen from Eq. 6.4-1.

The MOS inverting amplifier of Fig. 6.1-11*b* has a higher ac gain than the previous two amplifiers. It can be seen that when $V_{IN} = V_{SS}$, M1 is off and V_{OUT} is at V_{DD}. Therefore,

$$V_{OUT}(\max) \approx V_{DD} \tag{6.4-5}$$

Using the approach outlined by Eqs. 6.4-2 and 6.4-3 we can show that

$$V_{OUT}(\min) = (V_{DD} - V_{SS} - V_{TN}) \cdot \left[1 - \sqrt{1 - \left(\frac{\beta_2}{\beta_1}\right)\left(\frac{V_{DD} - V_{GG2} - |V_{TP}|}{V_{DD} - V_{SS} - V_{TN}}\right)^2}\right] + V_{SS} \quad (6.4\text{-}6)$$

if $V_{IN} = V_{DD}$. Evaluating these limits under the conditions given in Fig. 6.1-14, we get $V_{OUT}(\max) \approx 5$ V and $V_{OUT}(\min) \approx -4.97$ V, which agree with the results of Fig. 6.1-14.

The maximum output swing of the BJT inverting amplifier of Fig. 6.1-18*a* can be found in a similar manner. When $V_{IN} = V_{EE}$, Q1 is off and V_{OUT} is at V_{CC}. Therefore,

$$V_{OUT}(\max) \approx V_{CC} \quad (6.4\text{-}7)$$

When V_{IN} is increased so that Q1 becomes saturated, then V_{OUT} is equal to

$$V_{OUT}(\min) \approx V_{SS} + V_{CE1}(\text{sat}) \approx V_{SS} + 0.2 \text{ V} \quad (6.4\text{-}8)$$

It is seen that the BJT inverting amplifiers generally have a larger output swing than the MOS inverting amplifiers.

The previous considerations emphasized the ability to have large output voltage swings. However, no load was considered, so the results just given are appropriate for large resistance loads. Of perhaps more importance is the signal swing for small values of load resistance. Unfortunately, this is difficult to analyze. Instead, let us examine the ability to source or sink current when the output swings are small. Once again we consider the inverting amplifiers. Figures 6.4-1*a* and *b* show MOS and BJT amplifiers using a current-source load sometimes called a "pull-up". It will be assumed that current flows in both output devices during the entire swing of the output voltage. This is called Class

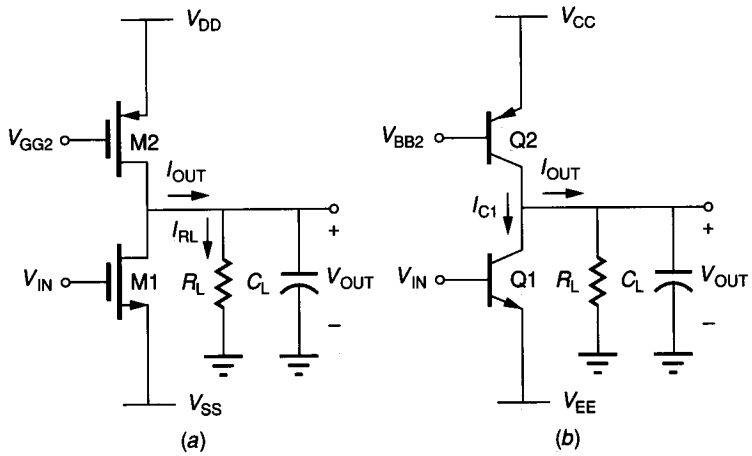


FIGURE 6.4-1
Class A output amplifiers: (*a*) Common-source configuration, (*b*) Common-emitter configuration.

A operation. Let us first consider the static performance (the ability to source and sink currents at a dc output voltage for which the output devices are both in saturation or forward active region).

The maximum source current, I_{OUT}^{+}, that can be obtained from the circuit of Fig. 6.4-1*a* occurs when M1 is off and M2 is saturated, is given as

$$I_{OUT}^{+} = \frac{K_P' W_2}{2L_2}[V_{DD} - V_{GG2} - |V_{T2}|]^2 \tag{6.4-9}$$

It is important to note that as long as M2 is saturated this current always flows in M2 regardless of the value of V_{IN}. The maximum sinking current, I_{OUT}^{-}, for Fig. 6.4-1*a* occurs when M1 is saturated and $V_{IN} = V_{DD}$ and is given as

$$I_{OUT}^{-} = \frac{K_N' W_1}{2L_1}(V_{DD} - V_{SS} - V_{T1})^2 - I_{OUT}^{+} \tag{6.4-10}$$

It should be observed that I_{OUT}^{-} must also include I_{OUT}^{+} because of the Class A nature of the biasing. Fortunately, the current-sinking capability of M1 can easily exceed I_{OUT}^{+} because the gate-source voltage of M1 can be very large.

If V_{OUT} approaches V_{SS}, then M1 will pass from the saturation to the ohmic region where $V_{DS1} < V_{GS1} - V_{T1}$. If a load resistance R_L is connected to the output, V_{DS1} is small, and $V_{IN} = V_{DD}$, then Eq. 6.4-10 for the ohmic region becomes

$$I_{D1} \approx \frac{K_N' W_1}{L_1}(V_{DD} - V_{SS} - V_{T1})(-I_{OUT}^{-} R_L - V_{SS}) \tag{6.4-11}$$

Since I_{D1} is the sum of I_{OUT}^{+} and I_{OUT}^{-}, we can solve for I_{OUT}^{-} as

$$I_{OUT}^{-} \approx \frac{-K_N'(W_1/L_1)(V_{DD} - V_{SS} - V_{T1})V_{SS} - I_{OUT}^{+}}{1 + K_N'(W_1/L_1)(V_{DD} - V_{SS} - V_{T1})R_L} \tag{6.4-12}$$

When V_{OUT} approaches V_{DD}, I_{OUT}^{+} will become dependent on R_L and have a smaller value than that of Eq. 6.4-9. Figure 6.4-2 shows a plot of the output voltage of the circuit of Fig. 6.1-11*b* as a function of the input for a 1 kΩ load resistor. Note that the *W/L* values have been increased to provide more current sinking and sourcing capability. Using the parameter values given in Fig. 6.4-2, I_{OUT}^{+} is 202 μA and I_{OUT}^{-} is 2.53 mA. When multiplied by 1 kΩ, these currents give the maximum output voltages. It is seen that the sinking current is approximately 10 times the sourcing current. The sourcing current could be increased by decreasing the gate voltage on M2 or increasing W_2/L_2. In either case, the bias current that flows would increase, causing the power dissipation in the inverter to increase. It should be noted that the load resistance of 1 kΩ has caused the inverter voltage gain to be less than unity.

The small signal output resistance of the inverting voltage amplifier is a measure of how the ac gain will be influenced by the presence of a small load resistance. For example, consider the MOS inverter of Fig. 6.1-11*b* with the parameters given in Fig. 6.4-2, where $R_L = 1$ kΩ. Using Eq. 6.1-50, we find that at $V_{OUT} = 0$ V the ac voltage gain should be −36.3, assuming that R_L is

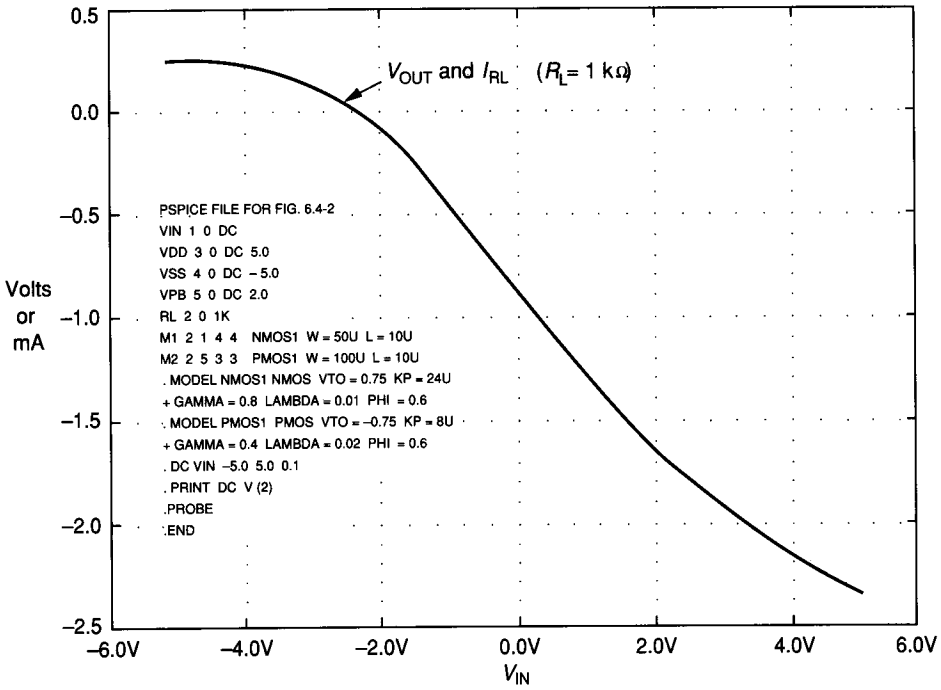


FIGURE 6.4-2
Simulation of Fig. 6.4-1*a*.

infinite. The output resistance under these conditions is found from Eq. 6.1-52 as $r_{out} = 165\ \text{k}\Omega$. When loaded with R_L, the new ac gain is given as

$$A_v' = A_v\left(\frac{R_L}{R_L + r_{out}}\right) \tag{6.4-13}$$

where A_v is the ac voltage gain for $R_L = \infty$ and A_v' is the gain for a finite R_L. In this case, A_v' is equal to $-36.3(1/166) = -0.22$. This value compares favorably with the simulated result of Fig. 6.4-2 at $V_{OUT} = 0$ V. Consequently, another desirable characteristic of an output amplifier is to have a small value of r_{out} so that the small signal voltage gain predicted by Eq. 6.4-13 is not reduced.

The maximum source/sink output currents and the ac output resistance characterize the static performance of the output amplifier. These two measures are related by the quiescent bias current (I_{BIAS}) of the amplifier. For example, suppose we want to sustain +4 V across a 10 kΩ load resistance. This would require an I_{BIAS} of at least 400 μA (assuming M1 is off). With a 400 μA bias current, the small signal output resistance is 125 kΩ if λ is 0.01 V^{-1}. Because of the large, small signal output resistance, the output of the common-source configuration is best modelled by a controlled current source in parallel with the 125kΩ output resistance.

Under dynamic conditions, the output sinking/sourcing current needed to charge or discharge C_L may be greater than that required to maintain a given dc

voltage across R_L. It is assumed in the following analysis that the output voltage is in the range where both output transistors are in saturation. The current required to charge a capacitor C_L at a rate of dV_{OUT}/dt is given by

$$| I_{OUT} | = C_L \left[\frac{dV_{OUT}}{dt} \right] \tag{6.4-14}$$

If the desired rate of rise is 10 V/μs and C_L is 50 pF, then the bias current must be at least 500 μA. This consideration is valid for $V_{OUT} \approx 0$. As the output voltage deviates from 0 V, the current available for charging C_L is reduced by the current necessary to sustain a nonzero value of V_{OUT} across R_L.

Similar conditions hold for the BJT Class A inverting voltage amplifier of Fig. 6.4-1*b*. The maximum sourcing current is determined by Q2 and is given as

$$I_{OUT}^{+} = I_{S2} \exp \left[\frac{V_{CC} - V_{BB2}}{V_t} \right] \tag{6.4-15}$$

There is an important distinction between this relationship and the similar one for the MOS amplifier in Eq. 6.4-9. That difference is that V_{BB2} must be able to sink from the base of Q2 a current of I_{OUT}^{+}/β_{F2}. Typically, Q2 is part of a current mirror so that I_{OUT}^{+} is defined by the input current to the mirror. The maximum sinking current can be determined as V_{IN} is increased. As V_{BE1} is increased, the sinking current becomes very large. A more appropriate measure of the sinking current would be to examine more closely the circuit that is driving the amplifier of Fig. 6.4-1*b*. In general, any driver can be characterized by an equivalent voltage source, V_S, and series resistance, R_S. The maximum sinking current can be expressed as

$$I_{OUT}^{-} = \left[\frac{V_S(\max) - V_{EE} - V_{BE1}}{R_S} \right] \beta_{F1} - I_{OUT}^{+} \tag{6.4-16}$$

where $V_S(\max)$ is the maximum positive swing of V_S and $V_{BE1} \approx 0.7$ V. Assuming $V_S(\max) \approx -2$ V and $R_S = 10$ kΩ for the conditions of Fig. 6.1-18*a* and Fig. 6.1-19, we get $I_{OUT}^{+} \approx 1.39$ mA and $I_{OUT}^{-} = 21.6$ mA. For a 1 kΩ load resistance, the output voltage swing would be from +1.39 V to −5 V. Figure 6.4-3 shows a simulation of the circuit of Fig. 6.4-1*b* using the same parameters as for Fig. 6.1-19, except that a load resistance of 1 kΩ has been added. We note that the current in Q1 increases from 0 to 6.6 mA, which is sufficient to overcome I_{OUT}^{+} and to sink 5 mA through $R_L = 1$ kΩ. We also note that the ac gain has been greatly reduced. The output sinking/sourcing analysis of Fig. 6.4-1*b* is similar to that of Fig. 6.4-1*a* and will not be repeated here.

The small signal output resistance can be used to predict the reduction of gain using Eq. 6.4-13. For example, the gain for $R_L = \infty$ and output resistance for the circuit of Fig. 6.4-1*b* were calculated in Example 6.1-4 for $V_{OUT} = 0$ V as −1544 and 26 kΩ, respectively. Using Eq. 6.4-13 we predict the new ac gain (at $V_{OUT} = 0$ V) as −57. This compares very well with the slope of Fig. 6.4-3 at $V_{OUT} = 0$.

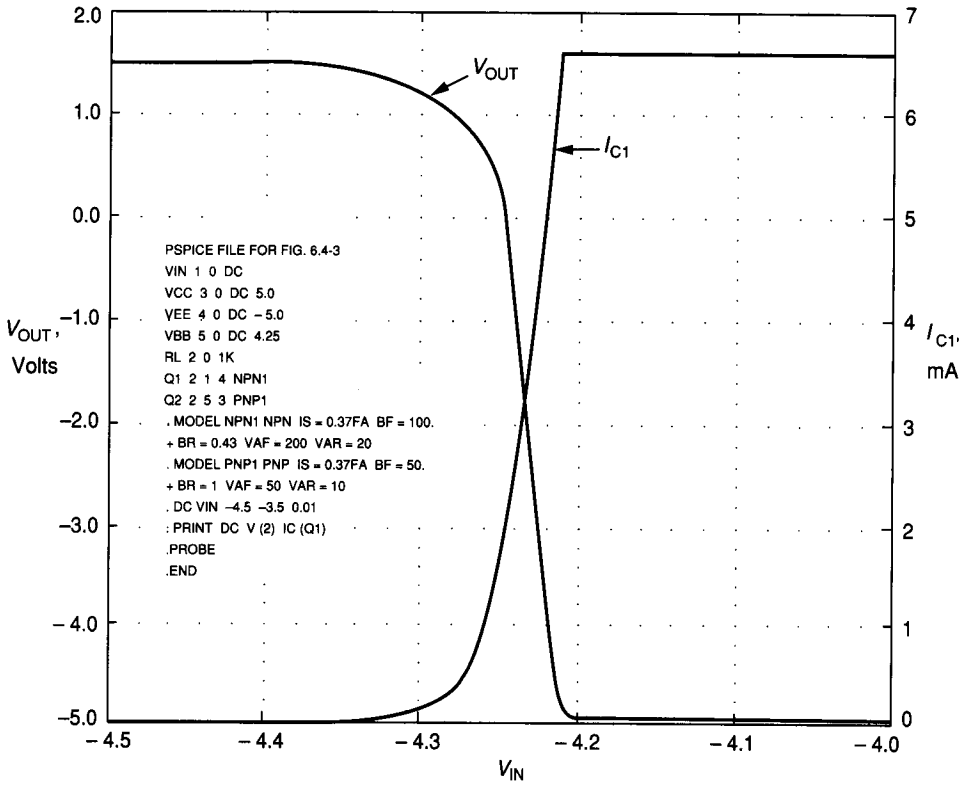


FIGURE 6.4-3
Simulation of Fig. 6.4-1*b*.

One of the disadvantages of the Class A inverting amplifiers of Fig. 6.4-1 is that considerable quiescent power is dissipated. It is well known that the maximum efficiency of the Class A amplifier is 25% for a sinusoidal signal. This means that under best conditions, for every milliwatt of ac power applied to R_L, 3 mW are dissipated in the transistors. For example, consider the two amplifiers of Fig. 6.4-1 with 1 kΩ load resistances. With the output signal at 0 V, the amplifier of Fig. 6.4-1*a* dissipates 2 mW and that of Fig. 6.4-1*b* dissipates 13.9 mW. The maximum symmetrical output voltage signal swing is 0.2 V (peak-to-peak) and 1.39 V (peak-to-peak) for Fig. 6.4-1*a* and *b*, respectively. Unfortunately, we have had to take the smaller of the positive or negative signal swing to avoid distortion. Assuming a sinusoidal output, the maximum power delivered to R_L is 0.04 mW and 1.93 mW, respectively. Correspondingly, the best sinusoidal efficiencies of the circuit of Fig. 6.4-1*a* and *b* are 2% and 13.9%, respectively. It is clear that the bias currents should be increased to reach the maximum output voltage signal swings if one wishes to approach more closely the maximum possible efficiency of 25%.

One advantage of the Class A amplifier is low distortion. This is a result of operating both MOS transistors in the saturation region or operating both BJT transistors in the normal active region over most of the output voltage swing.

A second method of implementing an output amplifier without feedback is the common-source or common-emitter, Class B or Class AB amplifiers. The circuits of Fig. 6.4-4*a* and *b* show MOS and BJT implementations, respectively. V_B is a floating battery used to establish the proper bias of the devices. The sinking/sourcing output current capability of such amplifiers is very large and is limited primarily by the power dissipation capability of the devices. If the transistors are biased so that no drain or collector current flows when V_{IN} is zero, the stage is termed Class B. When V_{IN} is positive, the lower device is on and the upper device is off. When V_{IN} is negative, the lower device is off and the upper device is on. The maximum possible efficiency of the Class B amplifier for a sinusoidal output signal is 78.5%, where the efficiency is defined as the ratio of the signal power dissipated in R_L to the power provided from the power supplies for sinusoidal input.

The primary advantage of the implementations of Fig. 6.4-4 is that the maximum sourcing/sinking current is not limited by the bias current. This allows output amplifiers to have I_{OUT}^{-} limitations similar to the I_{OUT}^{+} levels of the Class A output amplifiers. Figure 6.4-5 shows the simulated output swing capability for the circuit of Fig. 6.4-4*a* with $V_B = 0$, $W_1/L_1 = 50\ \mu/10\ \mu$, $W_2/L_2 = 150\ \mu/10\ \mu$, and $R_L = 1\ \text{k}\Omega$. This circuit has a maximum sink/source current limit given by Eq. 6.4-12 of 2.53 mA, resulting in a ± 2.53 V output signal swing. These calculations agree well with the simulation results of Fig. 6.4-5. The drain

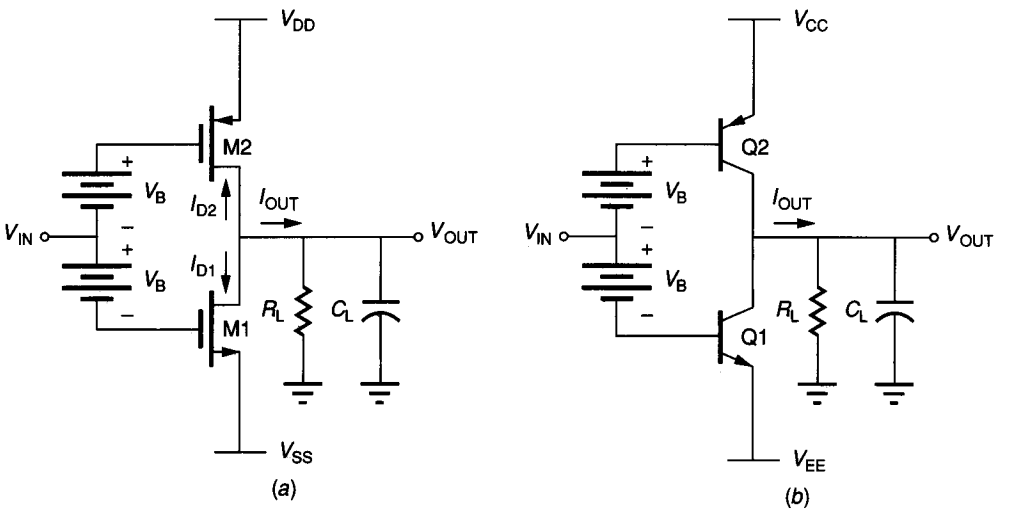


FIGURE 6.4-4
Class B and AB output amplifiers: (*a*) MOS common-source configuration, (*b*) BJT common-emitter configuration.

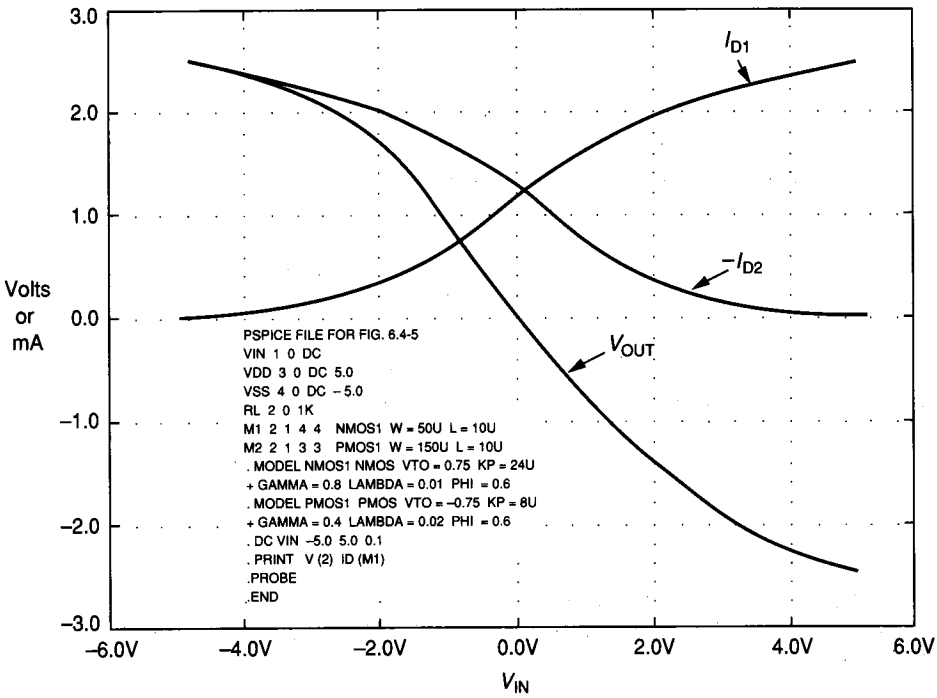


FIGURE 6.4-5
Simulation of Fig. 6.4-4*a* with $V_B = 0$ V.

currents in M1 and M2 are also plotted in Fig. 6.4-5. Because both M1 and M2 are conducting in the region around $V_{IN} \approx 0$, this amplifier is called Class AB. The results of Fig. 6.4-5 can be used to show that if $V_B \approx 4$ V, then the amplifier will be operating in Class B mode. Figure 6.4-6 shows a simulation corresponding to that of Fig. 6.4-5 for $V_B = 4$ V. Several things should be noted. The first is that M1 is off when M2 is on and vice versa. The second is that V_B has caused the maximum source and sink currents to be reduced from 2.53 mA to 1.6 mA. Also note that the transfer function is nonlinear about $V_{IN} = 0$. This nonlinearity will introduce distortion in the output signal. A good compromise for this amplifier would be to go back to Class AB operation by choosing $V_B \approx 3$ V.

As we have seen in previous sections, the battery V_B is necessary for the push-pull BJT inverting amplifier. The range of values for V_B of the BJT circuit of Fig. 6.4-4*b* is

$$V_{CC} - V_{IN} - 0.7 < V_B < V_{CC} - V_{IN} \tag{6.4-17}$$

Similar considerations to those discussed for Fig. 6.4-4*a* hold for Fig. 6.4-4*b*.

Class AB and B amplifiers represent a good method of implementing the output amplifier having the ability to provide ±3 V across 1 kΩ with ±5 V power supplies. Consider now the sizing of M1 and M2 in the circuit of Fig. 6.4-4*a*. We can use Eq. 6.4-11 with $I_{D1} = I_{\overline{OUT}}$ to calculate W_1/L_1. Let us assume

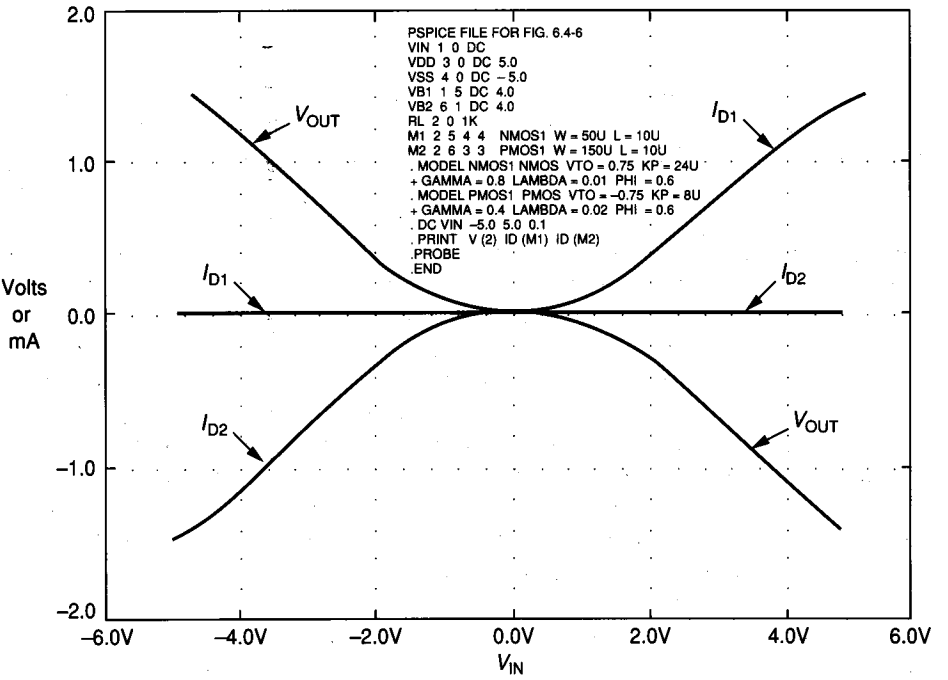


FIGURE 6.4-6
Simulation of Fig. 6.4-4*a* with $V_B = 4$ V.

that $I_{OUT}^{-} = 4$ mA to anticipate the reduction in $I_{OUT}^{-}(I_{OUT}^{+})$ that will occur when V_B is non-zero. The results give $W_1/L_1 = 180\ \mu/10\ \mu$. In order to balance the ability of the amplifier to source and sink current, $W_2/L_2 = (K_N/K_P)(W_1/L_1)$, or $W_2/L_2 = 540\ \mu/10\ \mu$. From the results shown in Figs. 6.4-5 and 6.4-6, we will choose $V_B = 3$ V. Figure 6.4-7 gives the simulated results. While this design can provide an output swing of ± 3 V across 1 kΩ, it experiences distortion above ± 2.2 V. This distortion is caused by the fact that the transistor sourcing or sinking the current is entering the ohmic region, and the current increase is linearly related to the gate voltage rather than to the square of the voltage. This can be clearly seen by the current results in Fig. 6.4-7. Consider the positive output voltage swing. The current is being sourced by M2, and at about $V_{IN} = 2$ V, which corresponds to $V_{OUT} = 2.2$ V, the rate of current increase in M2 falls off. This circuit is more suitable for ± 2 V output swings. To achieve a linear ± 3 V output voltage swing, we would have to increase the power supply to ± 6 V. It should also be noted that the voltage gain turned out to be approximately -1. Since it is not necessary for the output amplifier to have a large gain, this is not a problem; however, the voltage gain, $-g_{m1}R_L(=-g_{m2}R_L)$, depends on the value of R_L and may be less than unity.

Although the small signal output resistance of the Class B amplifier is high, it represents a good solution to the output amplifier, except for the implementation

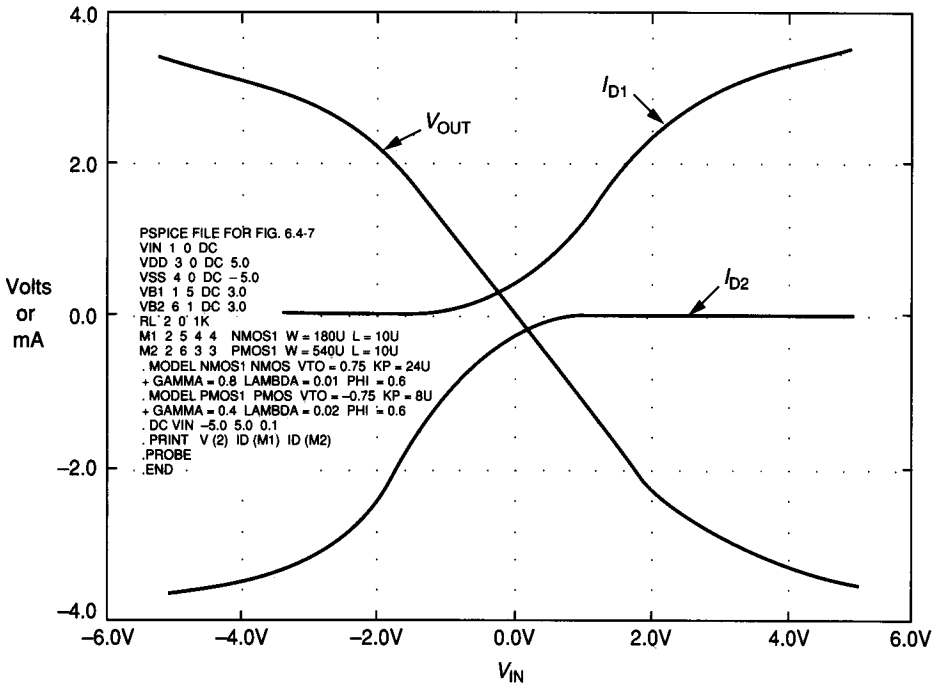


FIGURE 6.4-7
Simulation of Fig. 6.4-4*a* with $V_B = 3$ V.

of the floating battery, V_B. Figure 6.4-8 shows how the cross-coupling of four devices can allow the design of Class AB or B operation. The operation (Class AB or B) is determined by the voltages V_{GG4} and V_{GG5} (V_{BB4} and V_{BB5}), which are used to establish the bias current in the output devices M1 and M2 (Q1 and Q2). When the input voltage is taken positive, the current in M8 (Q8) increases and the current in M7 (Q7) decreases. If the operation is Class B, then M7 (Q7) turns off. As the current in M8 (Q8) increases, it is mirrored as an increasing current in M1 (Q1), which provides the sinking capability for the output current. When V_{IN} is decreased, M2 (Q2) can source output current. The output signal swing is limited to within a V_T value of V_{DD} or V_{SS} (V_{BE} of V_{CC} or V_{EE}).

The frequency response of the inverting amplifiers is generally determined by the load resistance and the shunt capacitance at the output including the load capacitance. Since $R_L(=1/G_L)$ is typically much less than r_{out} and C_L is typically much larger than the capacitances at the output node of the amplifier, the bandwidth is given as

$$\omega_{-3dB} = \frac{g_{out} + G_L}{C_{out} + C_L} \approx \frac{1}{R_L C_L} \tag{6.4-18}$$

which is primarily a function of the loading. If $C_L = 100$ pF and $R_L = 1$ kΩ, then the −3 dB bandwidth is 10 Mrps or 1.59 MHz.

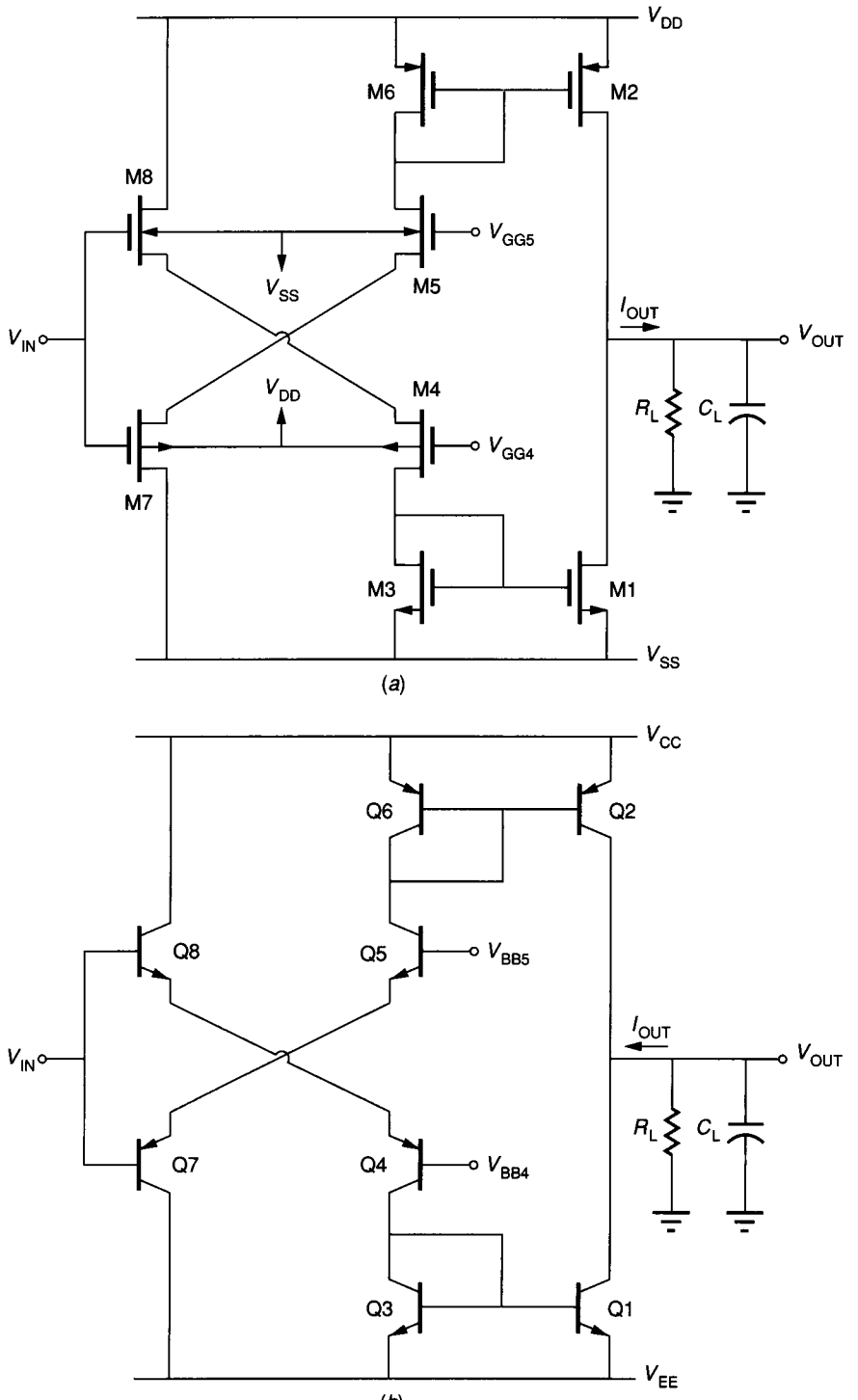


FIGURE 6.4-8
Class B or AB output amplifiers showing implementation of the floating battery for (*a*) Fig 6.4-4*a* and (*b*) Fig. 6.4-4*b*.

6.4.2 Output Amplifiers with Feedback

The second approach to the design of an output amplifier uses the principle of shunt feedback. Shunt feedback can be shown to reduce the output resistance by the following relationship

$$r'_{\text{out}} = \frac{r_{\text{out}}}{1 + \text{LG}} \tag{6.4-19}$$

where r_{out} is the output resistance without feedback and LG is the loop gain of the negative feedback loop. The simplest implementation of shunt feedback at the output is the Class A source follower and emitter follower configurations shown in Fig. 6.4-9. The follower configuration has both large current gain and low output resistance. Unfortunately, since the source is the output node, the source follower of Fig. 6.4-9*a* is dependent on the body effect, γ. The body effect causes the value of V_T to increase as the output voltage is increased. This creates a situation where the maximum output voltage of an n-channel source follower is considerably lower than $V_{DD} - V_{TO}$.

The emitter follower is also limited in its ability to obtain large positive output swing. It turns out that as the output voltage increases, more current is demanded from Q1. This emitter current is related to the base current by $I_E = (1 + \beta_F)I_B$. As the base voltage approaches V_{CC}, it becomes impossible to provide sufficient base current to sustain large positive swings. In this case, the maximum positive swing of the npn emitter follower is limited by the lack of current-sourcing capability at the peak of the positive swing. In both types of followers, the maximum negative swing is determined by the bias current sink. Usually, for appropriate size devices, the maximum negative swing is $V_{SS} + V_T$ for the MOS follower and $V_{EE} + V_{BE}$ for the BJT follower.

One advantage of the follower configuration as an output amplifier is a low small signal output resistance. This low resistance causes the ac voltage gain (and

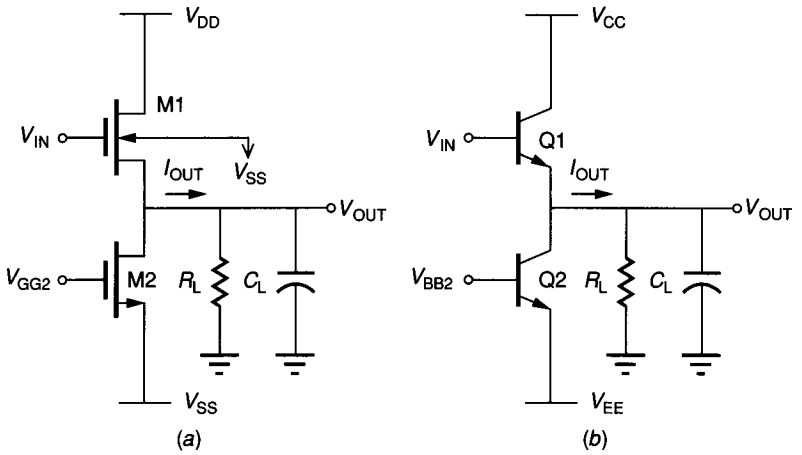


FIGURE 6.4-9
(*a*) Class A source follower, (*b*) Class A emitter follower.

frequency response) to be less dependent on R_L. The small signal model for the circuit of Fig. 6.4-9*a* is shown in Fig. 6.4-10. Figure 6.4-11 shows the small signal model for the emitter follower of Fig. 6.4-9*b*. Both of these circuits can be analyzed using Fig. 6.4-12 along with the appropriate values for the resistances and capacitances. For the source follower, we have

$$C_1 = C_{gd1} \tag{6.4-20a}$$

$$R_2 = \infty \tag{6.4-20b}$$

$$C_2 = C_{gs1} \tag{6.4-20c}$$

$$R_3 = \left[g_{m1} + g_{mb1} + g_{ds1} + g_{ds2} + G_L\right]^{-1} \approx \left[g_{m1} + G_L\right]^{-1} \tag{6.4-20d}$$

and

$$C_3 \simeq C_L \tag{6.4-20e}$$

For the emitter follower, we have

$$C_1 = C_{\mu 1} \tag{6.4-21a}$$

$$R_2 = r_{\pi 1} \tag{6.4-21b}$$

$$C_2 = C_{\pi 1} \tag{6.4-21c}$$

$$R_3 = \left[g_{m1} + g_{o1} + g_{o2} + G_L\right]^{-1} \approx \left[g_{m1} + G_L\right]^{-1} \tag{6.4-21d}$$

and

$$C_3 \simeq C_L \tag{6.4-21e}$$

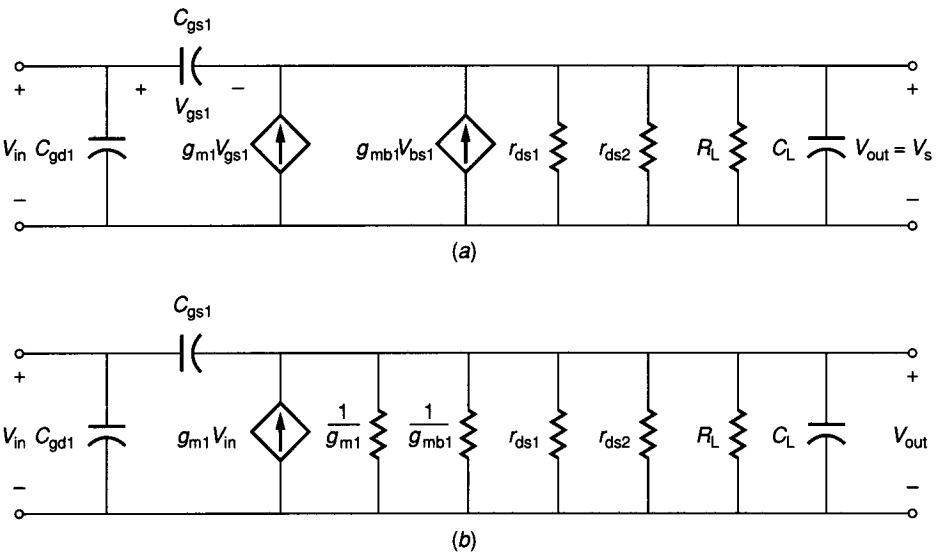


FIGURE 6.4-10
(*a*) Small signal model of Fig. 6.4-9*a*, (*b*) Simplified equivalent of (*a*).

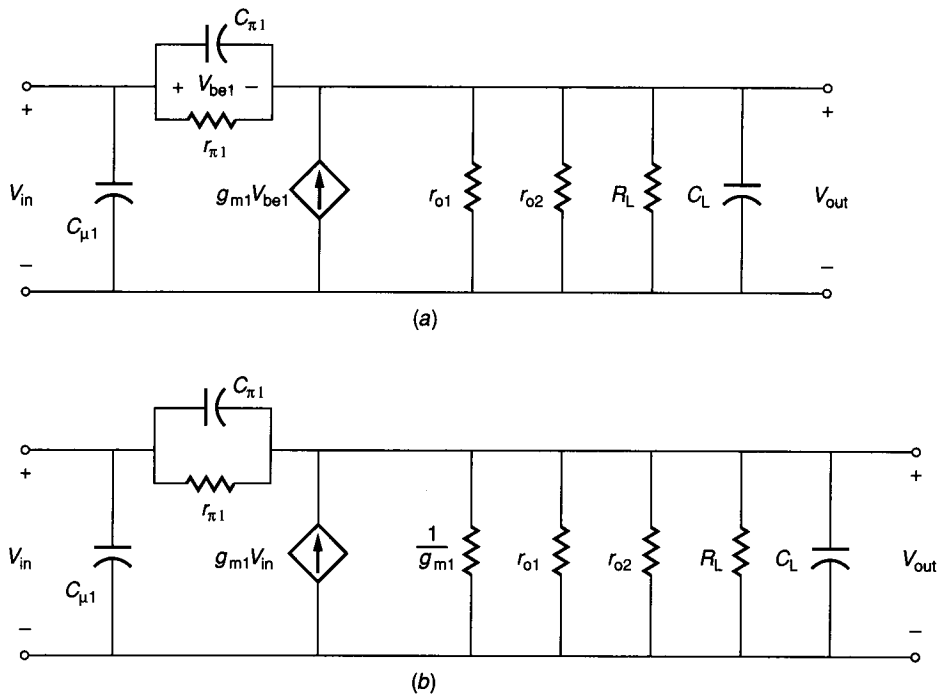


FIGURE 6.4-11
(*a*) Small signal model of Fig. 6.4-9*b*, (*b*) Simplified equivalent of (*a*).

Assuming that Fig. 6.4-12 is voltage-driven allows us to find the transfer function as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m + G_2 + sC_2}{G_2 + G_3 + s(C_L + C_2)} \tag{6.4-22}$$

From Eq. 6A-20 and 6.4-21, the midband gain is

$$\frac{V_{out}}{V_{in}} = A_{v0} = \frac{g_m + G_2}{G_2 + G_3} \approx \frac{g_{m1}}{g_{m1} + G_L} \tag{6.4-23}$$

The zero of Eq. 6.4-22 is

$$z_1 = -\frac{g_m + G_2}{C_2} \approx -\frac{g_{m1}}{C_2} \tag{6.4-24}$$

and the pole is

$$p_1 = -\frac{G_2 + G_3}{C_2 + C_L} \approx -\frac{g_{m1} + G_L}{C_L} \tag{6.4-25}$$

Typically, $|p_1| < |z_1|$. If the pole and zero are close together, they will tend to cancel each other.

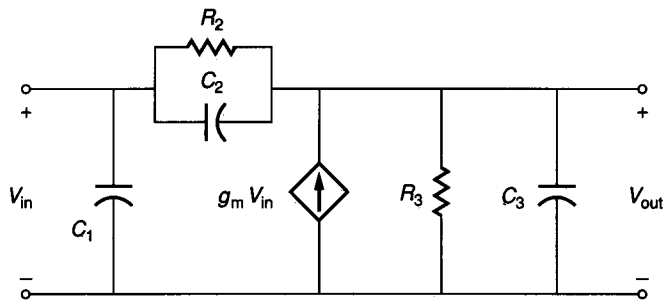


FIGURE 6.4-12
Generic small signal follower model.

The output resistance of the follower not including R_L is found from Fig. 6.4-12 as

$$r'_{out} = (G_2 + G_3)^{-1} = (G_2 + g_{m1})^{-1} \approx \frac{1}{g_{m1}} \tag{6.4-26}$$

For the MOS follower, this resistance is expressed as

$$r'_{out} \simeq \left(\frac{L_1}{2K'_N W_1 I_{D1}}\right)^{1/2} \tag{6.4-27}$$

and for the BJT follower, the output resistance is

$$r'_{out} \simeq \frac{V_t}{I_{C1}} \tag{6.4-28}$$

If the bias current in both followers of Fig. 6.4-9 is 100 μA, and if $W_1 = 10L_1$ and $K'_N = 25\ \mu A/V^2$, then the output resistance of the MOS follower is 4.47 kΩ and that of the BJT follower is 250 Ω.

The performance of the BJT follower is ideally independent of the emitter areas. Considerations of power dissipation and matching suggest large emitter areas whereas capacitive loading and high frequency response suggest small emitter areas.

The Class A shunt feedback follower configuration has the further disadvantage of an asymmetric current sinking and sourcing capability. For the followers of Fig. 6.4-9, the maximum current sourcing capability is limited primarily by the driver. For the MOS follower, the gate voltage of M1 must be sufficiently larger than the output voltage in order for M1 to source the required current. For the BJT follower, the current sourcing is directly related to the amount of base current the driver can provide. The sinking capability is equal to the bias current. As a consequence, the sourcing and sinking capabilities are usually different. The maximum efficiency of either follower configuration of Fig. 6.4-9 is 25%.

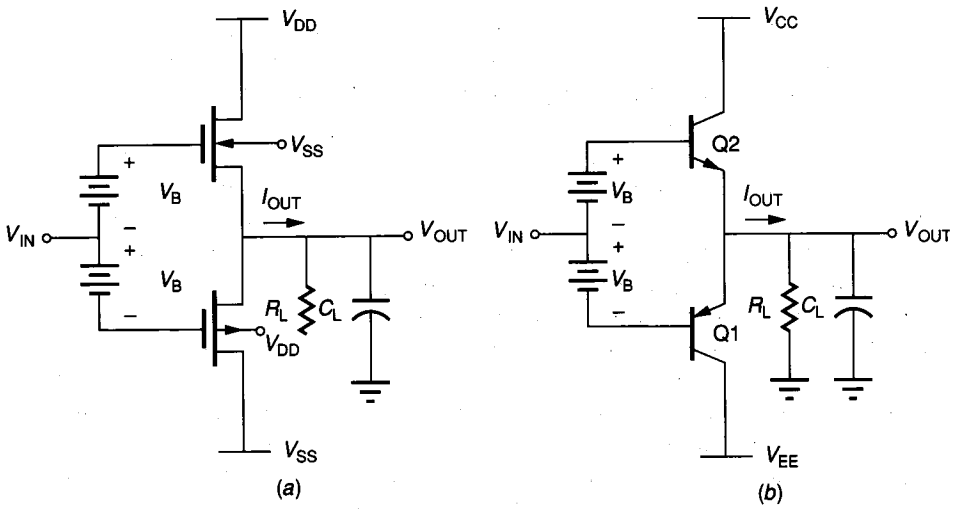


FIGURE 6.4-13
(*a*) Class B source follower, (*b*) Class B emitter follower.

In summary, the Class A follower has very low output resistance, poor signal swing, and low efficiency. The efficiency of the Class A follower can be improved by the Class B followers shown in Fig. 6.4-13. This configuration is also called the Class B push-pull amplifier. The maximum possible efficiency is 78.5%. Also, the maximum sourcing and sinking capabilities are likely to be of the same magnitude, although this depends on the driver. The signal swings at both the positive and negative limits will suffer from the increasing V_T for the MOS Class B follower and from the inability to provide sufficient base currents for the BJT Class B follower.

Figure 6.4-14 shows how the floating batteries, V_B, can be implemented for the Class B followers. In this case, the input is applied at the gate of M3 (base of Q3) instead of to the sources of M4 and M5 (bases of Q4 and Q5) and will require some form of level shifting. The bias current in M4 and M5 (Q4 and Q5) determines whether the circuit is Class B or Class AB. It is generally preferable to bias the output devices in Class AB in order to minimize the crossover distortion that occurs in the push-pull, follower type amplifier when the output current switches from one device to the other. Unfortunately, it is never possible to eliminate this distortion, and it is usually necessary to use external negative feedback to reduce the nonlinear distortion to an acceptable level. Figure 6.4-14 illustrates some of the problems in obtaining a large output signal swing for the Class B follower circuit. For example, the maximum output voltage of the circuit of Fig. 6.4-14*a* is approximately $V_{GG6} - V_{TO6} - V_{T2}$. This limit will usually be several volts below V_{DD}. The negative swing is a little better since M3 can take the gate of M1 to V_{SS}. Thus, the negative signal swing is approximately $V_{SS} + V_{T1}$. Unfortunately, V_{T1} will be larger than V_{TO1} because of the body effect.

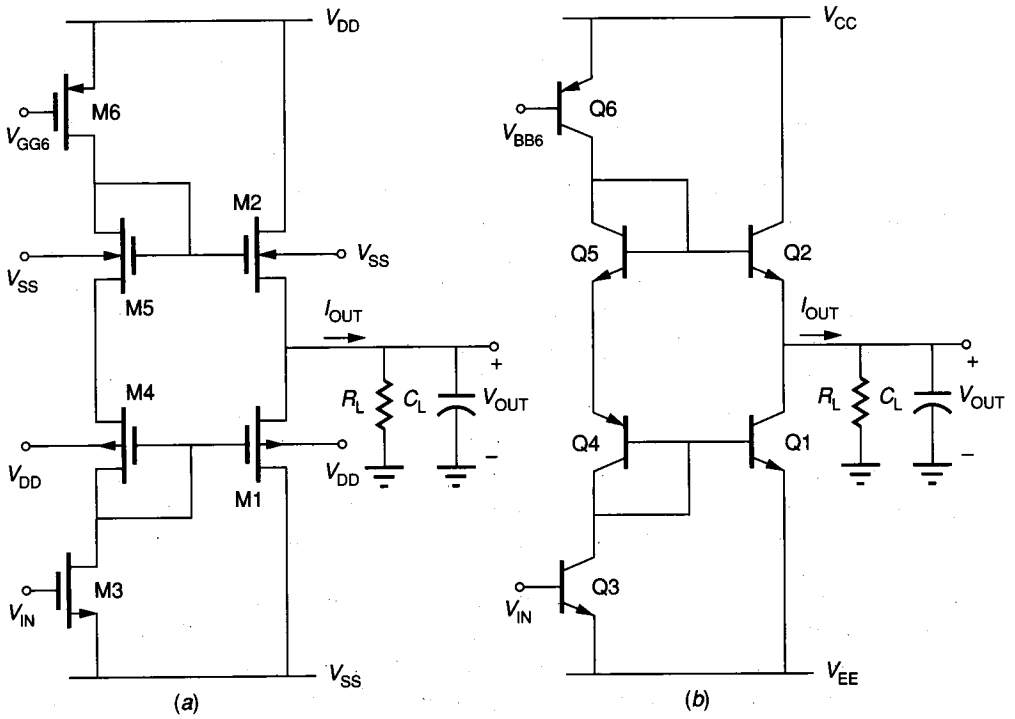


FIGURE 6.4-14
Implementation of: (*a*) Fig. 6.4-13*a*, and (*b*) Fig. 6.4-13*b*, including the implementation of V_B.

At this point we have a situation that often occurs in analog circuit design. The right principles have been identified, but the implementation is still not practical. None of the preceding output amplifiers have contained all of the desirable features of (1) large output signal swings, (2) low output resistance, (3) high efficiency, and (4) low nonlinear distortion. In addition, high frequency performance is also desirable. A practical solution to our problem is shown in Fig. 6.4-15, where we have taken the best candidate and concentrated on improving its negative characteristics. The Class B/Class AB common source (emitter) amplifiers in Fig. 6.4-4 offer good swing characteristics, high efficiency, and low nonlinear distortion. Their primary disadvantage is a high output impedance. Combining the shunt feedback principle with the common-source or common-emitter Class B or Class AB amplifier results in an output stage that meets all specifications even though it has been complicated by additional circuitry.

The output resistance of Fig. 6.4-4 will be reduced approximately by the value of loop gain as given in Eq. 6.4-19. The loop gain of the circuit of Fig. 6.4-15 will be that of the inverter plus the error amplifier. We note that the error amplifier could be implemented by the differential amplifiers of the preceding section. The error amplifiers are designed to turn on M1 or M2 (Q1 or Q2) in a manner that minimizes crossover distortion but maximizes efficiency.

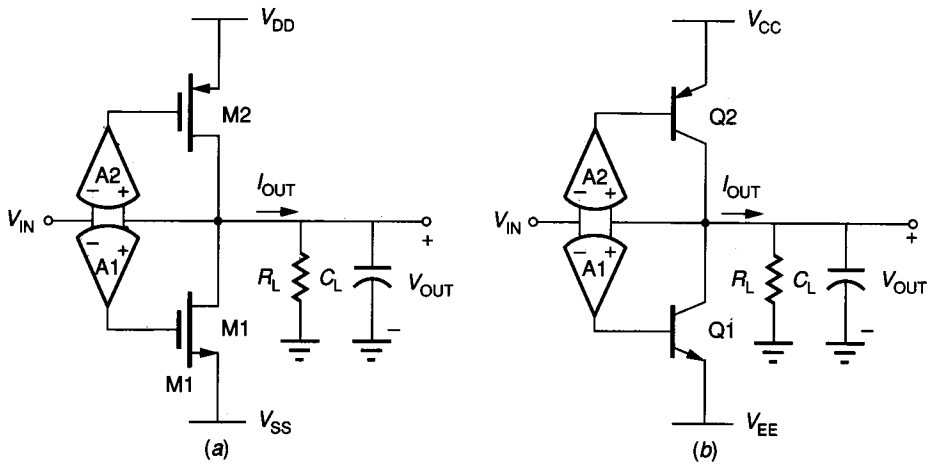


FIGURE 6.4-15
Use of negative feedback with error amplifiers A1 and A2 to obtain an improved output amplifier: (*a*) MOS, (*b*) BJT.

Figure 6.4-16 shows an interesting implementation of the circuit of Fig. 6.4-15. Since the inverter can have reasonable gain, it is possible to use resistive feedback to replace the more complex error amplifier. The resistance R_2 should be twice R_1 so that the input signal does not have to be capable of maintaining the output signal swing. The resistors do not have to be carefully matched and could be polysilicon, diffusion, n- or p-well, or even transistors in the case of the MOS version. Assuming that $R_2 = 2R_1$, the loop gain would be

$$\text{LG} \simeq \frac{g_m R_L}{3} \tag{6.4-29}$$

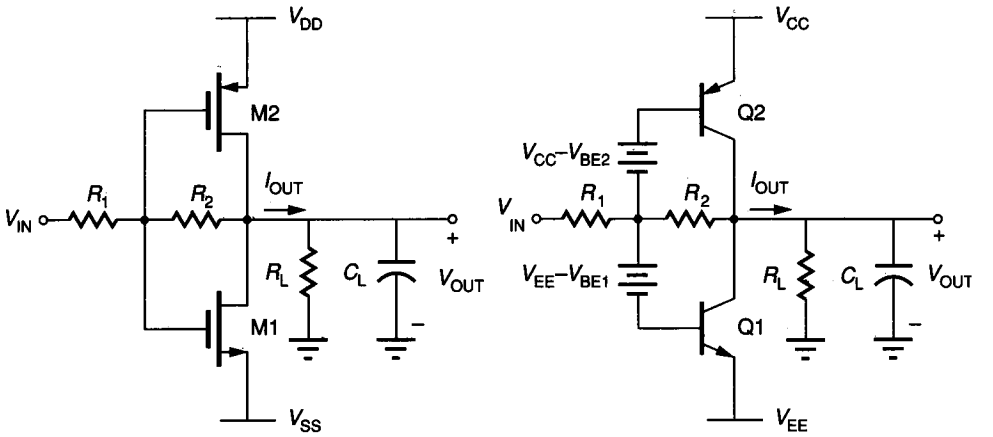


FIGURE 6.4-16
A possible implementation of Fig. 6.4-15.

where g_m is the transconductance of M1 or M2 (Q1 or Q2). Thus, the output resistance of the circuit of Fig. 6.4-16 is expressed as

$$r'_{out} \simeq \frac{r_{out}}{1 + (g_m R_L/3)} \tag{6.4-30}$$

where r_{out} is the resistance of the output amplifier with the loop open.

The frequency response of output amplifiers should be large in order not to cause stability problems in the circuit driving the output amplifier. In general, the frequency response of the output amplifier is determined by its input resistance and capacitance. This implies that the input devices of the output amplifier should be as small as possible for high frequency response.

The design of an output amplifier capable of serving as a buffer between an integrated circuit amplifier and a load consisting of a small resistance and/or large capacitance has been considered in this section. Although not all approaches have been examined, the material discussed gives the principles and allows the reader to appreciate the problems involved. The performance of the various output amplifiers presented in this section is compared in Table 6.4-1. The comparison is made on a qualitative basis because of the complexity involved in the analysis of output amplifiers. In many cases, the performance of the output amplifier determines the performance of the overall circuit and will require much more attention than has been allocated in this section. All of the circuits presented have been used in actual integrated circuits and will be used in various circuits in the next section.

6.5 OPERATIONAL AMPLIFIERS

One of the most important circuits in analog circuit design is the operational amplifier (op amp). Its primary use is to provide sufficient gain to define and implement analog signal processing functions through the use of negative feedback. Such analog signal processing functions include amplification, integration, and summation. In this section we will consider the characteristics and architectures of general op amps. This will be followed by a "first-cut" design of two-stage BJT and CMOS op amps. Architectures capable of driving large load capacitance and small load resistance are presented and discussed. Finally, a brief consideration of simulation and testing of op amps will be given.

6.5.1 Characterization of Op Amps

An op amp has a differential input capability and is represented by the symbol shown in Fig. 6.5-1. The differential input voltages are V_1 and V_2, and the single-ended output voltage is V_O. The op amp ideally has infinite differential input resistance, R_{id}, infinite differential-mode voltage gain, A_v, and a zero output resistance, R_{out}. Although we have assumed the op amp is a voltage-controlled voltage-source, it can be implemented by any of the four types of controlled sources.

TABLE 6.4-1
Performance comparison of output amplifiers

Output amplifier	Figure	I_{OUT}^{+}	I_{OUT}^{-}	r_{OUT}	Efficiency	Linearity	Maximum voltage swing
Class A MOS inverter	6.4-1*a*	I_{BIAS}	$>> I_{BIAS}$	High	<25%	Good	Fair
Class A BJT inverter	6.4-1*b*	I_{BIAS}	$>> I_{BIAS}$	Medium	<25%	Good	Good
Class AB MOS inverter	6.4-4*a*	High for large W/L	High for large W/L	High	<50%	Fair	Fair
Class AB BJT inverter	6.4-4*b*	High if base current is large	High if base current is large	Medium	<50%	Fair	Good
Class B MOS inverter	6.4-4*a*	High for large W/L	High for large W/L	High	<75%	Poor	Fair
Class B BJT inverter	6.4-4*b*	High if base current is large	High if base current is large	Medium	<75%	Poor	Good
Class A MOS source follower	6.4-9*a*	High for large W/L	I_{BIAS}	Low	<25%	Poor	Poor (+) Good (−)
Class A BJT emitter follower	6.4-9*b*	High if base current is large	I_{BIAS}	Low	<25%	Poor	Poor (+) Good (−)
Class B MOS source follower	6.4-13*a*	High for large W/L	High for large W/L	Low	<75%	Poor	Poor
Class B BJT emitter follower	6.4-13*b*	High if base current is large	High if base current is large	Low	<75%	Poor	Poor
Class AB inverter with negative feedback	6.4-15	High if base current or W/L is large	High if base current or W/L is large	Low	<75%	Good	Good

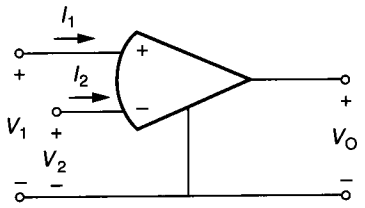


FIGURE 6.5-1
Symbol for the op amp.

In most cases, we can assume that the differential voltage gain, A_v, approaches infinity. If this assumption is valid, then the input terminals of the op amp realize a null port if the output, V_O, is connected back to the input (often through resistors or one or more op amp circuits) to achieve negative feedback. A *null port* is a two-terminal network whose voltage and current are simultaneously equal to zero. Thus, in Fig. 6.5-1, a null port is characterized by

$$| V_1 - V_2 | = 0 \tag{6.5-1}$$

and

$$| I_1 | = | I_2 | = 0 \tag{6.5-2}$$

These two relationships make it very easy to analyze the most common of op amp circuits when the differential gain is assumed to approach infinity and the output of an op amp is returned to the minus input to achieve negative feedback.

Unfortunately, the op amp only approaches the ideal op amp just described. Some of the nonideal op amp characteristics are illustrated in Fig. 6.5-2. This model will be used to define the various characteristics of the op amp. The finite differential input impedance is modeled by R_{id} and C_{id}. The output resistance

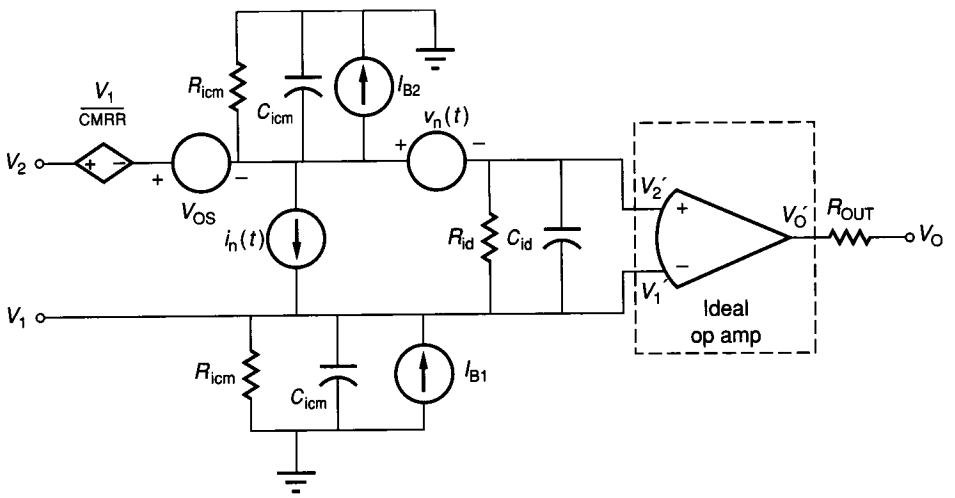


FIGURE 6.5-2
A model for a nonideal op amp showing some of the nonideal characteristics.

is modeled by R_{out}. The common-mode input resistances and capacitances are given by the resistances R_{icm} and capacitances C_{icm} connected from each of the inputs to ground. V_{OS} is the input offset voltage necessary to make the output voltage zero if both inputs of the op amp are grounded. I_{OS} (not shown) is defined as the magnitude of the difference between the two input bias currents, I_{B1} and I_{B2} necessary to make the output voltage of the op amp zero. The common-mode rejection ratio (CMRR) is approximately modeled by the voltage-controlled voltage source indicated as V_1/CMRR. The two sources designated as $\overline{V}_n$ and $\overline{I}_n$ are used to model the op amp noise and are called the noise voltage and noise current, in units of mean square volts and mean square amperes, respectively. Although these noise sources are weakly correlated, they are normally assumed to be uncorrelated.

Not all of the nonideal characteristics of the op amp are illustrated in Fig. 6.5-2. The output voltage of the op amp of Fig. 6.5-1 can be expressed as

$$V_o(s) = A_d(s)[V_1(s) - V_2(s)] + A_c(s)\left[\frac{V_1(s) + V_2(s)}{2}\right] \qquad (6.5\text{-}3)$$

where the first term on the right is the differential portion of $V_o(s)$ and the second term is the common-mode portion of $V_o(s)$. The differential frequency response of the op amp is given as $A_d(s)$, and the common-mode frequency response is given as $A_c(s)$. A typical differential frequency response for an op amp is

$$A_d(s) = \frac{A_{od}\omega_1\omega_2\omega_3\ldots}{(s + \omega_1)(s + \omega_2)(s + \omega_3)\cdots} \qquad (6.5\text{-}4)$$

where $\omega_1, \omega_2, \omega_3, \ldots$ are the poles of the operational amplifier. While the operational amplifier may have zeros, they will be ignored for the present. A_{od} (or simply A_o, where the use is understood) is the low-frequency gain of the op amp. Figure 6.5-3 shows the magnitude of a typical frequency response for the differential-mode gain, $A_d(j\omega)$ where $s = j\omega$. In this case, we see that ω_1 is much smaller than the rest of the poles, causing ω_1 to be the dominant influence in the frequency response. The objective of most compensation schemes which will be considered later is to achieve a single dominant pole so that the frequency response consists of just the -6 dB/octave slope until the magnitude of $A_d(j\omega)$ is less than 0 dB. The intersection of $|A_d(j\omega)|$ and the 0 dB axis is designated as the *unity-gain bandwidth* (GB) of the op amp. The *phase margin* is defined as the phase shift of the op amp at $\omega = GB$. A phase margin greater than 45° is desirable for negative resistive feedback around the op amp.

Other nonideal characteristics of the op amp not defined in Fig. 6.5-2 deserve mention. The *power supply rejection ratio* (PSRR) is defined as the ratio of the open loop gain of the op amp to the change in the output voltage of the op amp caused by the change in the power supply. Thus, the PSRR for V_{DD} is

$$\text{PSRR}(V_{DD}) = \frac{A_d}{(\Delta V_O/\Delta V_{DD})} = \frac{\Delta V_{DD} A_d}{\Delta V_O} \qquad (6.5\text{-}5)$$

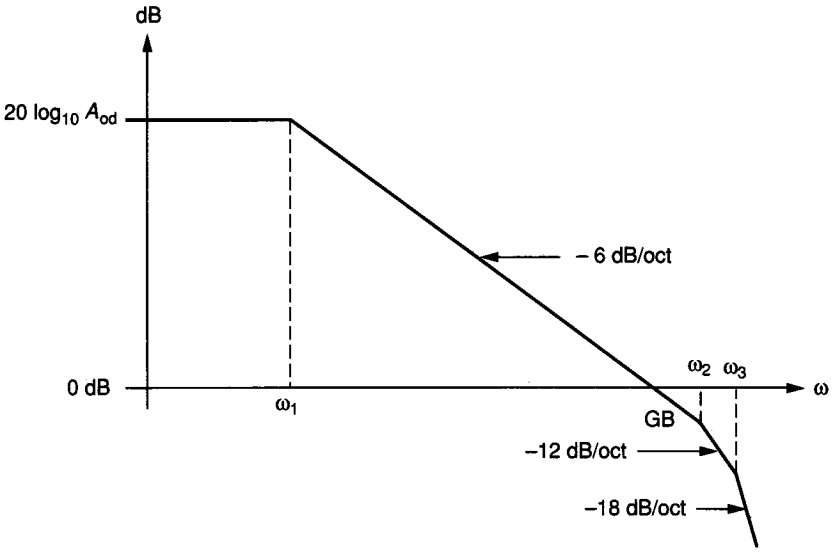


FIGURE 6.5-3
Typical frequency response of the magnitude of $A_d(j\omega)$ for an op amp.

An ideal op amp would have an infinite PSRR. The *common-mode input voltage range* is the voltage range over which the input common-mode signal can vary. Typically, this range is several volts less than the higher power supply voltage and several volts greater than the lower power supply voltage. The op amp has several other characteristics corresponding to those we have already considered for output amplifiers. These include the *maximum output sourcing* or *sinking current*, the *maximum output signal swing*, and the *slew rate*. Another characteristic of importance is the *settling time* defined as the amount of time the op amp requires in a given negative feedback configuration to respond to an input step and to settle to within a given percentage of the final value of the output step response.

The steps in designing an op amp depend on the desired values of these parameters. In this study we shall restrict ourselves to general purpose op amps that are implemented as part of an integrated circuit. Typical target specifications are shown in Table 6.5-1 for BJT and CMOS op amps. From these specifications we may propose several architectures.

The first possible op amp architecture is shown in Fig. 6.5-4*a* for the BJT op amp. This architecture is called the two-stage op amp. We observe that it consists of a differential amplifier similar to that of Fig. 6.3-11 cascaded with an inverter similar to that of Fig. 6.1-18*b*. The source of bias voltage for the differential amplifier current sink is also the source of bias voltage for the inverter's current-sink load. Two stages are often necessary because the differential amplifier generally has a voltage gain less then 60dB. The output resistance of the inverting amplifier is large and will not be capable of driving a low value of R_L. If the output resistance must be lower, then an output amplifier must be used, creating a third stage in the architecture.

TABLE 6.5-1
Typical specifications for integrated circuit BJT and CMOS op amps

Op amp specification	BJT	CMOS	Units
Differential gain, A_d	80	60	Decibels
Unity gain bandwidth, GB	1	1	Megahertz
Output resistance, r_{out}	1 K	100 K	Ohms
Input differential resistance, r_{id}	1 M	10^{12}	Ohms
Input offset voltage, V_{OS}	5	10	Millivolts
Input offset current, I_{OS}	100	-0	Nanoamperes
Power consumption, P_{DD}	10	5	Milliwatts
PSRR	80	80	Decibels
Phase margin (unity gain) (C_L = 20 pF)	60	60	Degrees
CMRR	100	100	Decibels
Slew rate (C_L = 20 pF)	± 1	± 1	Volts/microsecond
Settling time (C_L = 20 pF)	1	1	Microseconds

The two-stage architecture has the disadvantage of having two high-impedance nodes, which are indicated by A and B in Fig. 6.5-4*a*. This implies that two poles will be dominant, which will deteriorate the phase margin of the op amp. In order to resolve this situation, a Miller capacitance (C_c) is introduced between points A and B. The feedback path through C_c around the inverter causes these poles to split; it makes the pole at A dominant and for an appropriate value of C_c drives the pole at B out to or beyond GB. While this creates a single dominant pole, any large load capacitor will drive the pole at B back toward the origin, causing a poor phase margin.

The susceptibility of the Miller compensation scheme to capacitive loading has influenced the development of a second op amp architecture shown in Fig. 6.5-4*b*. This type of architecture is called the cascode configuration. A modification of this architecture, called the folded cascode configuration, is shown in Fig. 6.5-4*c*. In each of these cascode configurations, there is only one high-impedance node, which is at the output. The reason is that the input resistance of the cascode stage is very low ($1/g_m$), as was seen in Sec. 6.2. Since the gain of the cascode is approximately equal to that of the inverter, this is a very clever way of eliminating the high-impedance point at A of Fig. 6.5-4*a*. Compensation of the cascode op amp is accomplished by a capacitor connected from the output to ground. This has the attractive feature that as C_L increases, the compensation increases, keeping the op amp stable for large values of load capacitance.

Figure 6.5-5 shows the equivalent architectures for the CMOS op amp. The need for a second stage for the CMOS op amp is more obvious since the gain of a CMOS stage is typically less than that of an equivalent BJT stage. Although many other architectures for op amps exist, these represent the basic structures. They will aid in the designer's understanding of new or different architectures.

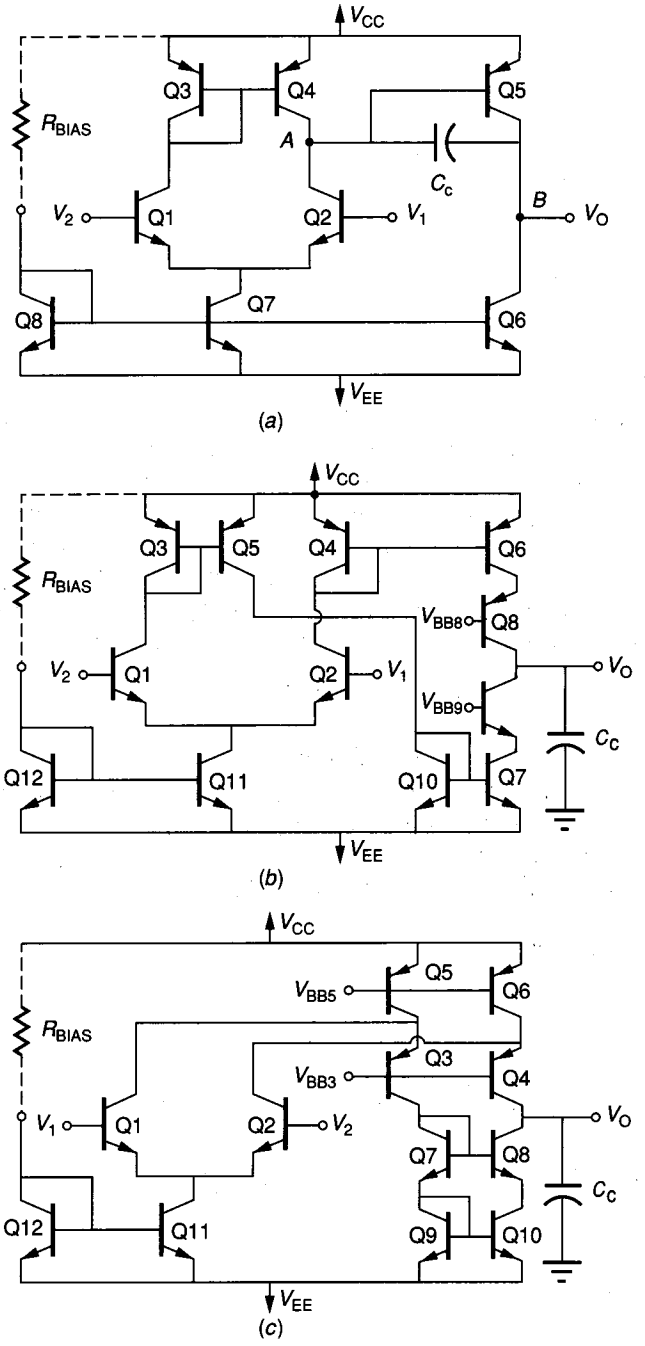
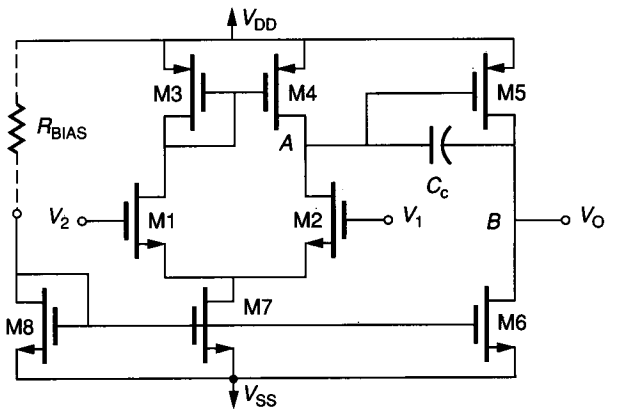
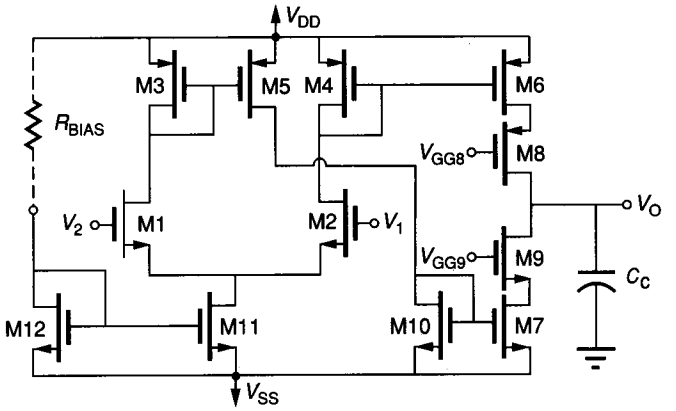


FIGURE 6.5-4
(*a*) Two-stage BJT op amp, (*b*) Cascode BJT op amp, (*c*) Folded cascode BJT op amp.



(a)



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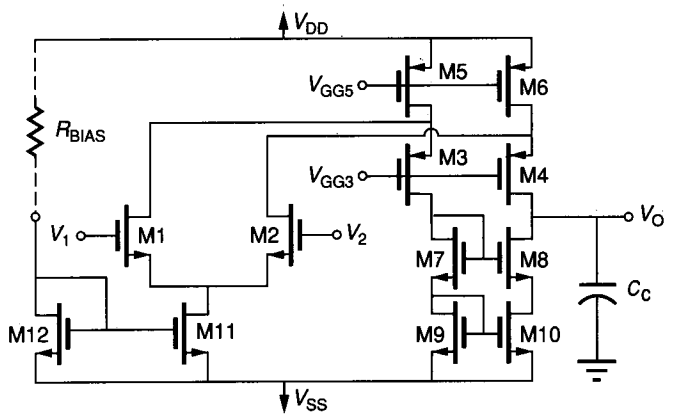


(c)

FIGURE 6.5-5
(*a*) CMOS two-stage op amp, (*b*) CMOS cascode BJT op amp, (*c*) CMOS folded cascode op amp.

6.5.2 The BJT Two-Stage Op Amp

The design of the two-stage BJT op amp will be considered first because it is the simplest.[1] Because the performance of the op amp is based on the small signal model, Fig. 6.5-6*a* shows the small signal model of the op amp of Fig. 6.5-4*a*. The first-stage model was developed in Fig. 6.3-15, where definitions of R_1, R_2, C_1, and C_2 are still valid, with the exception that $r_{\pi 5}$ is added in parallel to R_2, causing that resistance to be significantly decreased. The second stage in this model is simply that of an inverter. R_3 and C_3 are given as

$$R_3 = r_{o5} \parallel r_{o6} \tag{6.5-6}$$

and

$$C_3 = C_{\mu 5} + C_{\mu 6} + C_{CS5} + C_{CS6} + C_L \tag{6.5-7}$$

In order to simplify our considerations, assume that ω_1 and ω_1' of Eq. 6.3-84 approximately cancel and that $g_{m3} \simeq g_{m4}$. The resulting small signal, differential-input model for the two-stage BJT op amp is shown in Fig. 6.5-6*b* where $v_{id} = v_i - v_2$. The parameters of this model are defined as

$$g_{mI} = g_{m1} = g_{m2} \tag{6.5-8}$$

$$R_I = R_2 = r_{o2} \parallel r_{o4} \parallel r_{\pi 5} \tag{6.5-9}$$

$$C_I = C_2 = C_{\mu 2} + C_{\mu 4} + C_{\pi 5} + C_{CS2} + C_{CS4} \tag{6.5-10}$$

$$g_{mII} = g_{m5} \tag{6.5-11}$$

$$R_{II} = R_3 = r_{o5} \parallel r_{o6} \tag{6.5-12}$$

and

$$C_{II} = C_3 = C_{\mu 5} + C_{\mu 6} + C_{CS5} + C_{CS6} + C_L \tag{6.5-13}$$

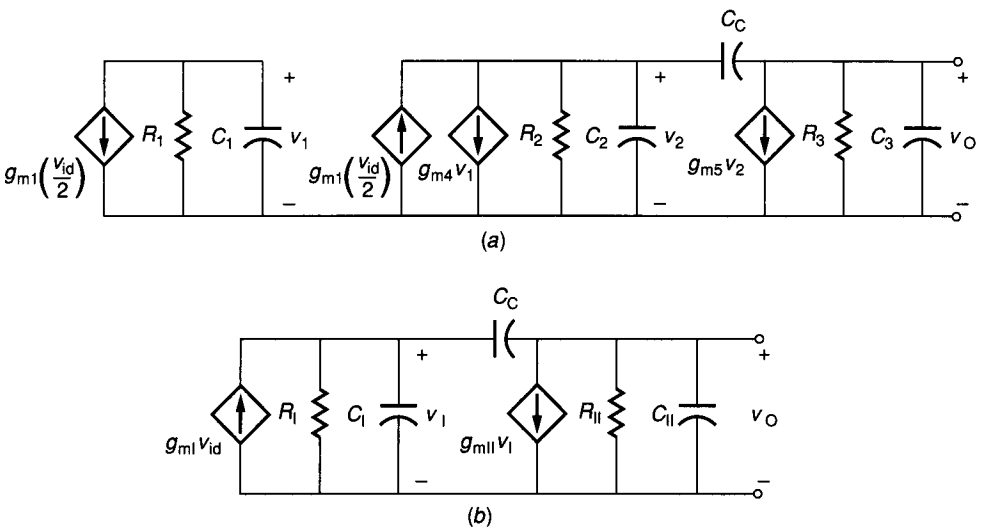


FIGURE 6.5-6
(*a*) Small signal model of Fig. 6.5-4*a* or Fig. 6.5-5*a*, (*b*) Simplified model of (*a*).

C_c is the compensation capacitance and is not included in C_I or C_{II}.

Analysis of the circuit of Fig. 6.5-6*b* illustrates how the Miller capacitor, C_c, splits the poles and accomplishes the dominant pole compensation. If C_c is zero, then the transfer function $V_O(s)/V_{ID}(s)$ is given as

$$\frac{V_O(s)}{V_{ID}(s)} = \frac{g_{mI}R_I g_{mII}R_{II}\omega_I'\omega_{II}'}{(s + \omega_I')(s + \omega_{II}')} = \frac{A_o\omega_I'\omega_{II}'}{(s + \omega_I')(s + \omega_{II}')} \tag{6.5-14}$$

where

$$\omega_I' = -p_I' = \frac{1}{R_I C_I} \tag{6.5-15}$$

and

$$\omega_{II}' = -p_{II}' = \frac{1}{R_{II}C_{II}} \tag{6.5-16}$$

p_I' and p_{II}' are the pole locations of Fig. 6.5-4*a* when C_c is zero.

When C_c is not zero, then the transfer function of Eq. 6.5-14 becomes

$$V_O(s)/V_{ID}(s) = A_o\left[1 - (sC_c/g_{mII})\right] \Big/ \Big\{ 1 + s\left[R_I(C_I + C_{II}) + R_{II}(C_{II} + C_c) + g_{mII}R_I R_{II}C_c\right] + s^2 R_I R_{II}\left[C_I C_{II} + C_c(C_I + C_{II})\right] \Big\} \tag{6.5-17}$$

Applying Eq. 6.1-26 to Eq. 6.5-17 gives

$$p_I \simeq \frac{-1}{g_{mII}R_I R_{II}C_c} \tag{6.5-18}$$

and

$$p_{II} \simeq \frac{-g_{mII}C_c}{C_I C_{II} + C_{II}C_c + C_I C_c} \tag{6.5-19}$$

Also, the zero introduced by C_c is located at

$$z = \frac{g_{mII}}{C_c} \tag{6.5-20}$$

Figure 6.5-7 summarizes these results. Figure 6.5-7*a* shows how the poles at $-p_I'$ and $-p_{II}'$ have been split into the poles at $-p_I$ and $-p_{II}$. C_c also creates a zero in the right-half plane (RHP). The effects of the RHP zero can be ignored for the BJT two-stage op amp. Figure 6.5-7*b* shows a possible form of the magnitude of the frequency response if GB $< p_{II} < z$. It is important to note that the BJT op amp will have $|p_{II}'|$ less than $|p_I'|$ if the input resistance to Q5 is not increased. Often a Darlington is used in place of Q5 for this purpose.

The preceding analysis of the BJT two-stage op amp can be summarized as follows. The low-frequency open-loop gain is given as

$$A_o = g_{mI}g_{mII}R_I R_{II} \tag{6.5-21}$$

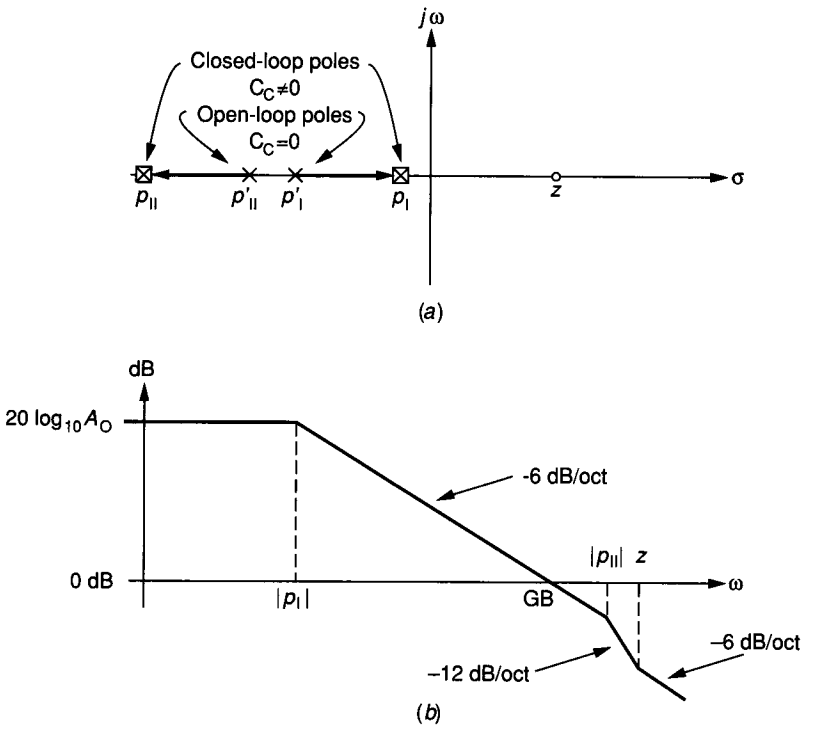


FIGURE 6.5-7
(*a*) Open- and closed-loop roots of Fig. 6.5-6*b*, (*b*) Closed-loop magnitude response of Fig. 6.5-6*b*.

The dominant pole is given by

$$| p_I | \simeq \frac{1}{g_{mII} R_I R_{II} C_c} \tag{6.5-22}$$

The unity-gain bandwidth, GB, is found by the product of Eqs. 6.5-21 and 6.5-22 and is

$$\text{GB} = \frac{g_{mI}}{C_c} \tag{6.5-23}$$

These three relationships form the basis of the two-stage op amp design along with two other constraints, which are developed below. For good phase margin, it is desirable to have $z > | p_{II} |$ and $| p_{II} | > \text{GB}$. From these two constraints, we get

$$g_{mII} > g_{mI} \tag{6.5-24}$$

and

$$C_{II} < \frac{g_{mII}}{g_{mI}} C_c \tag{6.5-25}$$

The design approach for the BJT two-stage op amp will be to establish the bias currents in the first and second stages of Fig. 6.5-4*a* to meet the specification for A_o and maintain the constraints of Eqs. 6.5-24 and 6.5-25. C_c will be chosen to meet the specification for GB. Replacing the small signal model parameters in terms of dc currents and device characteristics results in the following key equations which give a reasonable phase margin.

$$A_o \simeq \frac{g_{mI} g_{mII} r_{\pi 5}}{g_{o5} + g_{o6}} = \frac{\beta_{F5}/V_t}{1/V_{AN} + 1/V_{AP}} \left(\frac{I_{C1}}{I_{C5}} \right) \tag{6.5-26}$$

$$GB = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{I_{C1}}{V_t C_c} \tag{6.5-27}$$

$$\frac{g_{mII}}{g_{mI}} = \frac{g_{m5}}{g_{m1}} = \frac{I_{C5}}{I_{C1}} \tag{6.5-28}$$

To illustrate the design of a BJT two-stage op amp, we will assume that the desired specifications are $A_o \geq 10,000$ and GB $\simeq$ 1 MHz. Obviously, there are many other specifications of the op amp, as illustrated in Table 6.5-1, but we will start with these two. Assuming that $\beta_{FN} \simeq 200$, $\beta_{FP} \simeq 50$, $V_{AFN} \simeq 100$ V, and $V_{AFP} \simeq 50$, Eq. 6.5-26 becomes

$$A_o = 66,700 \left(\frac{I_{C1}}{I_{C5}} \right) \tag{6.5-29}$$

Choosing $I_{C5} = 5I_{C1}$ gives $A_o = 13,340$. Picking $C_c = 30$ pF gives $I_{C1} \simeq 5$ μA from Eq. 6.5-27. Thus, $I_{C5} \simeq 25$ μA. From these currents we can calculate the differential input resistance as $r_{id} \simeq 2r_{\pi 1} = 2$ MΩ and the output resistance as $r_{out} = 1.334$ MΩ. The slew rate is determined by how fast C_c can be charged and discharged. This is given by the expression

$$\text{Slew rate} = \text{SR} = \frac{I}{C_c} \tag{6.5-30}$$

where I is the smaller of $2I_{C1}$ or I_{C5}. In this example, the slew rate of the op amp is $2I_{C1}/C_c = 0.33$ V/μs. It is seen that the design of the BJT two-stage op amp is simple but constrained in its ability to simultaneously satisfy many op amp specifications. The performance is satisfactory for most applications, with the possible exception of the high output resistance. The choices that were made in this design example can be varied to achieve different values of specifications.

Up to this point, the design of the BJT two-stage op amp has not depended on the geometries of the individual devices. In other words, while Q1 and Q2 should be matched and Q3, Q4, and Q5 should be matched, there is no geometric relationship between them. The sizes of Q6, Q7, and Q8 determine the currents. Generally, a resistor is connected from the collector of Q8 to V_{CC} to establish I_{C8}. This current will be dependent on power supply variations, leading to a poor PSRR. To improve the PSRR, the current for I_{C8} must be provided by one of the current sources of Sec. 5.3. When I_{C8} is defined, the ratio of the emitter areas of Q6, Q7, and Q8 can be used to define I_{C7} ($=I_{C1}/2$) and I_{C6} ($=I_{C5}$). It is

important to keep each BJT operating in the forward active region for the best performance and largest signal swings. The sizing of the emitter areas depends on the application. Devices in the input (Q1 and Q2) and in all current mirrors should be as large as possible for matching without degrading the frequency response. The remaining device areas should be as small as possible if power dissipation is not a concern.

After an initial design has been obtained by the method illustrated, the next step is to use a simulator such as SPICE that permits the designer to consider second-order effects and examine the influence of parameter and process variation. This step is important since it gives the designer a good understanding of the performance of the op amp and of how to make tradeoffs using the computer to achieve the final design specifications.

6.5.3 The CMOS Two-Stage Op Amp

Let us consider next the design of the two-stage CMOS op amp shown in Fig. 6.5-5*a*. Since the small signal model of Fig. 6.5-6 holds for the CMOS case, Eqs. 6.5-21 through 6.5-25 are also valid. The values of R_I, R_{II}, C_I, and C_{II} for the CMOS case are given as

$$R_I = r_{ds2} \parallel r_{ds4} \tag{6.5-31}$$

$$R_{II} = r_{ds5} \parallel r_{ds6} \tag{6.5-32}$$

$$C_I = C_{gd2} + C_{gd4} + C_{gs5} + C_{db2} + C_{db4} \tag{6.5-33}$$

and

$$C_{II} = C_{gd6} + C_{db5} + C_{db6} + C_L \tag{6.5-34}$$

The key equations pertaining to the CMOS two-stage op amp design are given as

$$\begin{aligned} A_o &= g_{mI} g_{mII} R_I R_{II} = \frac{g_{m1} g_{m5}}{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds6})} \\ &= \left[\left(\frac{1}{\lambda_2 + \lambda_4}\right)\left(\frac{2K'_N W_1}{I_{D1} L_1}\right)^{1/2}\right]\left[\left(\frac{1}{\lambda_5 + \lambda_6}\right)\left(\frac{2K'_P W_5}{I_{D5} L_5}\right)^{1/2}\right] \\ &\simeq \frac{1}{2\lambda^2}\left(\frac{K'_N K'_P W_1 W_5}{I_{D1} I_{D5} L_1 L_5}\right)^{1/2} \end{aligned} \tag{6.5-35}$$

$$\text{GB} = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{1}{C_c}\left(\frac{2K'_N W_1 I_{D1}}{L_1}\right)^{1/2} \tag{6.5-36}$$

and

$$\frac{g_{mII}}{g_{mI}} = \frac{g_{m5}}{g_{m1}} = \left[\frac{K'_N I_{D1}(W_1/L_1)}{K'_P I_{D5}(W_5/L_5)}\right] \tag{6.5-37}$$

Comparing Eqs. 6.5-35 through 6.5-37 with Eqs. 6.5-26 through 6.5-28 reveals a very important difference between BJT and CMOS integrated circuits. This difference is that the performance of the CMOS op amp is dependent on the geometry of the devices, whereas the BJT op amp is independent of the geometry of its transistors. While this creates additional complexity in the expressions, the designer has much more freedom to meet the specifications of the design.

The additional degrees of freedom allow the designer to impose constraints that will ensure that all MOS devices operate in saturation over wide process variations. In Sec. 5.4, we showed how the ratio of the W/L values of two MOS devices connected gate-to-gate and source-to-source could control the ratio of the drain currents. This principle is employed in the circuit of Fig. 6.5-5*a* to ensure that M4 operates in saturation. All other devices either operate in saturation by their connection or by external potentials applied to the inputs or outputs. For matching and symmetry, we must choose $W_1/L_1 = W_2/L_2$ and $W_3/L_3 = W_4/L_4$. If we force V_{GS3} to be equal to V_{GS5} by the following relationship

$$\frac{W_3}{L_3} = \frac{W_5}{L_5}\left(\frac{I_3}{I_5}\right) \tag{6.5-38}$$

then since $I_5 = I_6$, $I_3 = I_4$, and $W_3/L_3 = W_4/L_4$, we may express Eq. 6.5-38 as

$$\frac{W_4}{L_4} = \frac{W_5}{L_5}\left(\frac{I_4}{I_6}\right) \tag{6.5-39}$$

However, because $I_4 = 0.5I_7$ and $I_7/I_8 = (W_7/L_7)/(W_8/L_8)$, the condition for M4 to remain in saturation becomes

$$\frac{W_4}{L_4} = \frac{(W_5/L_5)}{2}\left(\frac{W_7/L_7}{W_6/L_6}\right) = \frac{(W_5/L_5)}{2}\left(\frac{I_7}{I_6}\right) \tag{6.5-40}$$

To illustrate the design of a two-stage CMOS op amp such as that given in Fig. 6.5-5*a*, assume that the desired specifications are $A_o \geq 50{,}000$, GB $= 1$ MHz, and the slew rate is 2 V/μs. Assume that the device parameters are $K'_N = 2K'_P = 25\ \mu\text{A/V}^2$, $\lambda = 0.01\ \text{V}^{-1}$ and $C_c = 5$ pF. From the slew rate specification and C_c, we see that $I_{D1} = 5\ \mu$A. We will pick I_{D5} equal to 50 μA to make the zero due to Miller compensation larger than the second pole. Solving for W_1/L_1 in Eq. 6.5-36 gives $W_1/L_1 \simeq 4.0$. Since M1 and M2 are matched, W_2/L_2 is also 4.0. In Eq. 6.5-35 we may solve for W_5/L_5 to get 4.5. Since the ratio of current in M6 and M7 is I_{D5} to $2I_{D1}$, we may solve for W_4/L_4 from Eq. 6.5-40 as being 10 times less than W_5/L_5, or 0.45. Finally, one can solve for the value of W_8/L_8 necessary to establish a reasonable current in M8 and solve for W_6/L_6 and W_7/L_7 using the current ratios. The small signal input resistance, R_{id}, of the CMOS op amp is infinity because of the infinite gate resistance. The output resistance is equal to the parallel combination of r_{ds5} and r_{ds6} and is 1 MΩ for this example.

At this point, the circuit designer typically sets the smaller value of W or L equal to perhaps twice the smallest allowable value and solves for the remaining dimension. For a minimum L or W of 5 μ, Table 6.5-2 gives a set of possible

TABLE 6.5-2
A set of first-cut W and L values for the design of a CMOS two-stage op amp such as that shown in Fig. 6.6-5*a*

	M1	M2	M3	M4	M5	M6	M7	M8
W (μ)	40	40	10	10	45	10	10	10
L (μ)	10	10	22	22	10	10	50	10

W and L values for the op amp of Fig. 6.5-5*a* if the current in M8 is 50 μA when $W_8/L_8 = 1$. At this point, the designer would turn to a simulator to refine and optimize the design.

Unfortunately, the transconductance of the MOS device is not as large as for the BJT, which causes a problem due to the zero of Eq. 6.5-20. Using the values of the preceding example, we find that the zero is located at 2.39 MHz (the RHP zero for the BJT two-stage op amp was at 10.6 MHz). This RHP zero will destroy the phase margin of the CMOS two-stage amplifier. Figure 6.5-8 shows a clever way to eliminate this zero and to make the two-stage CMOS op amp of Fig. 6.5-5*a* practical. It can be shown that the new zero location is given by

$$z' = \frac{1}{C_c[(1/g_{mII}) - R_z]} \tag{6.5-41}$$

With the nulling resistor, the designer can conceptually move the RHP zero to infinity; in fact, the zero can be moved into the left-hand plane and used for lead compensation. R_z is typically implemented by an n-channel and p-channel transistor in parallel with the gates taken to the appropriate power supply. For our example of the two-stage CMOS op amp, g_{m5} was 75 μS; therefore, a value of $R_z = 13.33$ kΩ would move the RHP zero to infinity and retrieve the good stability properties. The same nulling resistor technique can be applied to the two-stage BJT op amp if necessary.

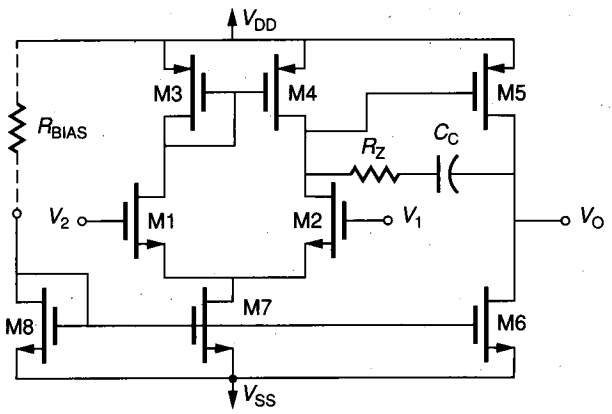


FIGURE 6.5-8
Nulling method to remove the effects of the RHP zero due to low device transconductance.

6.5.4 Cascode Op Amps

If the load to an op amp is primarily capacitive, it is not necessary to use a low resistance output stage to achieve satisfactory performance because large output currents are only required under dynamic conditions. The difficulty with a capacitive load for the two-stage op amp is that it destroys the Miller compensation and eventually causes the op amp to become unstable if C_L is too large or the closed-loop gain of the op amp approaches unity. In this case, the cascode architectures shown in Fig. 6.5-4 and Fig. 6.5-5 are very useful. Consider the BJT cascode op amp of Fig. 6.5-4*b*. The current from the collector of Q1 is mirrored into the collector current of Q7 while the collector current of Q2 is mirrored into the collector current of Q6. These currents are applied to the common-base configuration of Q8 and Q9. Q6 and Q8 and Q7 and Q9 are cascode amplifiers, as will be recognized from Sec. 6.2. The differential currents are combined at the collectors of Q8 and Q9, resulting in a single-ended output voltage, V_O. The important feature of the circuit of Fig. 6.5-4*b* is that the high-impedance point at A in Fig. 6.5-4*a* is no longer present. Since the output resistance is very high, the compensation can be accomplished by a capacitor connected from the output to ground. This means that a large load capacitance, C_L, will simply provide more compensation, keeping the op amp circuit stable. The low-frequency gain of the BJT cascode op amp is similar to that of the two-stage BJT op amp because the gain of the cascode stage is approximately equal to the gain of the inverter stage.

The BJT folded cascode op amp of Fig. 6.5-4*c* uses the same principle as the BJT cascode op amp to eliminate the high-impedance point at A, thus achieving a configuration with the high-impedance point at the output of the op amp. In this architecture, Q1-Q3 and Q2-Q4 form the cascode pairs. It is necessary to use a cascode current mirror (Q7 through Q10) to maintain the high output resistance of this configuration. The folded cascode is useful in acheiving a wide common-mode input voltage range.

In many cases, the two-stage BJT op amp is satisfactory for driving moderate values of C_L because of the higher values of g_m for a BJT. The higher value of g_m pushes the RHP zero away from the origin and keeps C_L from having a strong influence on the stability of the op amp. However, the CMOS cascode configurations of Fig. 6.5-5*b* and *c* are often used because of the low g_m of the MOS devices compared with that of the BJT devices. Another reason for using the cascode architecture is due to PSRR performance. It can be shown that variations in the upper power supply for the two-stage architecture couple through the base-emitter of Q5 (gate-source of M5) and C_c to the output, resulting in poor PSRR performance. The cascode configurations do not have this problem, which was another motivation for their development.

To understand the performance of the cascode op amp configuration in more detail, consider the folded cascode CMOS op amp of Fig. 6.5-5*c*. Figure 6.5-9*a* shows a small signal model for this op amp. The bulk effects of all devices whose source is not on ground have been ignored. r'_{in}, r'_{out} and the current-controlled current source, i, represent the cascode mirror consisting of M7 through M10 (see Sec. 5.4). Figure 6.5-9*b* is a simplified version of Fig. 6.5-9*a* using the technique

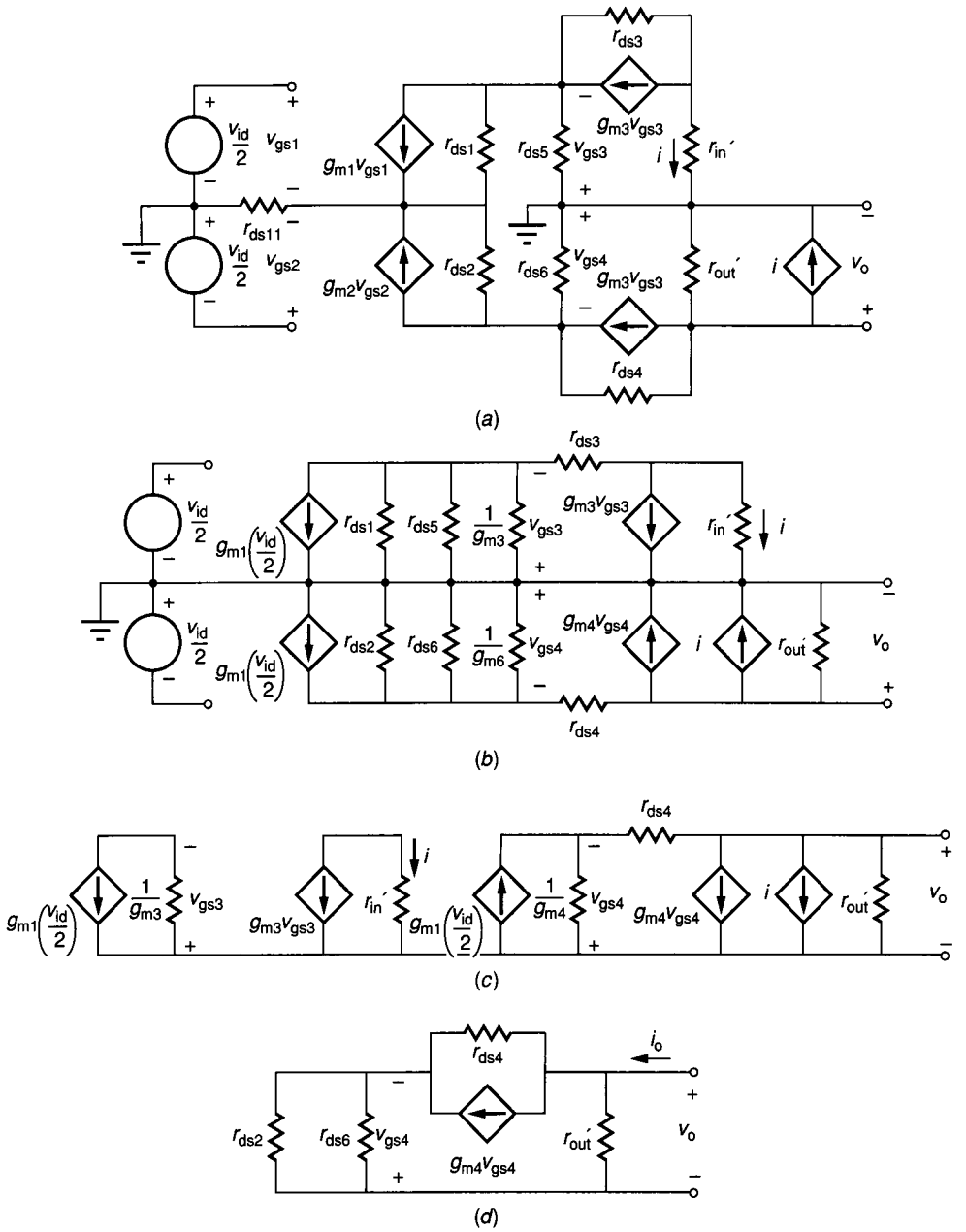


FIGURE 6.5-9
(*a*) Small signal model of the CMOS folded cascode op amp, (*b*) Simplification of (*a*), (*c*) Approximate model of (*b*), (*d*) Model for calculating the output resistance.

illustrated in Sec. 6.3 for the differential amplifier of Fig. 6.3-4*c*. Neglecting r_{ds} as compared to $1/g_m$ results in the approximate small signal model of the circuit of Fig. 6.5-5*c* shown in Fig. 6.5-9*c*. Analysis of this circuit shows that the low-frequency voltage gain is

$$\frac{v_o}{v_{id}} = A_o \simeq g_{m1} r'_{out} \simeq g_{m1} g_{m8} r_{ds8} r_{ds10} \tag{6.5-42}$$

where r'_{out} was given by simplication of Eq. 5.3-10. Assuming that all *W/L* ratios are unity, $K'_N = 2K'_P = 25\ \mu A/V^2$, $\lambda_N = \lambda_P = 0.01\ V^{-1}$, and $I_{D1} = I_{D2} = 5\ \mu A$, the dc current in M5 through M9 (M6 through M10) is 50 μA and the low-frequency gain, A_o, is 22,361. The output resistance of the circuit of Fig. 6.5-5*c* can be found with the assistance of the circuit of Fig. 6.5-9*d*. r_{out} is found as

$$\begin{aligned} r_{out} &= r'_{out} \,||\, r_{ds4}\left[1 + (1 + g_{m4} r_{ds4}) \frac{r_{ds2} r_{ds4}}{r_{ds2} + r_{ds4}}\right] \\ &\simeq (g_{m8} r_{ds8} r_{ds10}) \,||\, [(g_{m4} r_{ds4})(r_{ds2} \,||\, r_{ds4})] \end{aligned} \tag{6.5-43}$$

Using these values for the folded cascode CMOS op amp, we find that r_{out} is equal to 78.3 MΩ.

The frequency performance of the folded cascode CMOS op amp is simply given as

$$\frac{V_O(s)}{V_{ID}(s)} \simeq \frac{A_o \omega_I}{s + \omega_I} = \frac{GB}{s + \omega_I} \tag{6.5-44}$$

where ω_I is given as

$$\omega_I = \frac{1}{R_{out} C_L} \tag{6.5-45}$$

C_L is the total capacitance attached to the output of the folded cascode CMOS op amp. The slew rate is found as

$$SR = \frac{I}{C_L} \tag{6.5-46}$$

where I is I_{D11} of Fig. 6.5-5*b* or *c*. The performance of this op amp can be evaluated with the assistance of Eqs. 6.5-42 through 6.5-46. Continuing with the preceding assumptions, we find that for GB = 5 MHz, the value of C_L is 9.1 pF. This gives a slew rate of about 1.1 V/μs. Of course, the *W/L* values can be used to modify the design to achieve different specifications.

One of the disadvantages of this architecture is that the output signal swing is limited by the cascode configuration. This swing limitation can be alleviated using the technique described for cascode current mirrors (see Fig. 5.4-10). A practical implementation of the folded cascode CMOS op amp is shown in Fig. 6.5-10.[2] With ±5 V power supplies, the op amp has an output swing of ±4.1 V. It has a low-frequency gain of 5000, a GB of approximately 5 MHz, and a PSRR in the range of 60–70 dB. The input offset voltage, V_{OS}, is ±6 mV. In the basic

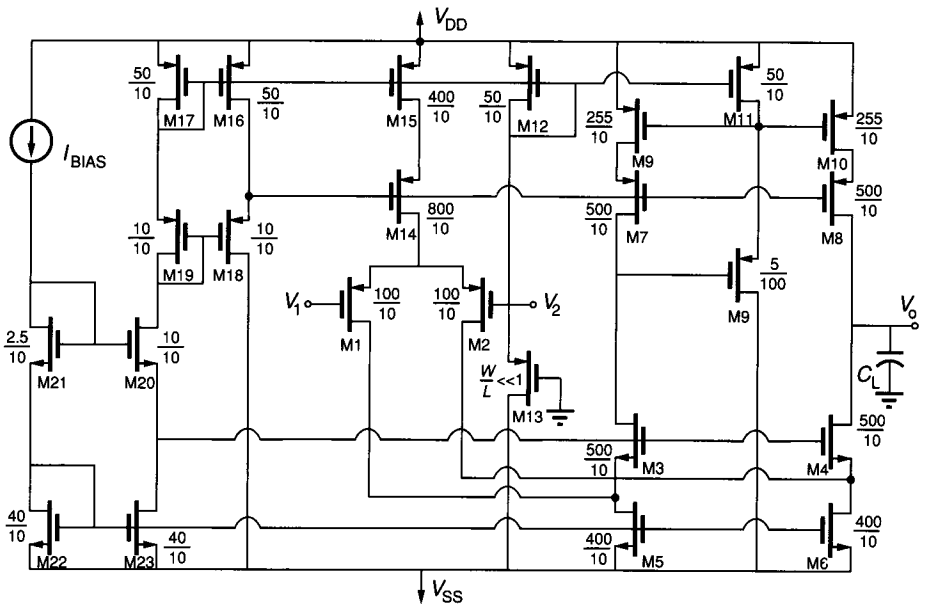


FIGURE 6.5-10
Folded cascode CMOS op amp design. *W/L* values are in microns.

folded cascode architecture of Fig. 6.5-5*c*, the operating region of all devices can be defined by external voltages so that ratio constraints are not necessary. In choosing the *W/L* values, one of the primary considerations is to increase the signal swings. The *W/L* values of the circuit of Fig. 6.5-10 correspond to $K'_N = 23.6\ \mu A/V^2$, $K'_P = 5.84\ \mu A/V^2$, $V_{TN} = 0.79$ V, $V_{TP} = -0.52$ V, $\gamma_N = 0.526\ V^{1/2}$, $\gamma_P = 0.67\ V^{1/2}$, $\lambda_N = 0.0207\ V^{-1}$, and $\lambda_P = 0.0121\ V^{-1}$.

6.5.5 Op Amps with an Output Stage

None of the op amps considered so far are capable of driving low values of load resistance. If the application requires a low output resistance, then the two-stage op amp can be followed with an output amplifier by use of the concepts of Sec. 6.4. Figure 6.5-11 shows the combination of the BJT two-stage op amp of Fig. 6.5-4*a* with the output stage of Fig. 6.4-14*b* to obtain an op amp with the ability to drive a low value of R_L. Q6 and Q7 are used to determine the operating current in the push-pull output transistors, Q8 and Q9. One of the difficulties in adding an output stage is to decide whether or not to include the output stage within the Miller compensation. The two choices are indicated in Fig. 6.5-11 by C_{c1} and C_{c2}. C_{c2} is less desirable because the pole due to the output stage will be large and close to GB, resulting in three poles inside the compensation loop. The Miller compensation method does not work well in this situation because complex conjugate poles can be created. The ability of the output stage to drive

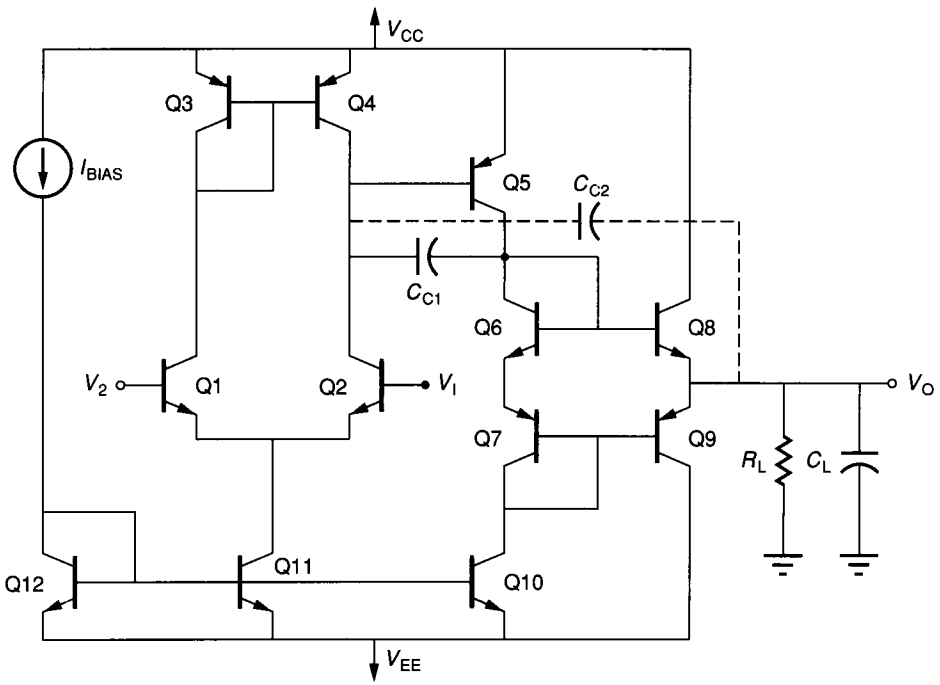


FIGURE 6.5-11
BJT two-stage op amp with a push-pull output stage.

a load resistance has been discussed in the preceding section. Further information can be found in the references.[3–7]

Figure 6.5-12*a* shows a two-stage CMOS op amp with an output stage similar to that of Fig. 6.4-14*a*. The compensation capacitor does not include the output stage and uses a nulling resistor, R_z, to achieve good stability properties. The ability to sink or source current is determined by the second stage of the op amp (M5). The bias current in the output devices (M8 and M9) should be chosen to reduce the crossover distortion and keep the quiescent dissipation low. Also, the bias current in the output devices will determine the small signal value of output resistance. The output swing of this op amp will be limited due to the body effects, causing V_T to increase as the positive or negative rail is approached by the output voltage.

Figure 6.5-12*b* shows use of the substrate BJT to create an output stage. This technique will provide low small signal output resistance because of the large value of g_m for the BJT. Unfortunately, the BJT suffers from the inability to source current for large positive output swings. Because the output devices are of a different type and in a different configuration (emitter follower and common source), the sourcing and sinking currents will be difficult to match. In addition, this configuration will create appreciable distortion.

A better solution to the output stage problem for the CMOS op amp is to couple the circuits of Fig. 6.4-15*a* and Fig. 6.5-10 resulting in the

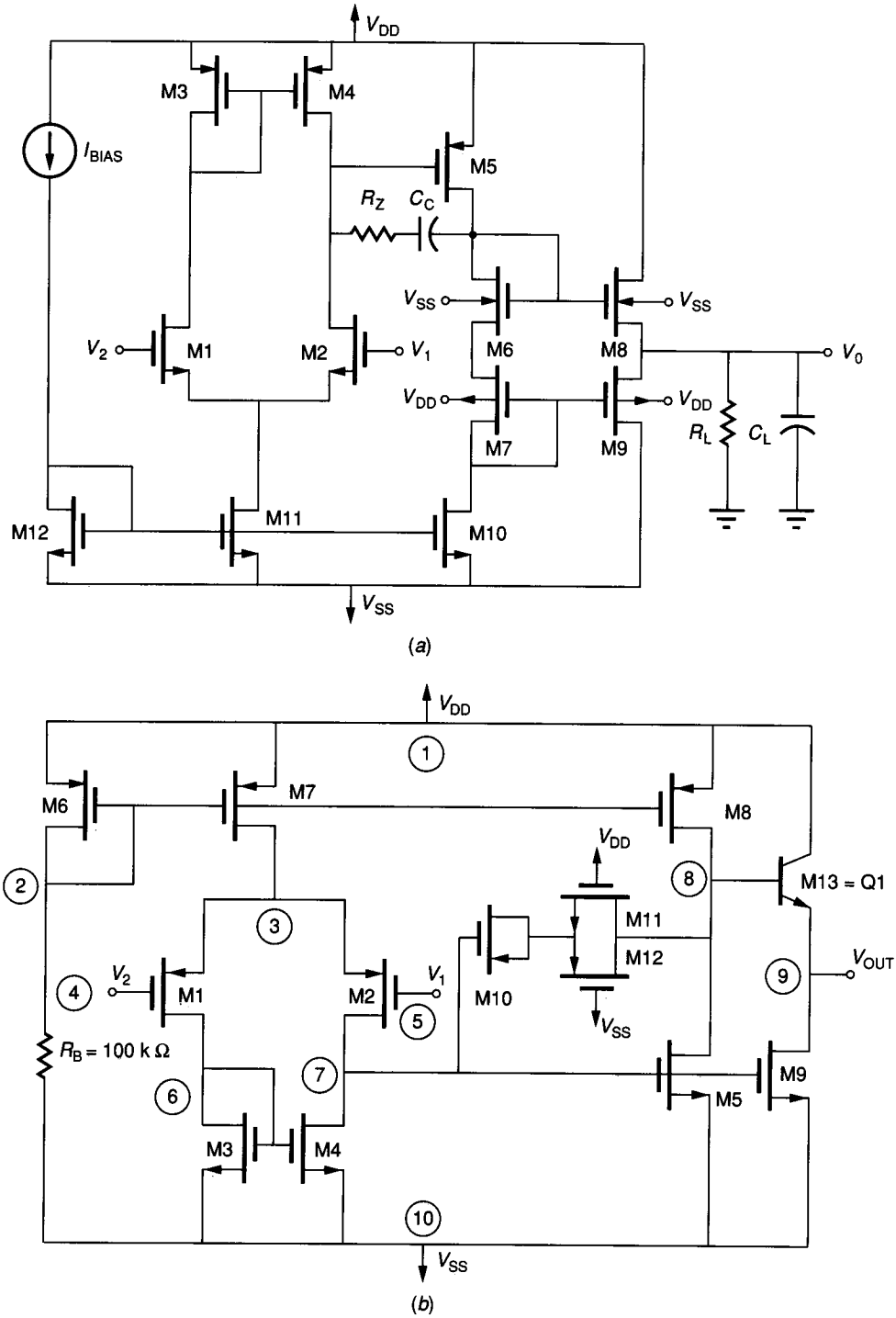


FIGURE 6.5-12
(*a*) CMOS two-stage op amp with a push-pull output stage, (*b*) CMOS two-stage op amp with a substrate BJT used in the output stage.

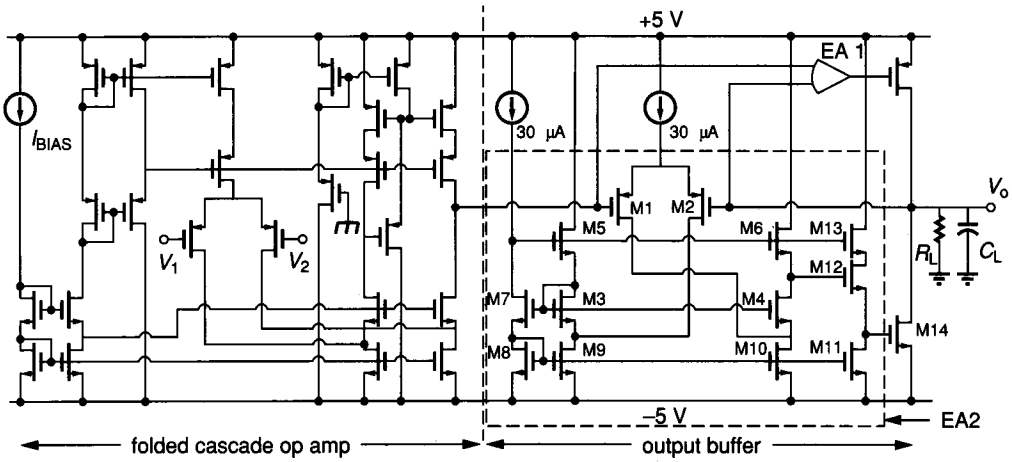


FIGURE 6.5-13
Folded cascode CMOS op amp with output buffer.

arrangement of Fig. 6.5-13. Only one of the error amplifiers is shown in this figure. The resulting CMOS op amp has an output resistance of 300 Ω and achieves an output signal swing of approximately −4.3 V to +3.5 V for ±5 V power supplies and a load of 2000 Ω and 100 pF. Total power dissipation of the op amp and buffer stage is 5 mW for ±5 V supplies.

6.5.6 Simulation and Measurement of Op Amps

It has been mentioned that the next step after developing a first-cut design of an op amp is simulation. This is a key step in the successful design of an op amp. Another important step is the actual measurement of the op amp when it is fabricated. Because the considerations necessary for the simulation and testing are so closely related, they will be considered simultaneously. One of the more important characterizations of op amp performance is operation in the open-loop mode. However, as it is difficult to measure an op amp in its open-loop mode, it is also difficult to simulate an op amp in the open-loop mode. The reason for this difficulty is the high differential gain of the op amp. Figure 6.5-14 shows how this step might be performed. V_{off} is an external voltage whose value is

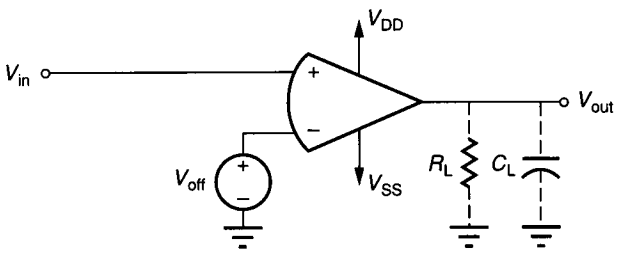


FIGURE 6.5-14
Open-loop mode with offset compensation.

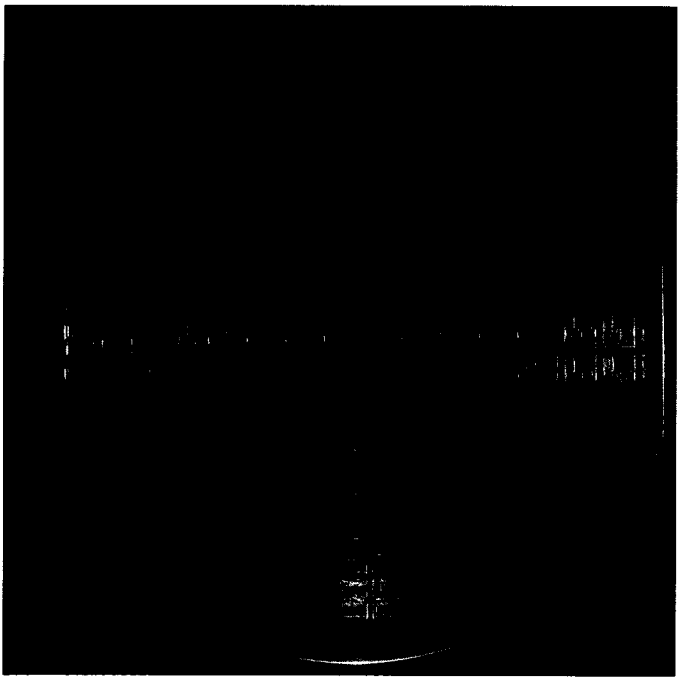


PLATE ONE Wafer photo — Motorola 68000 Family Microprocessor
(Photo courtesy of Motorola, Inc.)

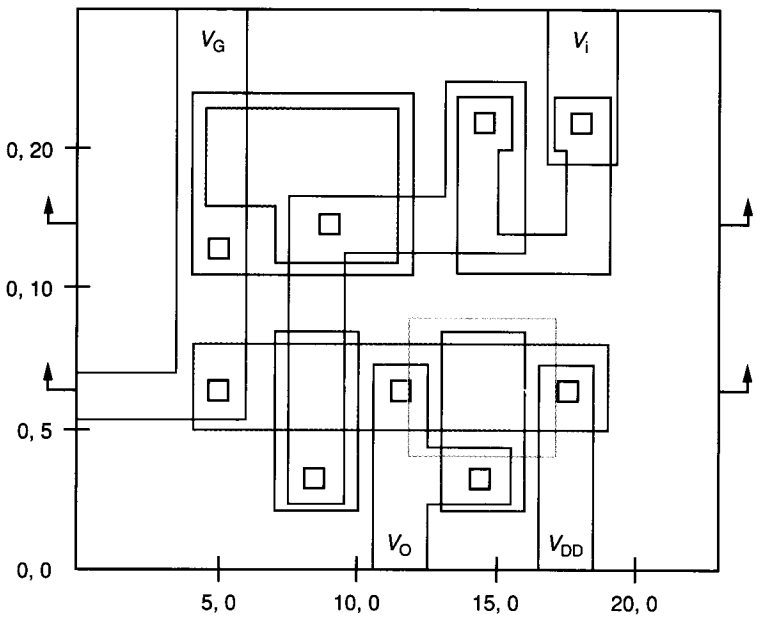
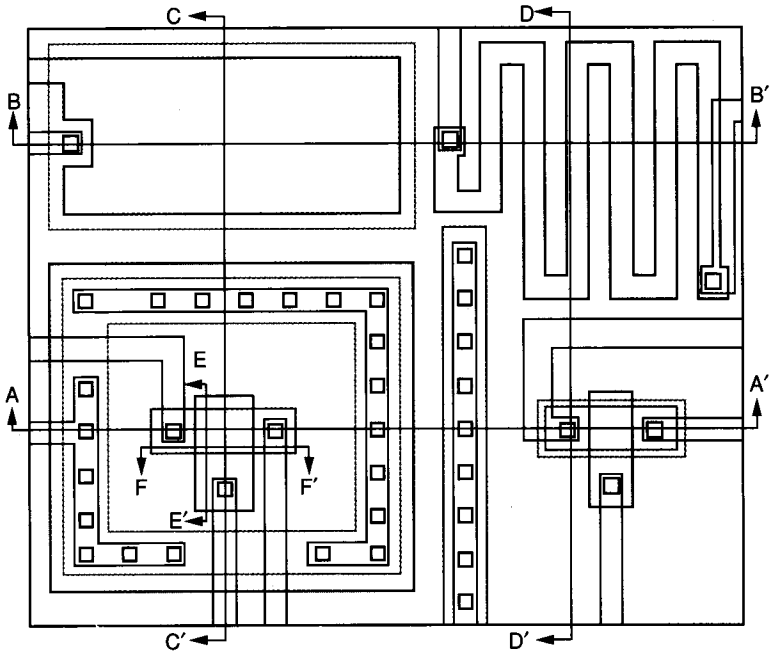
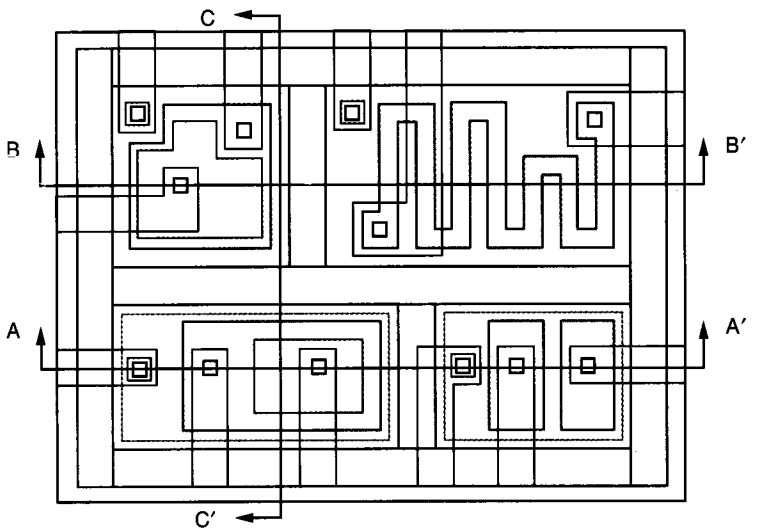


PLATE TWO Layout for NMOS process



Top view (a) Fig. 2b.1a

PLATE THREE Layout for CMOS process



Top view of Bipolar Die (Fig. 2c.1a)

PLATE FOUR Layout for Bipolar process

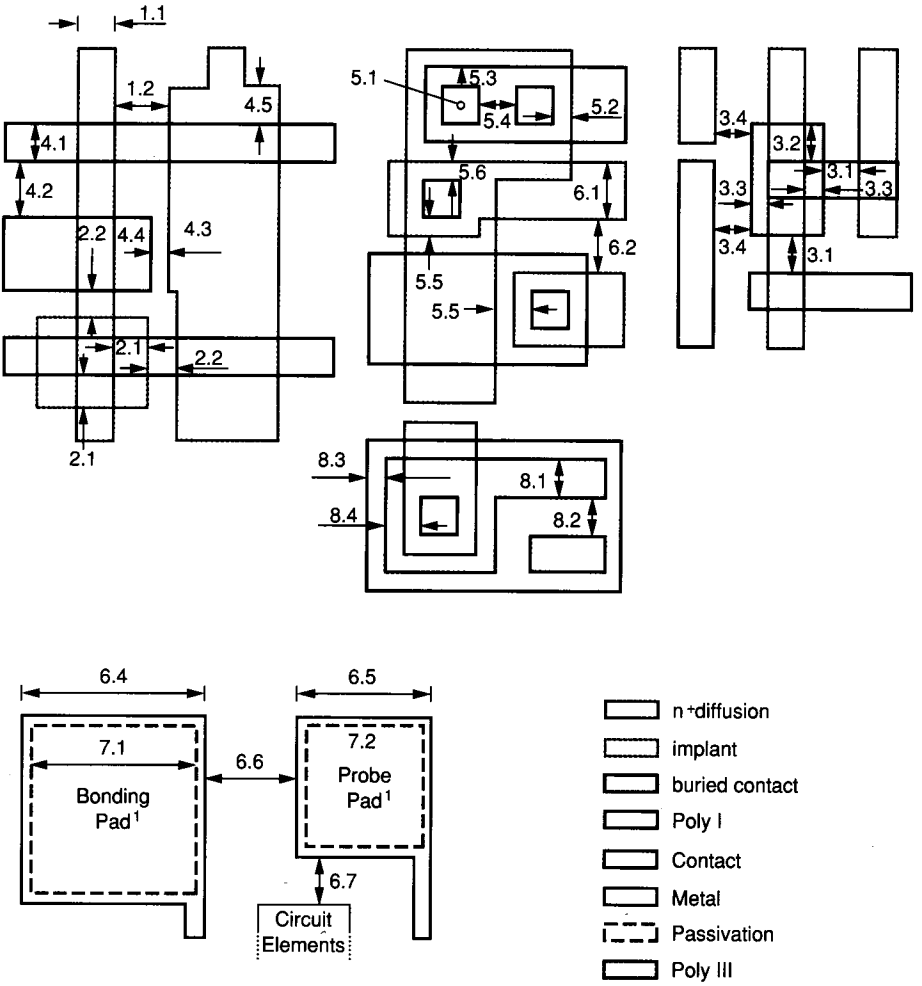


PLATE FIVE Table 2A.3 Graphical interpretation of NMOS design rules of Table 2A.2

[1]Scale for pads is much smaller than scale for other features depicted in this figure.

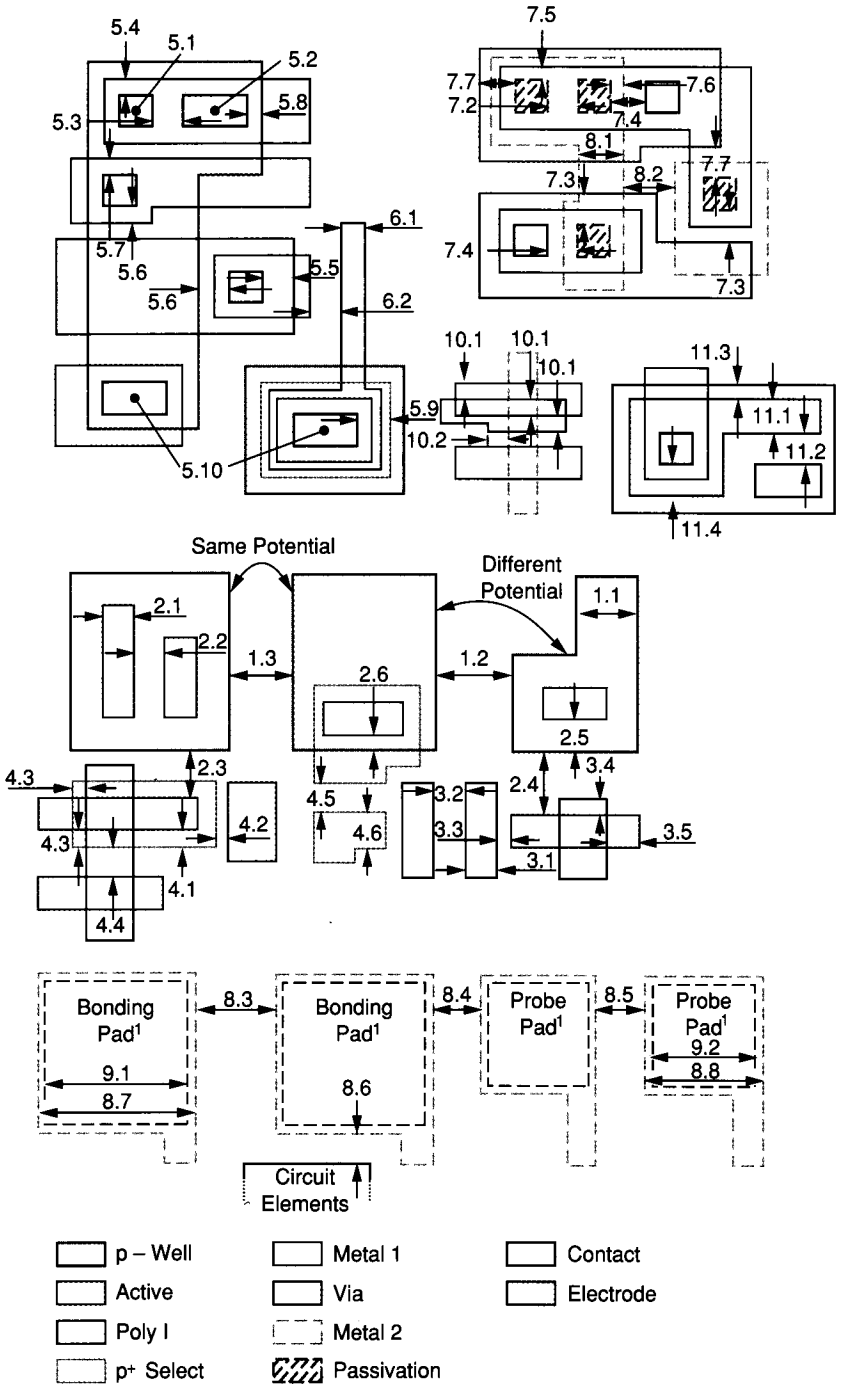


PLATE SIX Table 2B.3 Graphical interpretation of CMOS design rules of Table 2B.2

[1] Scale for pads is much smaller than scale for other features depicted in this figure.

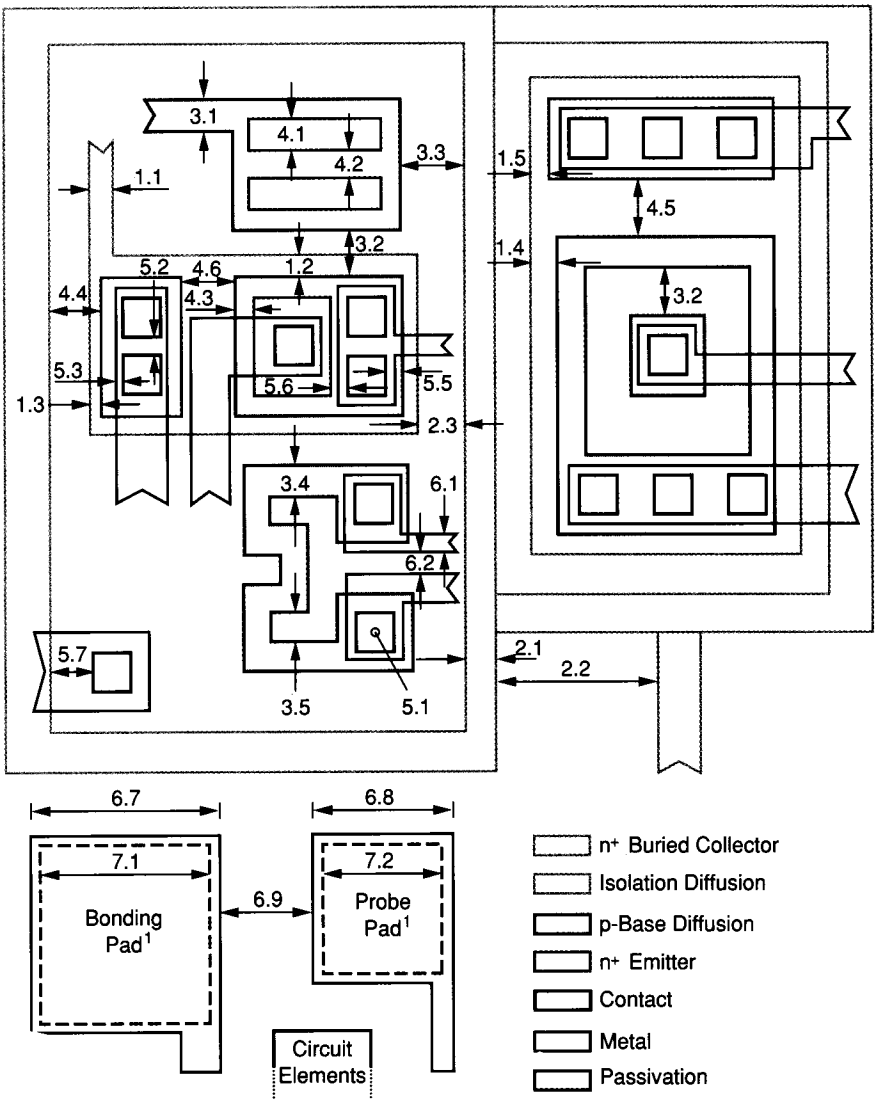


PLATE SEVEN Table 2C.3 graphical interpretation of Bipolar design rules of Table 2C.2

[1] Scale for pads is much smaller than scale for other features depicted in this figure.

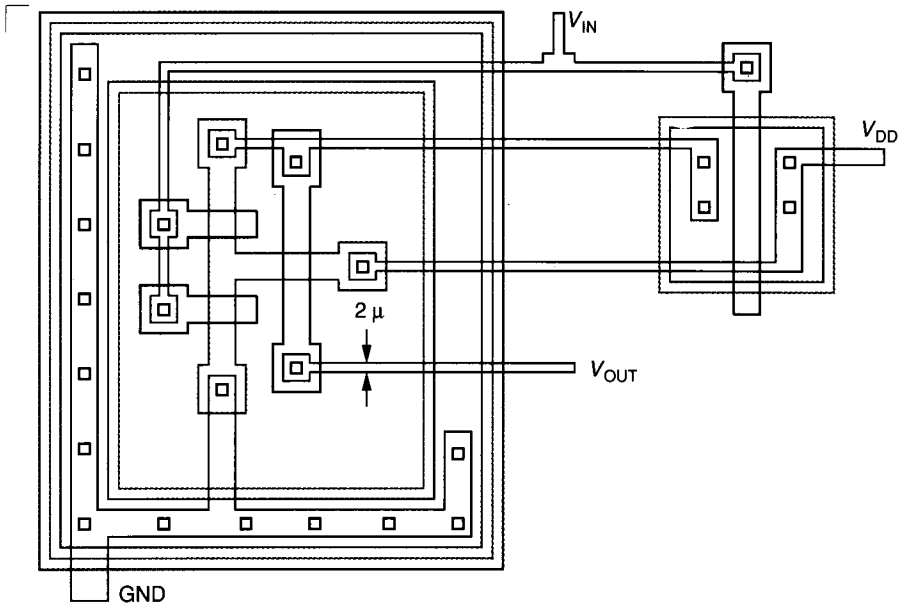


PLATE EIGHT Layout of Schmitt Trigger circuit (see Problem 2.20)

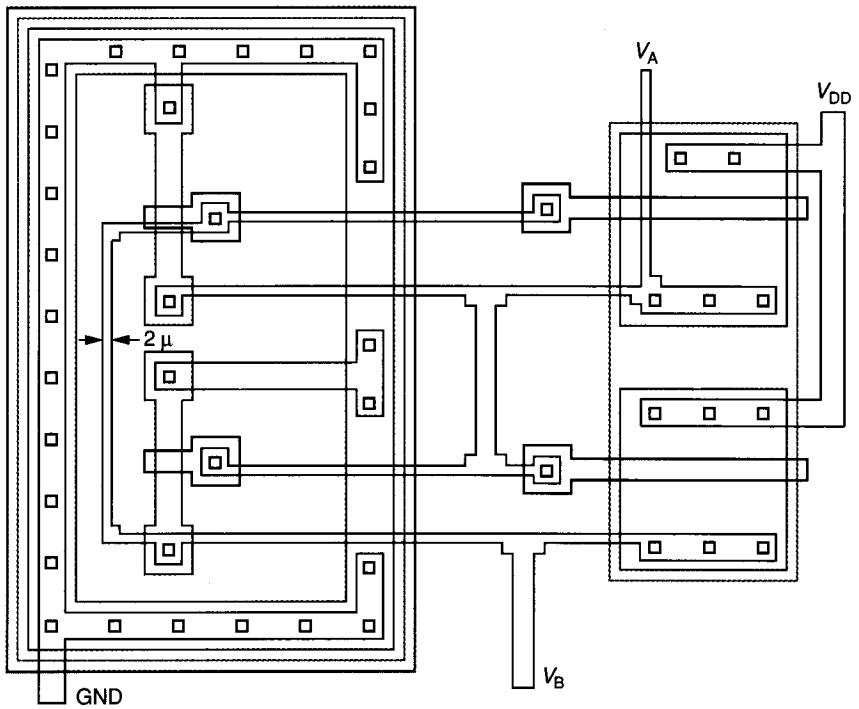


PLATE NINE Layout of latch circuit (see Problem 2.23)

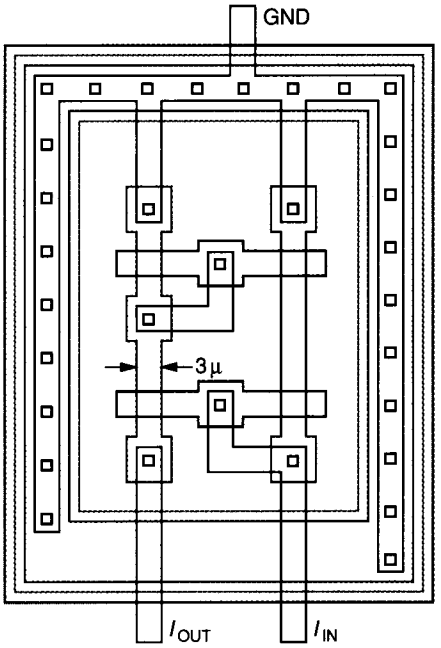


PLATE TEN Layout of common source amplifer (see Problem 2.22)

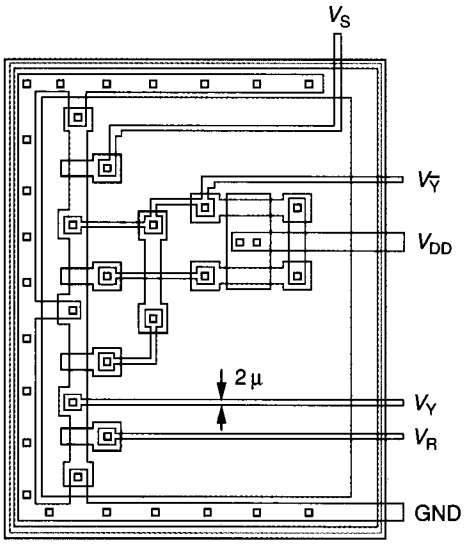


PLATE ELEVEN Layout of flip flop (see Problem 2.23)

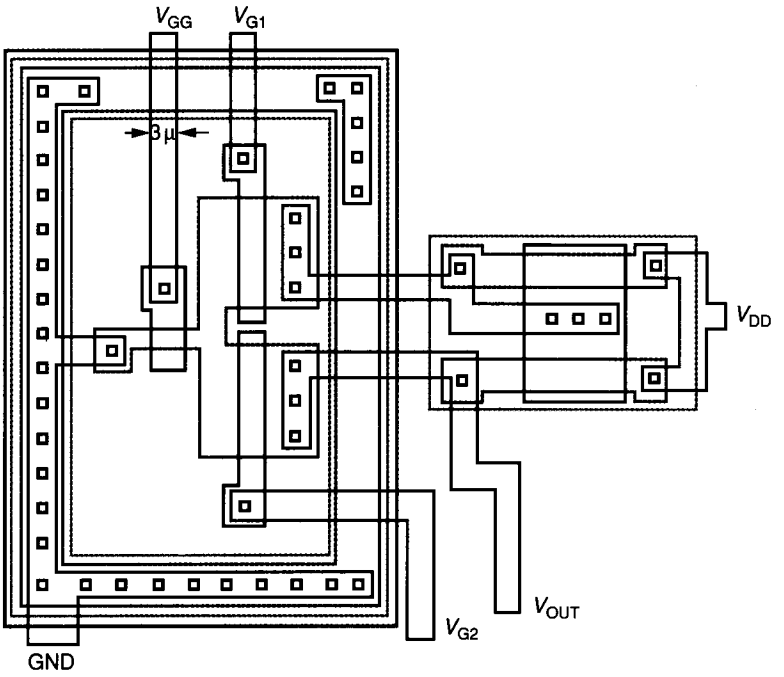


PLATE TWELVE Layout of differential amplifier with error (see Problem 2.31)

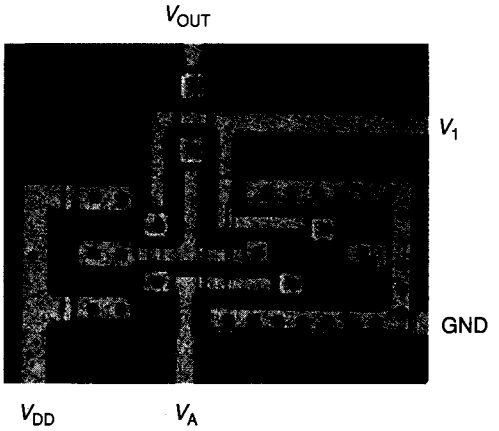


PLATE THIRTEEN Die photo of logic circuit (see Problem 2.26)

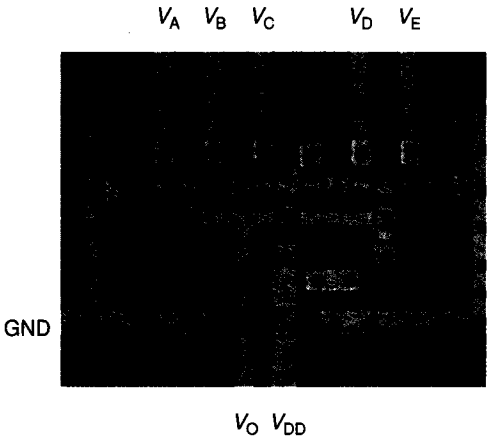


PLATE FOURTEEN Die photo of logic circuit (see Problem 2.26)

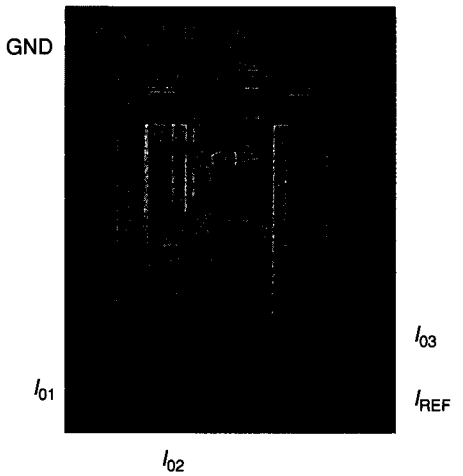


PLATE FIFTEEN Die photo of current source (see Problem 2.27)

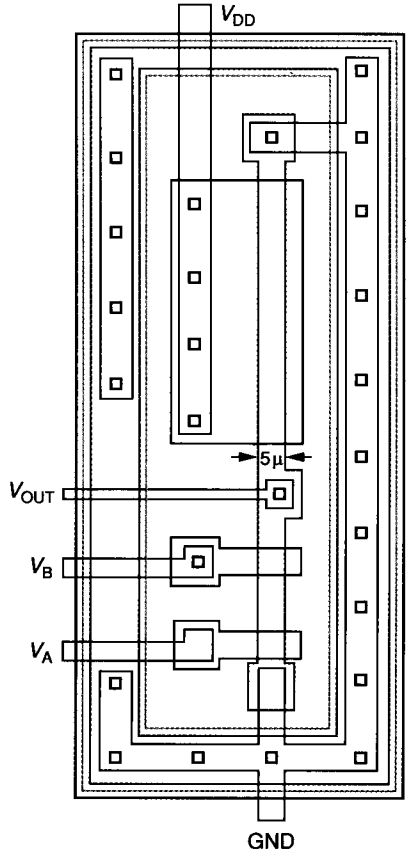


PLATE SIXTEEN Layout of NAND circuit with error (see Problem 2.29)

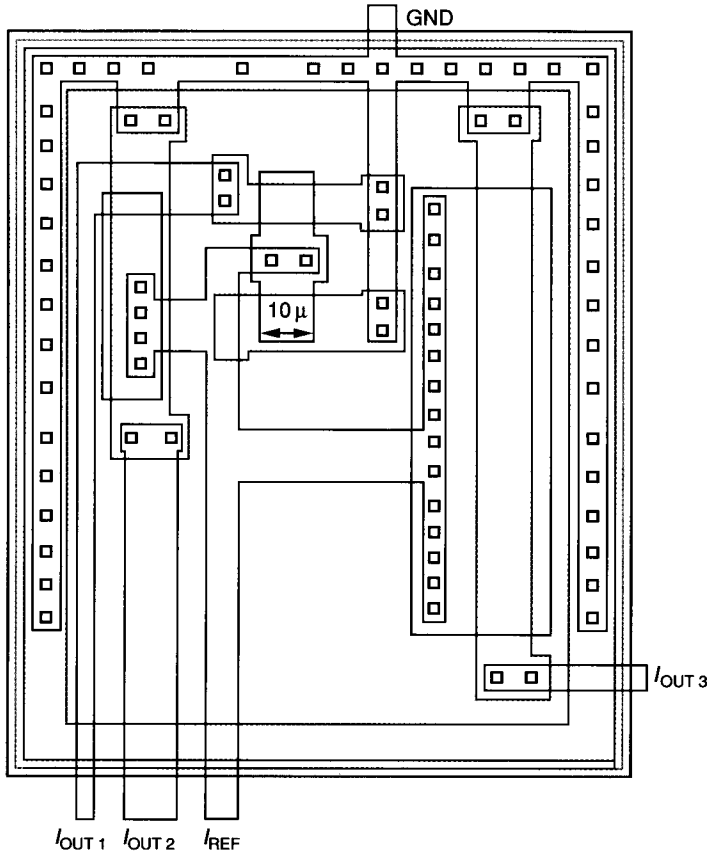


PLATE SEVENTEEN Layout of current source with error (see Problem 2.30)

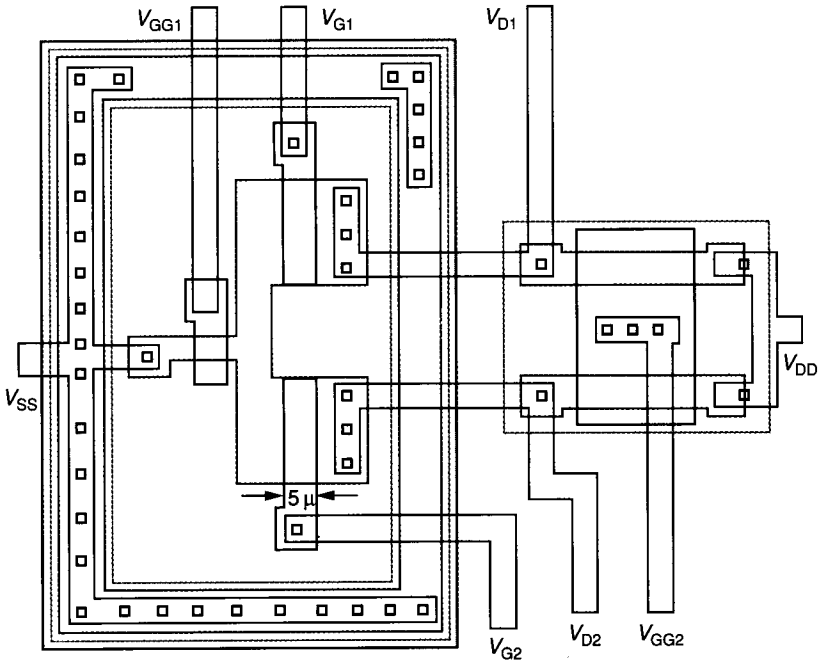


PLATE EIGHTEEN Layout of differential amplifier with error (see Problem 2.31)

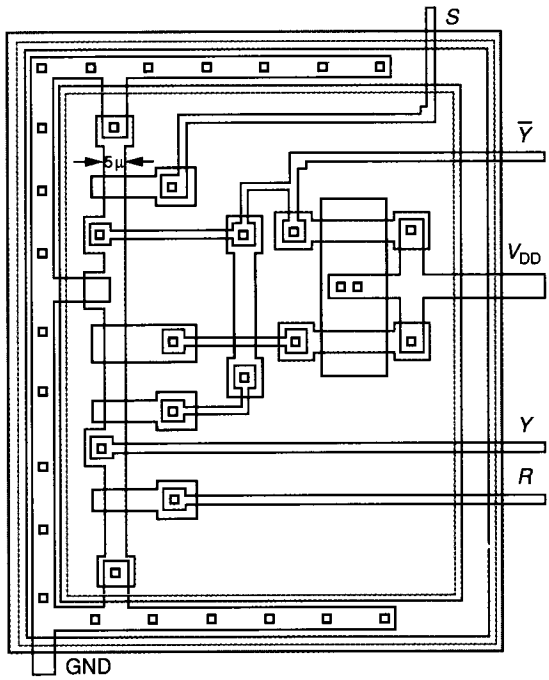


PLATE NINETEEN Layout of flip-flop with error (see Problem 2.32)

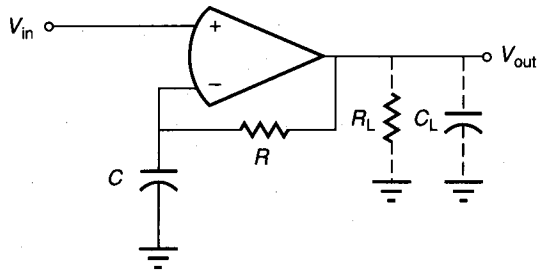


FIGURE 6.5-15
A method of measuring open-loop characteristics with dc bias stability.

adjusted to keep the dc value of V_{OUT} between the power supply limits. Without V_{off}, the op amp output will be at the positive or negative power supply for either the measurement or simulation case. The resolution necessary to find the correct value of V_{off} usually escapes the novice designer. It is necessary to find V_{off} to the accuracy of the magnitude of the power supply voltage divided by the low-frequency differential gain (typically in the range of millivolts).

The approach proposed in Fig. 6.5-14 to measure the open-loop gain is only practical for simulation. A better method of measuring the open-loop gain is shown in the circuit of Fig. 6.5-15. In this configuration, it is necessary to select the reciprocal *RC* time constant to be about 10 to 100 times less than the anticipated dominant pole of the op amp. Under these conditions, the op amp has total dc feedback, which stabilizes the bias. The dc value of V_{OUT} will be exactly the dc value of V_{IN}. The true open-loop frequency response characteristics will not be observed until the frequency is approximately 10 times $1/RC$. Above this frequency, the ratio of V_{OUT} to V_{IN} is essentially the open-loop gain of the op amp. This method works well for both simulation and measurement.

Simulation or measurement of the open-loop configuration of the op amp will characterize the open-loop transfer curve, the open-loop output swing limits, the phase margin, the dominant pole, the unity-gain bandwidth, and other open-loop characteristics. The designer should connect the anticipated loading at the output in order to get meaningful results. In some cases where the open-loop gain is not too large, it can be measured by applying v_{in} in Fig. 6.5-16 and measuring v_{out} and v_i. In this configuration, one must be careful that R is large enough not to cause a dc current load on the output of the op amp.

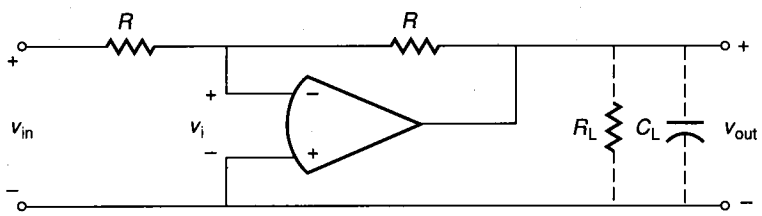


FIGURE 6.5-16
Configuration for simulating the open-loop frequency response for moderate-gain op amps.

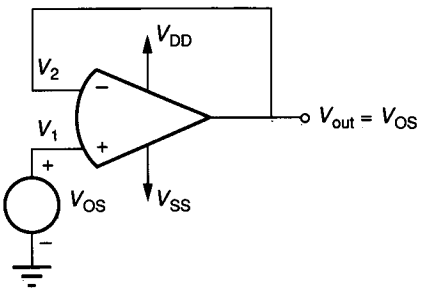


FIGURE 6.5-17
Configuration for measuring the input offset voltage.

The dc input offset voltage, V_{OS}, can be measured using the circuit of Fig. 6.5-17. If the dc input offset voltage is too small, it can be amplified by the use of a resistor divider in the negative feedback path. Figure 6.5-17 is also a good configuration for measuring or simulating the input common-mode range. Figure 6.5-18 shows the anticipated unity-gain transfer characteristic of the op amp in Fig. 6.5-17, illustrating the input common-mode range.

The common-mode gain is most easily simulated using the circuit of Fig. 6.5-19. It is seen that if V_{off} fails to keep the op amp in the linear region, this measuring configuration will fail. An alternate method of measuring the common-mode gain is given in Fig. 6.5-20. This circuit can be used to measure the CMRR, which will also give the common-mode gain. The method involves a sequence of two steps. The first step is to set V_{HH} to V_{HH} + 1 V, V_{LL} to V_{LL} + 1 V, and V_{out} to 1 V by applying -1 V to the input designated as $-V_{out}$. This is equivalent to applying a common-mode input signal of 1 V to the amplifier with the nominal supply values. The value at V_{OFF} is measured and designated as V_{OFF1}. Next, V_{HH} is set to $V_{HH} - 1$ V, V_{LL} to $V_{LL} - 1$ V, and V_{out} to -1 V

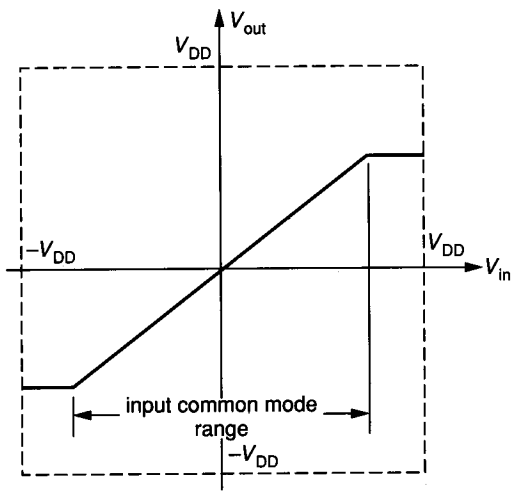


FIGURE 6.5-18
Unity-gain transfer function of the op amp.

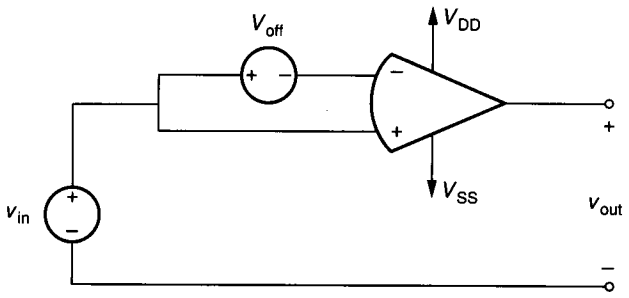


FIGURE 6.5-19
Configuration for simulating the common-mode gain.

by applying +1 V to the input designated as $-V_{out}$. V_{OFF} is measured and designated as V_{OFF2}. The CMRR can be found by

$$\text{CMRR} = \frac{2000}{|\, V_{OFF1} - V_{OFF2} \,|} \tag{6.5-47}$$

This measurement is a spot measurement and must be modified to obtain the frequency response of the CMRR. The modification involves placing small sinusoidal signals of the proper phase in series with the power supplies.

The configuration of Figure 6.5-20 can also be used to measure the PSRR. First, set V_{HH} to V_{HH} + 1 V and V_{out} to 0 V by grounding $-V_{out}$. In this case, V_i is the input offset voltage for V_{HH} + 1 V. Measure V_{OFF} under these conditions, and designate it as V_{OFF3}. Next, set V_{HH} to V_{HH} − 1 V and V_{out} to 0 V, and measure V_{OFF}, designated as V_{OFF4}. The PSRR of the V_{HH} supply is given as

$$\text{PSRR of } V_{HH} = \frac{2000}{|\, V_{OFF3} - V_{OFF4} \,|} \tag{6.5-48}$$

For the PSRR of V_{LL}, change V_{LL} and keep V_{HH} constant while V_{out} is at 0 V.

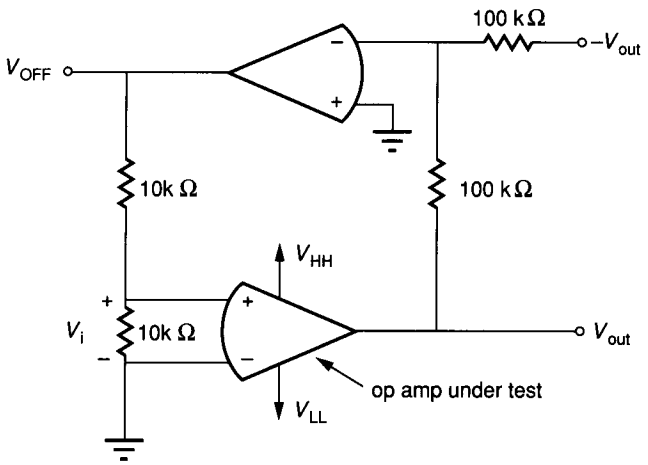


FIGURE 6.5-20
Circuit used to measure CMRR and PSRR.

The circuit of figure 6.5-17 can also be used to measure the PSRR of the positive or negative power supply. Assume that the output voltage can be expressed as

$$V_{out} = A_{vd}(V_1 - V_2) + A_{dd}V_{dd} \tag{6.5-49}$$

where A_{dd} is the small signal voltage gain from V_{dd} to V_{out}. It can be shown that

$$V_{out} = \frac{A_{dd}V_{dd}}{1 + A_{vd}} \simeq \frac{A_{dd}}{A_{vd}}V_{dd} = \frac{V_{dd}}{\text{PSRR}} \tag{6.5-50}$$

if $A_{vd} > 1$. Therefore, applying an ac signal V_{dd} in series with V_{DD} of Fig. 6.5-17 and measuring (or simulating) V_{out} will give the value of 1/PSSR.

The last configuration we will consider is for the large signal transient response. Figure 6.5-21*a* shows a configuration suitable for measuring the transient response of the op amp. Figure 6.5-21*b* shows a typical transient response. Both the positive and negative slew rates and the positive and negative settling times can be obtained from this configuration.

Other configurations not considered here include tests for noise, tolerances, process parameter variations, temperature, etc. The primary objective of any configuration is to keep the op amp in the desired region of operation and to maximize the accuracy of the measurement/simulation data.

The design of BJT and CMOS op amps has been introduced in this section. The basic two-stage architectures were introduced. The first-cut design of BJT and CMOS two-stage op amps was illustrated. This step should be followed by an extensive simulation of the design and the optimization of its performance. The CMOS two-stage op amp is unable to drive large capacitive loads, which led to the introduction of the cascode architectures. An example of a first-cut design for a CMOS folded cascode op amp was presented. This was followed by the addition of an output stage to permit the op amp to drive low resistive loads. Finally, the configuration and techniques useful in simulating and measuring the performance of op amps has been discussed.

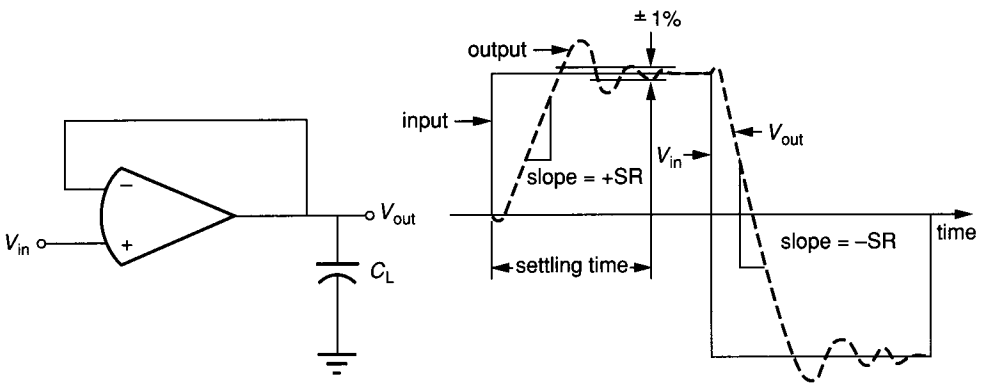


FIGURE 6.5-21
Measurement/simulation of slew rate and settling time.

The reader should be cautioned that the material presented was selected to give an appreciation for, and an introduction to, the subject of integrated circuit op amp design. The design of an actual op amp may deviate from the simplified examples considered in this section. If the reader is faced with the task of designing an op amp for a sophisticated application, this material is a good starting place. It should be followed by a careful reading of the technical literature—in particular, pertinent articles in the *IEEE Journal of Solid State Circuits* and some of the references cited in this section.

6.6 COMPARATORS

In many signal processing applications, the ability to compare two signals and identify which is larger is very important. A *comparator* is a circuit that compares one analog signal with another. The output of the comparator depends on which input signal is larger. Figure 6.6-1 shows the symbol for a comparator. We note that it has two inputs and one output.

6.6.1 Characterization of Comparators

The ideal operation of the comparator is illustrated by Fig. 6.6-2. In Fig. 6.6-2*a*, a noninverting comparator is shown. This characteristic can be described as

$$V_{OUT} = \begin{cases} V_{OH} & V_P \geq V_N \\ V_{OL} & V_P < V_N \end{cases} \tag{6.6-1}$$

where V_{OH} is the upper limit and V_{OL} is the lower limit of the output voltage of the comparator. The comparator of Fig. 6.6-2*a* is called *noninverting* because the output goes from the low state to the high state when the voltage V_P becomes larger than V_N. Figure 6.6-2*b* shows an inverting comparator. This type of comparator can be described as

$$V_{OUT} = \begin{cases} V_{OL} & V_P \geq V_N \\ V_{OH} & V_P < V_N \end{cases} \tag{6.6-2}$$

where the output goes from the high state to the low state when the voltage V_P becomes larger than V_N.

The comparator characteristics of Fig. 6.6-2 are ideal in the sense that they require the comparator to have infinite gain during the output transition. Figure

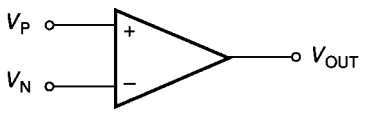


FIGURE 6.6-1
Circuit symbol for a comparator.

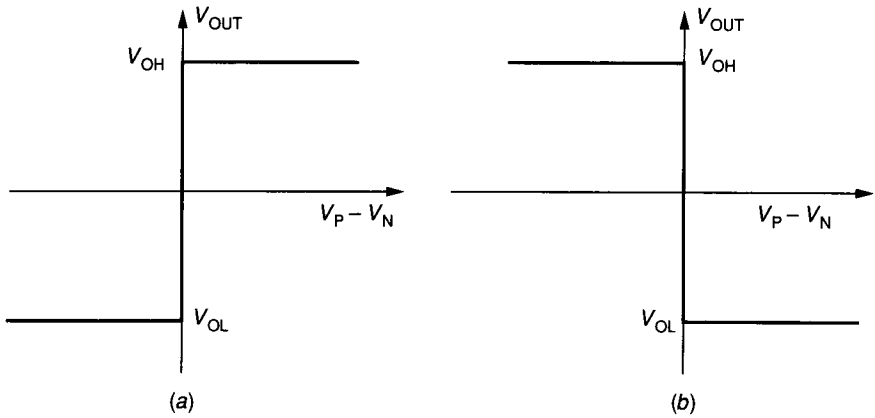


FIGURE 6.6-2
Ideal voltage transfer characteristics of: (*a*) A noninverting comparator, (*b*) An inverting comparator.

6.6-3 shows the transfer characteristics for comparators that do not have infinite gain. The noninverting comparator is described by

$$V_{OUT} = \begin{cases} V_{OH} & (V_P - V_N) > V_{IH} \\ A_v(V_P - V_N) & V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OL} & (V_P - V_N) < V_{IL} \end{cases} \tag{6.6-3}$$

where V_{IL} and V_{IH} represent the values of $(V_P - V_N)$ at which the output is at V_{OL} and V_{OH}, respectively, as $| V_P - V_N |$ is increased from zero. The inverting comparator is shown in Fig. 6.6-3*b* and is described as

$$V_{OUT} = \begin{cases} V_{OL} & (V_P - V_N) > V_{IH} \\ -A_v(V_P - V_N) & V_{IL} \leq (V_P - V_N) \leq V_{IH} \\ V_{OH} & (V_P - V_N) < V_{IL} \end{cases} \tag{6.6-4}$$

The performance of a comparator can be characterized by its (1) resolving capability or threshold sensing, (2) input offset voltage, (3) speed or propagation delay time, and (4) input common-mode range. The *resolving capability* of a comparator is defined in terms of Fig. 6.6-3 as $V_{IH} - V_{IL}$. It is easy to see that the resolving capability of a comparator is related to its gain. Assuming that V_{OH} and V_{OL} are fixed by power supply limits, the resolving capability, ΔV , can be expressed as

$$\Delta V = \frac{V_{OH} - V_{OL}}{A_v} \tag{6.6-5}$$

As A_v becomes large, the resolving capability approaches the ideal of Fig. 6.6-2. The input offset voltage, V_{OS}, is the value of voltage applied between the inputs

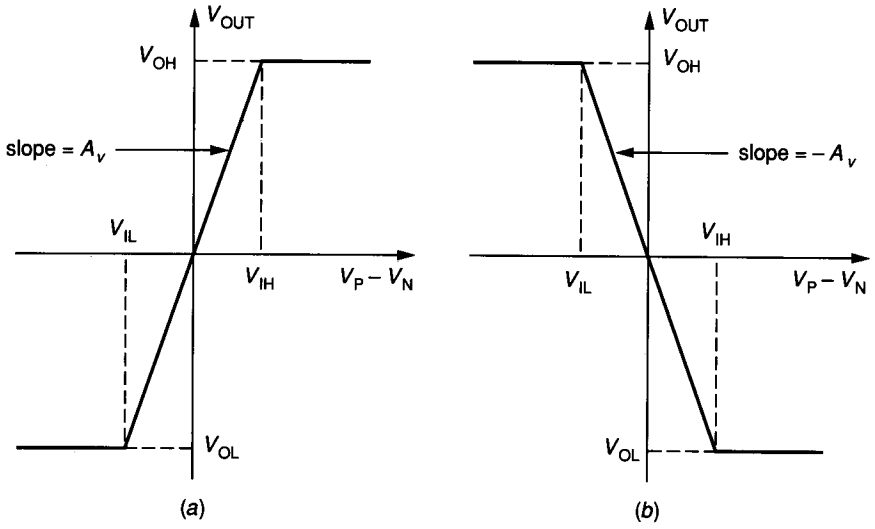


FIGURE 6.6-3
Practical voltage transfer characteristics of: (*a*) A noninverting comparator, (*b*) An inverting comparator.

to make V_{OUT} equal to zero when V_P and V_N are connected together (i.e., the comparator V_{OS} is the same as the op amp V_{OS}). Figure 6.6-4 shows the effect of V_{OS} on the transfer characteristics of the noninverting comparator of Fig. 6.6-3*a*.

The *propagation time* of the comparator is a measure of how quickly the output changes states after the input threshold has been reached. Figure 6.6-5 shows the time domain response of a noninverting comparator. The propagation

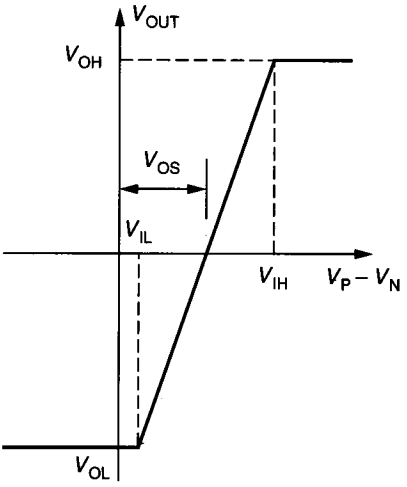


FIGURE 6.6-4
Practical noninverting voltage transfer characteristic with input offset voltage illustrated.

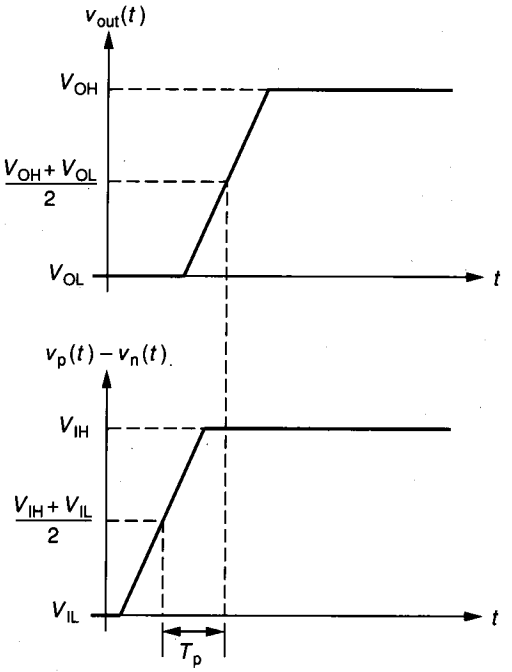


FIGURE 6.6-5
Time response for the practical noninverting comparator.

time, T_p, is the time between when $(V_P - V_N)$ is equal to zero, typically $0.5(V_{IH} + V_{IL})$, and when V_{OUT} is equal to $0.5(V_{OH} + V_{OL})$. This parameter is very important since it determines how many comparisons the comparator can make per unit of time. The propagation delay generally varies as a function of the slope, the amplitude of the input, and its common mode value. A larger input or a steeper slope will generally result in a smaller delay time.

The input common-mode range of the comparator is the range of voltages over which the inputs continue to sense the difference between applied input voltages. The resolving capability and input offset voltage are a function of the common-mode input voltage.

6.6.2 High-Gain Comparators

A comparator can be implemented by three methods: use of a high-gain differential amplifier, use of positive feedback, and charge balancing. The charge balancing comparator uses switches and a clock and functions as a comparator only at discrete periods of time. We will discuss only the first method and show how positive feedback can be used to enhance its performance. Charge balancing comparators are discussed elsewhere.[8,9] A good candidate for a comparator is the differential amplifier presented in Sec. 6.3. The key attribute

of the differential amplifier is its ability to amplify the difference between the inverting and noninverting inputs over a wide common-mode range. As a result, the threshold point, or trip point, can be made independent of process and supply variations to a first order. The transfer curve describing the differential amplifier has been presented in Sec. 6.3. For the CMOS differential amplifier of Fig. 6.3-4*c*, the input common-mode range is given by Eqs. 6.3-40 and 6.3-44. The gain of this differential amplifier is given by Eq. 6.3-36 and was calculated as 103 if $K'_N = 24\ \mu A/V^2$, $W_1/L_1 = 1$, $\lambda_N = \lambda_P = 0.01$, and $I_{SS} = 10\ \mu A$. If it is assumed that the difference between V_{OH} and V_{OL} is 5 V, then the resolving capability is about 32 mV. If W_1/L_1 is increased to 10, the resolving capability is 10 mV. The BJT differential amplifier of Fig. 6.3-11 is a good implementation of a comparator. Because of the larger gain, the resolving capability is better than that of the CMOS differential amplifier of Fig. 6.3-4*c*. Assuming $V_{AN} = 100$ V, $V_{AP} = 50$ V, and $V_{OH} - V_{OL} = 5$ V, then the BJT differential amplifier has a gain of 1333 which gives a resolving capability of 3.75 mV.

The input offset voltage of the differential amplifier is due to the mismatches in the devices. Mismatches of this type are unavoidable and result from imperfections in the process. Offsets can be minimized by using a common-centroid geometry layout. Figure 6.6-6 illustrates a common-centroid geometry for a CMOS differential amplifier. It is also desirable to keep the number of bends and corners in the layout to a minimum for the two devices that must match. Typical offsets in the differential amplifier range from 5 to 15 mV for CMOS and from 3 to 10 mV for bipolar. The input offset voltage can be reduced by using large areas for the devices and by keeping the gate-source voltages small.

The propagation time of the differential amplifier used as a comparator is due to the pole at the output. Using Fig. 6.3-15*b* and ignoring the doublet gives a step response of

$$v_o(t) = V_o\left[1 - \exp\left(\frac{-t}{\tau_2}\right)\right] \tag{6.6-6}$$

where τ_2 is equal to R_2C_2 of Fig. 6.3-15*b* and V_o is the final value of the output. The time at which $v_o(t)$ is 50% of V_o is equal to $0.69\tau_2$. Assuming that the rise time of the input step is zero gives the propagation delay of the differential amplifier comparator as

$$T_p \simeq 0.69\tau_2 = 0.69R_2C_2 \tag{6.6-7}$$

Using the values $R_2 = 1\ M\Omega$ and $C_2 = 0.7$ pF for the CMOS differential amplifier comparator gives a propagation delay of 0.43 μs. Using values of $R_2 = 0.67\ M\Omega$ and $C_2 = 7$ pF for the BJT differential amplifier comparator gives a propagation delay time of 3.23 μs. The load capacitance seen by the differential amplifier comparator will greatly influence the propagation delay time. It will be seen that the propagation delay time may be determined by the large signal response (slew rate) rather than the linear step response.

The gain of most CMOS differential amplifier comparators is too small to give satisfactory resolving capability. In order to increase the gain, we turn to the

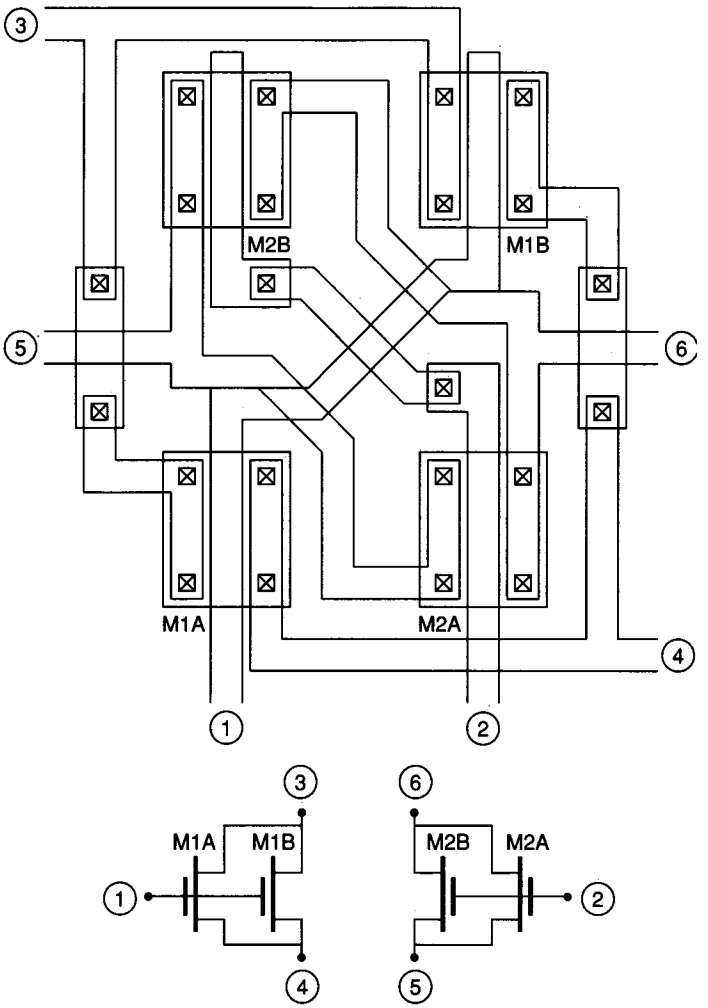


FIGURE 6.6-6
Cross-coupled transistor pair having a common-centroid geometry.

two-stage op amp as a possible architecture for a CMOS comparator. Consider the two-stage CMOS comparator shown in Fig. 6.6-7. It will be assumed that the bulk-source voltages of M1 and M2 are zero (i.e., M1 and M2 are in a floating p-well). This circuit should be designed so that all devices are in saturation. This can be achieved if M1 and M2 are matched and if M3 and M4 are matched and if $V_{SG3} = V_{SG4} = V_{SG5}$. Using these guidelines, we can establish design rules for transistor sizes in this circuit. In order to keep the circuit balanced, M1 and M2, and M3 and M4 must be matched. If the input is balanced, then when V_P and V_N are equal, the current flowing in M7 is split equally through M1 and M2. As a result, we have the following relationships.

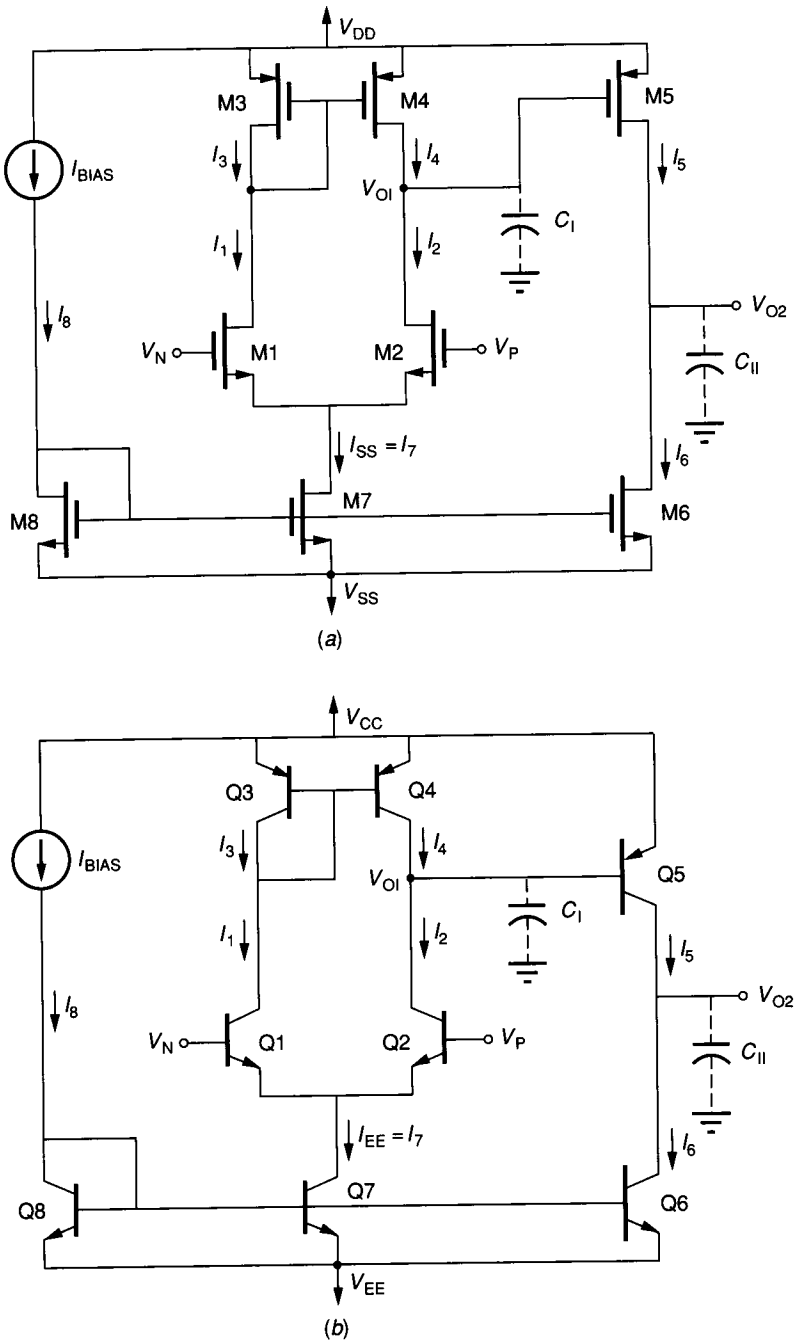


FIGURE 6.6-7
Two-stage comparators. (*a*) CMOS, (*b*) BJT.

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} \tag{6.6-8}$$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} \tag{6.6-9}$$

and

$$I_1 = I_2 = 0.5I_7 = I_{SS} \tag{6.6-10}$$

These relationships together with Eq. 6.5-40 completely describe the constraints necessary to achieve the desired balance conditions. Unfortunately, there will always be current mismatches in the current mirrors, which will lead to systematic offset (as opposed to a statistical device mismatch offset). This systematic offset is investigated in the following example.

Example 6.6-1. Calculation of systematic offset. The two-stage comparator of Fig. 6.6-7*a* with the following device sizes has been designed using Eqs. 6.6-8–6.6-10 and Eq. 6.5-40: $W_1/L_1 = W_2/L_2 = 20\ \mu/10\ \mu$, $W_3/L_3 = W_4/L_4 = 20\ \mu/10\ \mu$, $W_5/L_5 = 40\ \mu/10\ \mu$, $W_6/L_6 = 10\ \mu/10\ \mu$, $W_7/L_7 = 10\ \mu/10\ \mu$. Assume that $V_{DD} = 10$ V, $V_{SS} = 0$ V, $V_{DS7} = 3$ V, and $V_{DS3} = V_{DS4} = 2$ V. The pertinent process parameters are $K_N' = 24.75\ \mu A/V^2$, $K_P' = 10.13\ \mu A/V^2$, $|V_{TO}| = 1$ V, $\gamma_N = \gamma_P = 0.5\ V^{1/2}$, $\lambda_N = 0.015\ V^{-1}$, and $\lambda_P = 0.02\ V^{-1}$. Find the systematic offset voltage at the input of the comparator.

Solution. Assuming the bias current in M7 is 20 μA gives the following current ratios (see Sec. 5.4).

$$\frac{I_6}{I_7} = \left(\frac{1 + \lambda_N V_{DS6}}{1 + \lambda_N V_{DS4}}\right)\left(\frac{W_6/L_6}{W_7/L_7}\right) = \left[\frac{1 + (0.015)(5)}{1 + (0.015)(2)}\right](1) = 1.029$$

$$\frac{I_5}{I_4} = \left(\frac{1 + \lambda_P V_{DS5}}{1 + \lambda_P V_{DS4}}\right)\left(\frac{W_5/L_5}{W_4/L_4}\right) = \left[\frac{1 + (0.020)(5)}{1 + (0.020)(2)}\right](2) = 2.115$$

and

$$I_7 = 2I_4$$

Thus, the currents I_6 and I_5 can be expressed as

$$I_6 = (1.029)(2)I_4 = 2.058I_4$$

and

$$I_5 = 2.115I_4$$

Since I_5 is greater than I_6, then the current in M5 must be reduced. Next we determine by how much V_{GS5} must be reduced in order to make I_5 equal I_6. The method for accomplishing this is expressed by the following relationship.

$$\Delta V_{GS6} = \left[\frac{2L_5}{K_5 W_5}\right]^{1/2}\left[(I_6)^{1/2} - (I_5)^{1/2}\right] = -14.1\ \text{mV}$$

It can be shown that the voltage gain of the differential amplifier is 81.32. Dividing this value into ΔV_{GS6} gives the systematic offset at the input of the comparator as $|V_{OS}| = 0.174$ mV.

The two-stage BJT op amp is also suitable for use as a comparator. In many cases, the higher gain of the BJT differential amplifier comparator makes it unnecessary to turn to the two-stage architecture. We can note that if the two-stage comparator only switches from V_{OH} to V_{OL} or from V_{OL} to V_{OH}, that compensation is not necessary.

The performance of the input common-mode range of the two-stage BJT and CMOS comparators is identical to that of the BJT and CMOS differential amplifiers of Sec. 6.3. For the CMOS two-stage comparator, a procedure for designing the input stage for a specific common-mode input range is to size M3 to meet the maximum input requirement and design the sizes of M1 and M2 to meet the minimum input requirement. The input common-mode range limits for the CMOS differential amplifier were given in Eqs. 6.3-40 and 6.3-42. These limits, according to the device numbering in Fig. 6.6-7, are

$$V_{G1}(\max) = V_{DD} - \left[\frac{I_7}{\beta_3}\right]^{1/2} - |V_{TO3}| - V_{T1} \tag{6.6-11}$$

where $\beta_3 - K'_P(W_3/L_3)$ and

$$V_{G1}(\min) \simeq V_{TO7} + V_{TO1} + V_{G7} \tag{6.6-12}$$

However, since V_{G7} is not known, it is more convenient to express Eq. 6.6-12 as

$$V_{G1}(\min) \simeq V_{SS} + V_{DS7} + \left[\frac{I_7}{\beta_1}\right]^{1/2} + V_{T1} \tag{6.6-13}$$

where $\beta_1 = K'_N(W_1/L_1)$. An example will be given to illustrate the design of the input stage for a specified input common-mode range.

Example 6.6-2. Designing for a specified input common-mode range. Using the circuit of Fig. 6.6-7*a*, size the transistors M1 through M4 for an input common-mode range of 1.5 to 9 V with $V_{DD} = 10$ V and $V_{SS} = 0$ V.

Solution. Assume the same device parameters as used in Example 6.6-1, except that the magnitude of the p-channel and n-channel threshold voltages vary from 0.4 to 1.0 V, $I_7 = 20$ μA, and $V_{DS}(\text{sat}) = 0.1$ V. Using Eq. 6.6-13 with $V_{G1}(\min) = 1.5$ V, $V_{DS7} = 0.1$ V and $V_{T1} = 1$ V (worst case), we get $\beta_1 = 125$ μA/V^2, which gives $W_1/L_1 = W_2/L_2 = 5.05$. Using Eq. 6.6-11 with $V_{G1}(\max) = 9$ V and worst-case threshold voltages gives $\beta_3 = 125$ μA/V^2, which gives $W_3/L_3 = W_4/L_4 = 12.34$.

6.6.3 Propagation Delay of Two-Stage Comparators

In completing the design of the two-stage CMOS comparator, the gain of the comparator will be achieved by the geometry and dc current of M5. The remaining characteristic to be examined is the propagation delay of the two-stage comparator. Since the comparator is made up of two stages, the total delay is determined by adding the propagation delays of each stage together. Figure 6.6-7 shows the

CMOS and BJT two-stage comparators and the two parasitic capacitors that will be the primary source of the propagation delay. These capacitors are the same ones used in Fig. 6.5-6*b*. C_c was not included in Fig. 6.5-6*a* because the comparators are not usually compensated since they do not normally operate in the linear range. Compensation is only necessary when negative feedback is applied around the comparator. The analysis for the propagation delay of the two-stage comparator is based on the waveforms illustrated in Fig. 6.6-8. The delay for the first stage is the time required for V_{OI} to go from its quiescent state (V_{OHI} or V_{OLI}) to the trip point (V_{TRP2}) of the second stage. The delay for the second stage is the time required for V_{OII} to go from its quiescent state (V_{OHII} or V_{OLII}) to the trip point of the load circuit, which will be assumed to be $0.5(V_{OHII} + V_{OLII})$.

We will consider the propagation delay time for both the BJT and CMOS two-stage comparators simultaneously. It is seen that the propagation delay time for a rising output (T_p^+) will be different from the propagation delay time for a falling output (T_p^-). As a result, we will define the propagation delay time of a comparator (T_p) as the average of T_p^+ and T_p^-. First, let us assume that the output of the comparator is falling and develop an expression for T_p^-. It will be assumed that the difference between V_P and V_N is large enough that M2 (Q2) is off and all of I_7 goes through M1 (Q1). Therefore, the current available to

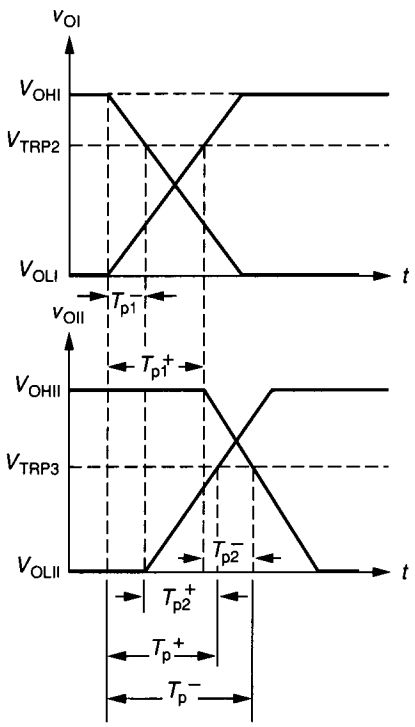


FIGURE 6.6-8
The slewing waveforms at the output of each stage of the two-stage comparator.

charge C_I from V_{OLI} to V_{OHI} is I_7. Thus, the rising propagation delay for the first stage (T_{p1}^+) is

$$T_{p1}^+ = C_I \frac{V_{TRP2} - V_{OLI}}{I_7} \tag{6.6-14}$$

Similarly, the propagation delay time for the falling output of the second stage is

$$T_{p2}^- = C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5} \tag{6.6-15}$$

Adding Eqs. 6.6-14 and 6.6-15 together results in

$$T_p^- = C_I \frac{V_{TRP2} - V_{OLI}}{I_7} + C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5} \tag{6.6-16}$$

The trip point at the input of stage 2 for the BJT is approximately $V_t \ln (I_{BIAS}/I_s)$. I_{BIAS} is the bias current in the second stage, Q6. The trip point for the CMOS output stage is found by equating the currents in M5 and M6, assuming both devices are saturated. The result is

$$\frac{\beta_5}{2}[V_{GS5} - V_{T5}]^2 = I_6 = I_5 \tag{6.6-17}$$

where $\beta_5 = K_P'(W_S/L_S)$ which gives a trip point of

$$V_{TRP2} = V_{DD} - V_{GS5} = V_{DD} - V_{T5} - \left[\frac{2I_5}{\beta_5}\right]^{1/2} \tag{6.6-18}$$

The propagation delay time for a positive-going output is similar, except that the current source charging C_{II} is not limited by the dc value of I_5. The falling propagation delay time for the input stage is given as

$$T_{p1}^- = C_I \frac{V_{OHI} - V_{TRP2}}{I_7} \tag{6.6-19}$$

The rising propagation delay time is given by

$$T_{p2}^+ = C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5(\text{max})} \tag{6.6-20}$$

where $I_5(\text{max})$ is the current M5 or Q5 can source to C_{II} when the gate or base is taken low. In order to find $I_5(\text{max})$, one must know the value of V_{GS5}. Obviously, the value of V_{GS5} will be somewhere between V_{TRP2} and V_{OLI}. Let us approximate V_{GS5} as halfway between V_{OHI} and V_{OLI}. This gives $I_5(\text{max})$ for the CMOS comparator as

$$I_5(\text{max}) \simeq \frac{\beta_5}{2}\left[\frac{V_{OHI} - V_{OLI}}{2} - V_{T5}\right]^2 \tag{6.6-21}$$

For the BJT comparator, $I_5(\text{max})$ is

$$I_5(\text{max}) \simeq \beta_F 5 I_7 \tag{6.6-22}$$

With this interpretation of $I_5(\max)$, the rising propagation delay time of the two-stage comparator is

$$T_p^+ = C_I \frac{V_{OHI} - V_{TRP2}}{I_7} + C_{II} \frac{V_{OHII} - V_{OLII}}{2I_5(\max)} \tag{6.6-23}$$

An example will illustrate the use of these relationships.

Example 6.6-3. Calculation of the propagation delay time for the two-stage comparator. Calculate the propagation time for the CMOS and BJT two-stage comparators of Fig. 6.6-7. Let $V_{DD} = -V_{SS} = 5$ V, $V_{OLI} = -3$ V, $V_{OHI} = 4$ V, $V_{OHII} = 4$ V, and $V_{OLII} = -4$ V. Using the values $C_{gs} = 0.2$ pF, $C_{ds} = 0.1$ pF, and $C_L = 0.5$ pF and assuming the model values of $K_P' = 12.5\ \mu A/V^2$ and $W_5/L_5 = 4.5$. Let $V_{CC} = -V_{EE} = 5$ V, $V_{OHI} = -V_{OLI} = 4.7$ V and $V_{OHII} = -V_{OLII} = 4.5$ V. Furthermore, let us assume that $\beta_{F5} = 100$, $I_{s5} = 0.01$ pA, $C_\mu = 0.2$ pF, $C_\pi = 2$ pF, $C_{CS} = 0.4$ pF, and $C_L = 3$ pF.

Solution. Let us first consider the CMOS two-stage comparator. From Eqs. 6.6-18 and 6.6-21, the values of $V_{TRP2} = 2.67$ V and $I_5(\max) = 112.5\ \mu A$. From Eqs. 6.6-14 and 6.6-15, we obtain the values $T_{p1}^+ = 0.227\ \mu s$ and $T_{p2}^- = 0.056\ \mu s$. Using Eq. 6.6-16 gives the falling propagation delay time as $T_p^- = 0.283\ \mu s$. From Eqs. 6.6-19 and 6.6-20, we get $T_{p1}^- = 0.0132\ \mu s$ and $T_{p2}^+ = 0.0249\ \mu s$. This gives a rising propagation delay time of $0.038\ \mu s$. The average propagation delay time is $T_p = 0.161\ \mu s$. It is seen that the fastest transition of the CMOS comparator is for a rising output.

Next let us consider the BJT two-stage comparator. V_{TRP2} is equal to $V_{CC} - V_t \ln(I_5/I_{s5})$, which is 4.482 V. $I_5(\max)$ is equal to 1 mA from Eq. 6.6-22. From Eqs. 6.5-10 and 6.5-13 we find that $C_I = 3$ pF and $C_{II} = 3.8$ pF. Assuming $I_5 = 200\ \mu A$ and $I_7 = 40\ \mu A$ in Eqs. 6.6-14 through 6.6-16 gives $T_{p1}^+ = 0.69\ \mu s$, $T_{p2}^- = 0.086\ \mu s$, and $T_p^- = 0.775\ \mu s$. Equations 6.6-19, 6.6-20, and 6.6-23 give $T_{p1}^- = 0.0164\ \mu s$, $T_{p2}^+ = 0.0043\ \mu s$, and $T_p^+ = 0.021\ \mu s$. The average propagation delay time of the BJT two-stage comparator is found as $T_p = 0.398\ \mu s$.

We note two things of interest about the two-stage comparator. First, as illustrated in Example 6.6-3, the propagation delay time for a falling output is different from the propagation delay time for a rising output. The reason is due to the value of V_{TRP2}. In both cases, V_{TRP2} is very close to the value of V_{OHI}, which minimizes the delay of the first stage. In addition, the ability to source more output current than sinking current at the output of the second stage reduces the delay time of the second stage. Therefore, two methods that will reduce the propagation delay time of a two-stage comparator are increasing the current sinking/sourcing capability and reducing the signal swings. Of course, smaller values of C_I and C_{II} will reduce the propagation delay times.

Another form of comparator is the *clamped comparator*, shown in Fig. 6.6-9. This comparator architecture attempts to reduce the propagation delay time by keeping the output swing of the first stage clamped. Closer examination of Fig. 6.6-9 shows that only the drains (collectors) of the output devices M5 and M6 (Q5 and Q6) have a large difference between V_{OH} and V_{OL}. Consequently, the propagation delay for the first stage is greatly reduced. While this comparator

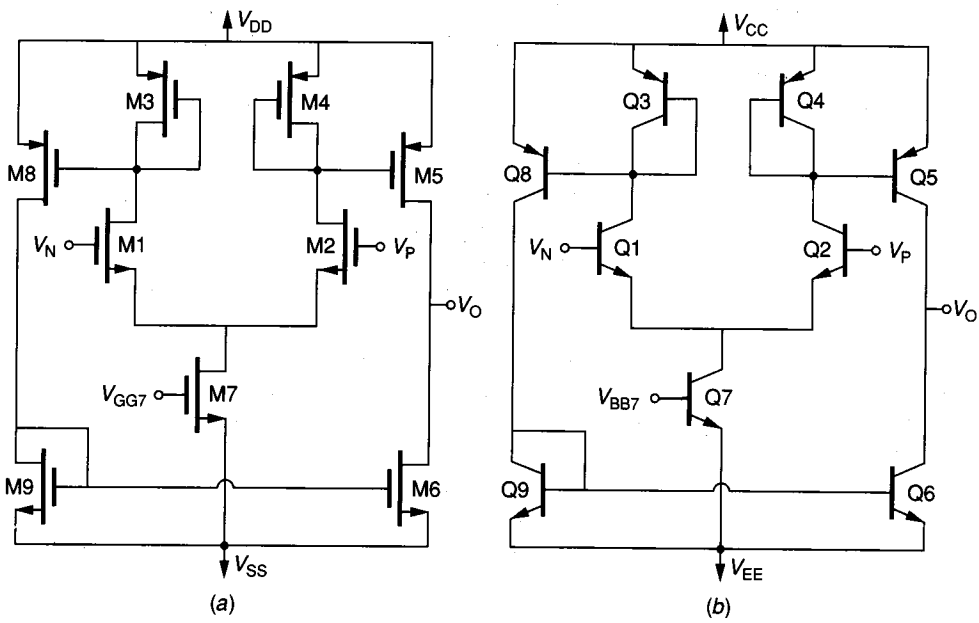


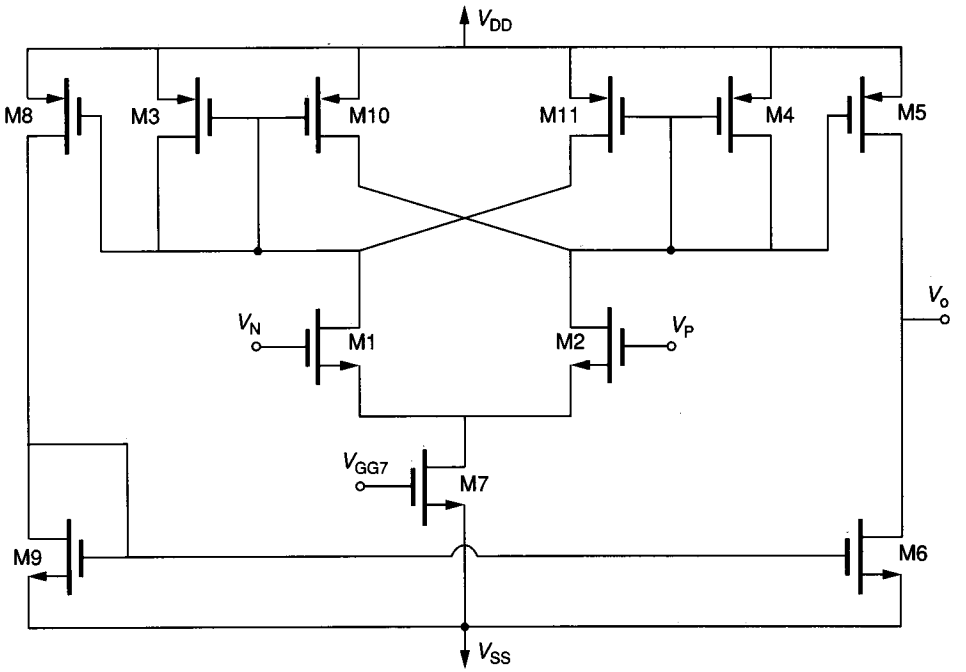
FIGURE 6.6-9
Two-stage clamped comparators: (*a*) CMOS, (*b*) BJT.

architecture reduces the propagation delay time, the overall comparator gain is reduced. Since the effective load devices of the input differential amplifier are smaller, the gain is significantly reduced. In fact, the voltage gain of the first stage will be approximately equal to the ratio of the transconductances of M1 (Q1) and M3 (Q3).

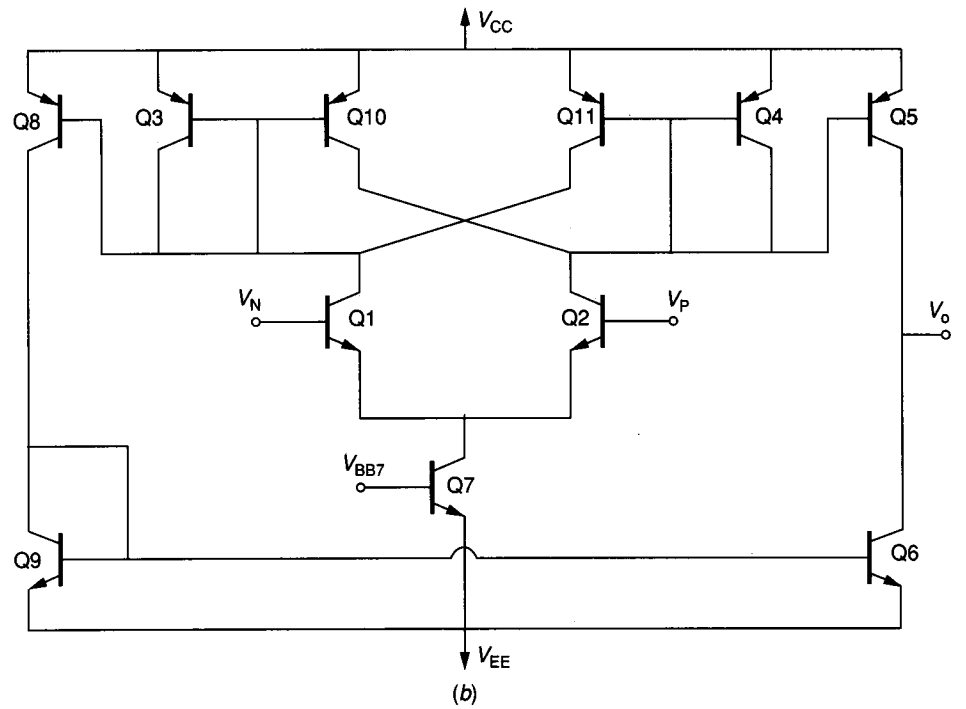
The use of weak positive feedback to overcome the low gain of the clamped comparator can result in satisfactory gain and minimized propagation delay time. One possible implementation is shown in Fig. 6.6-10, where M10 and M11 (Q10 and Q11) have introduced positive feedback paths between the outputs of the differential amplifier. The amount of positive feedback must be less than unity so that the stage still acts like a linear stage as a result of overall negative feedback provided by the source (emitter) connections of the input transistors M1 and M2 (Q1 and Q2).

6.6.4 Comparators Using Positive Feedback

The second approach to implementing comparators uses strong positive feedback or regenerative techniques. This approach is similar to that used in sense amplifiers for memories. Figure 6.6-11 shows a flip-flop with storage capacitors to ground at each output. The circuit works as follows. Assume that the strobe is low, so that M5 (Q5) is off. The flip-flop, consisting of M1 through M4 (Q1 through Q4), is deactivated since no current can flow through any of the devices. This mode



(*a*)



(*b*)

FIGURE 6.6-10
Two-stage, cross-coupled clamped comparator: (*a*) CMOS, (*b*) BJT.

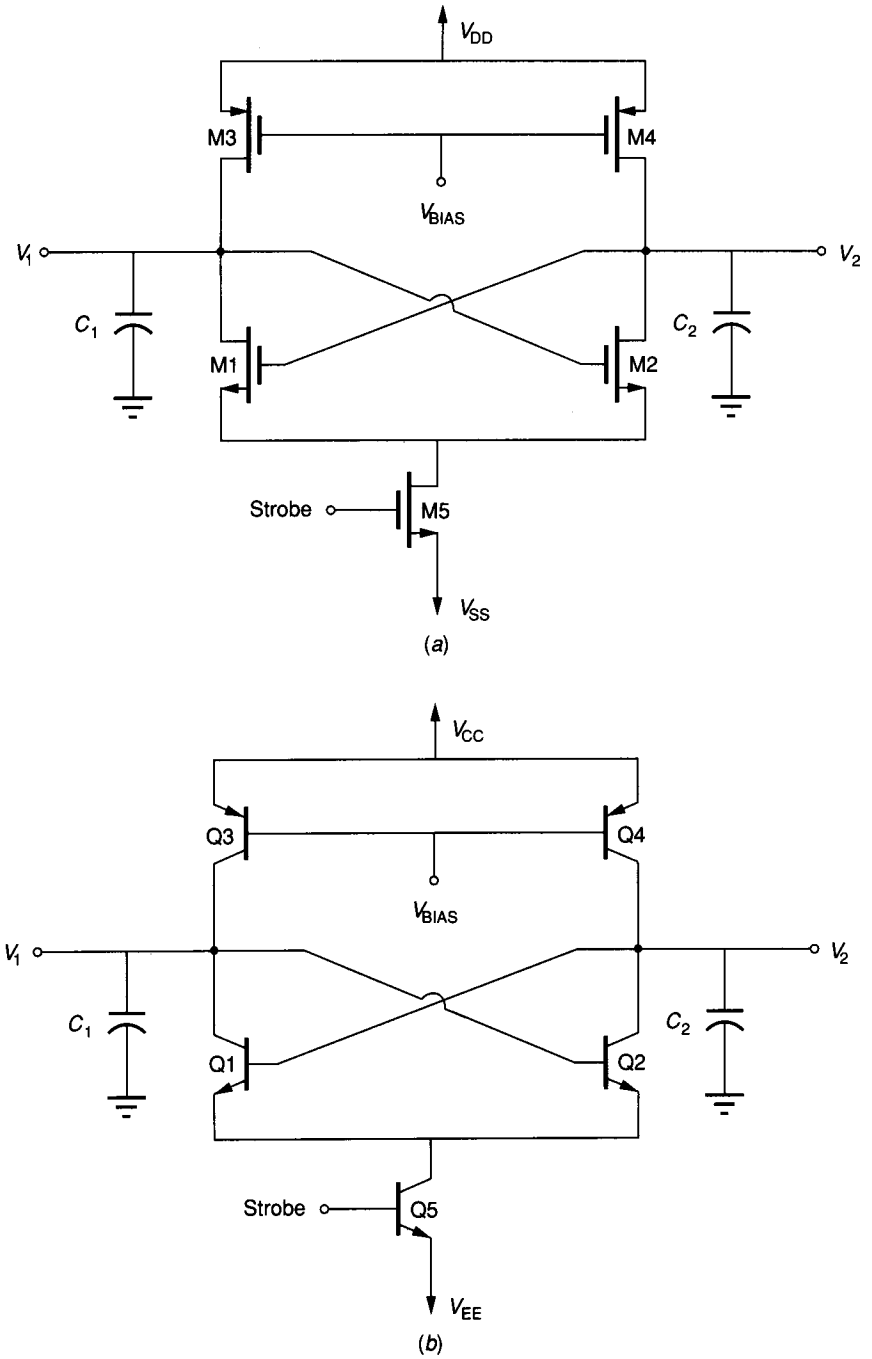


FIGURE 6.6-11
Strobed flip-flop: (*a*) CMOS, (*b*) BJT.

is called the *memory mode,* because the capacitors C_1 and C_2 will "remember" the states of V_1 and V_2. During this time, C_1 and C_2 can also be changed to new values of V_1 and V_2, respectively. When the strobe turns on the flip-flop, then it will go to the state corresponding to the values of V_1 and V_2. For example, if V_1 is greater than V_2, then when the strobe (clock) pulse is applied to M5 (Q5), the voltage at the gate (base) of M2 (Q2) will be higher than the voltage at the gate (base) of M1 (Q1). If the devices are matched, then the flip-flop will regeneratively switch to the state with V_1 high and V_2 low. This circuit can detect differences in V_1 and V_2 within 5 to 10 mV depending on how well the devices in the circuit are matched. A circuit showing how the clocks are applied and how the outputs are buffered is illustrated in Fig. 6.6-12. During the sample mode, ϕ_1 is low and ϕ_2 is high. If V_2 is greater than V_1, then the logic output Q is true. If V_1 is greater than V_2, then the logic output $\overline{Q}$ is true.

6.6.5 Autozeroing

One of the more serious problems of all comparators is the input offset voltage. Clever design techniques and careful layout can reduce but not eliminate the effects of offset. In most applications, the comparator does not operate continuously but rather makes a comparison between two voltages and then is reset. During the reset phase, it is possible to apply a technique called *autozeroing*. This technique works particularly well with CMOS because of the high input resistance of MOS devices. This is rather fortunate, as the offset of CMOS circuits is typically a factor of 2 or more worse than for equivalent BJT circuits.

Figure 6.6-13 illustrates an input offset voltage canceling algorithm. The comparator is shown in terms of an ideal comparator with an external offset voltage in Fig. 6.6-13*a*. A polarity is arbitrarily assigned for purposes of convenience. It is also assumed that the comparator works on a nonoverlapping two-phase clock cycle. During the first cycle, designated ϕ_1, the offset is measured as shown in Fig. 6.6-13*b* and stored in a capacitor, C_{AZ}. During the second cycle, designated ϕ_2, the capacitor is connected in such a manner as to cancel the effects of the offset, as illustrated in Fig. 6.6-13*c*.

A practical implementation of an autozeroed comparator is shown in Fig. 6.6-14. During ϕ_1, the offset is sampled and stored in C_{AZ}. During ϕ_2, the capacitor C_{AZ} is connected in such a manner as to cancel the offset voltage. The comparator can be CMOS or BJT as long as the input resistance is sufficiently large so that C_{AZ} does not discharge during ϕ_2. Figure 6.6-15*a* shows the configuration modified for the case where the comparator is noninverting and V_N is zero. Figure 6.6-15*b* shows the modification of Fig. 6.6-14 for the case where the comparator is inverting and V_P is zero.

Although the autozero technique seems like the perfect solution to the offset problem, it does not completely remove the influence of offset for several reasons. The first is that when the MOS switches open and close, charge is injected or removed by the large clock swings on the gates of the switches. Second, the capacitor C_{AZ} will lose some of its charge during the ϕ_2 phase. Third, if the offset is completely canceled for a given common-mode value of V_P and V_N

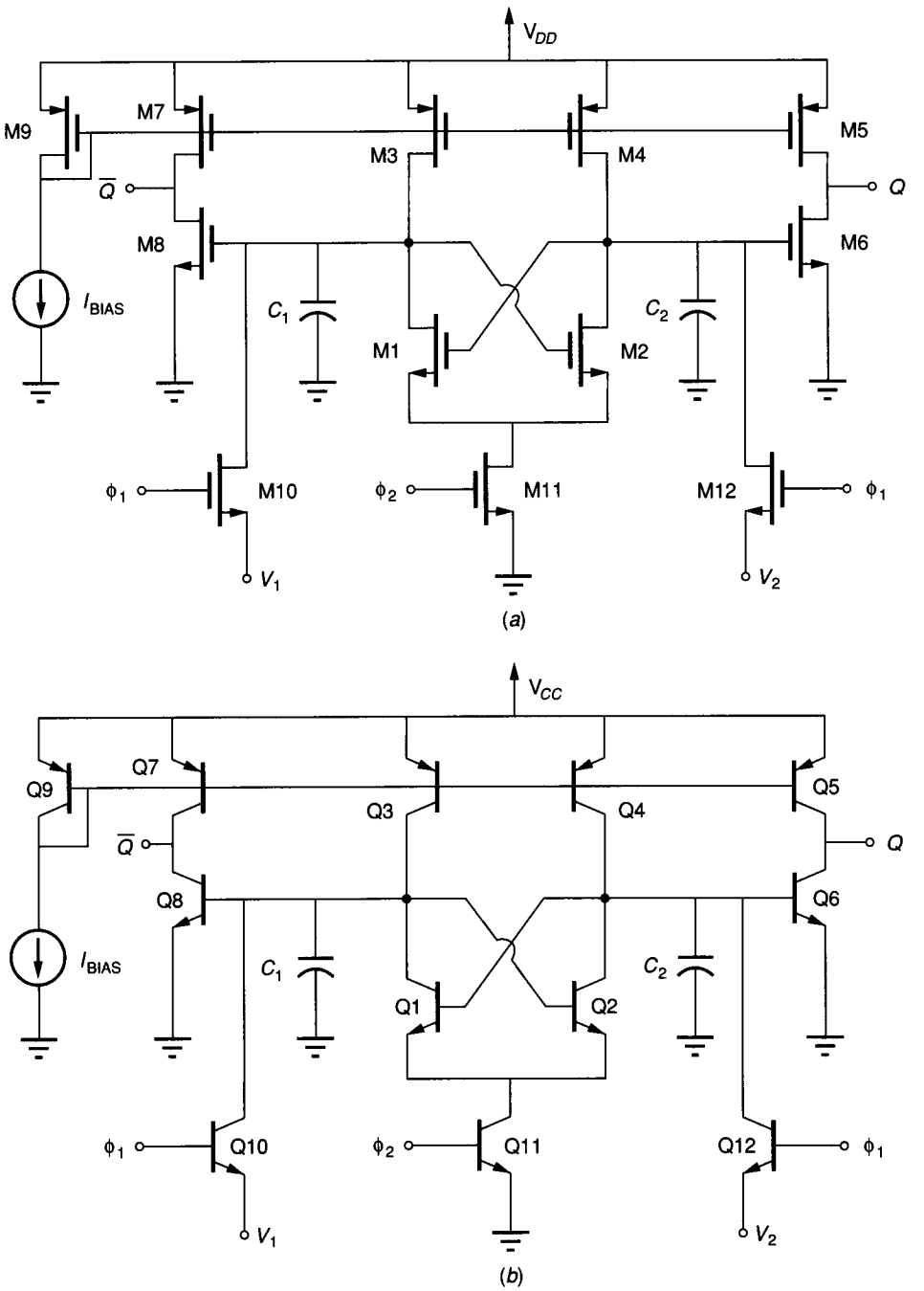


FIGURE 6.6-12
Sense amplifier used as a comparator: (*a*) CMOS, (*b*) BJT.

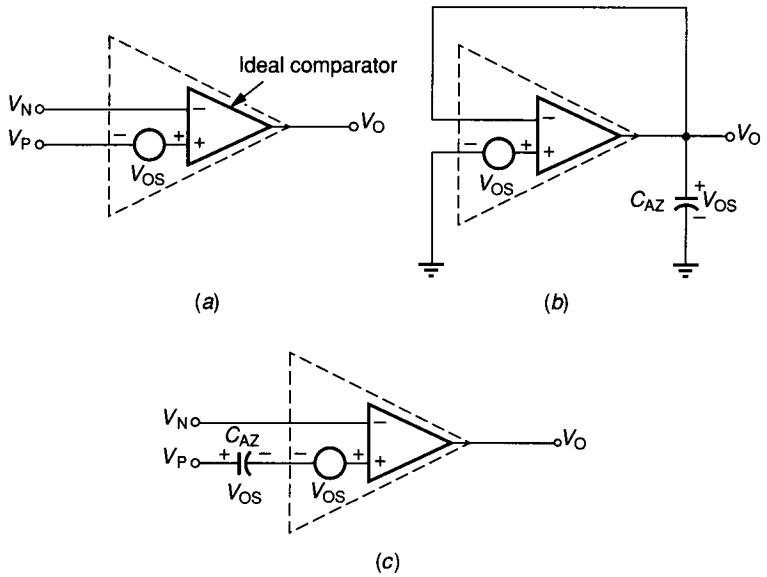


FIGURE 6.6-13
Algorithm to achieve autozeroing of a comparator with offset: (*a*) Model for offset, (*b*) Storing of V_{OS} in C_{AZ}, (*c*) Cancellation of V_{OS}.

during ϕ_1, it may not cancel during ϕ_2 because a different common-mode value of V_P and V_N may have a different value of offset voltage. There is also the problem of stability because the comparator has unity gain, negative feedback applied to it during the sampling mode. It is necessary to compensate the comparator. Finally, a noise kT/C_{AZ} is injected into the circuit each time the switch closes.

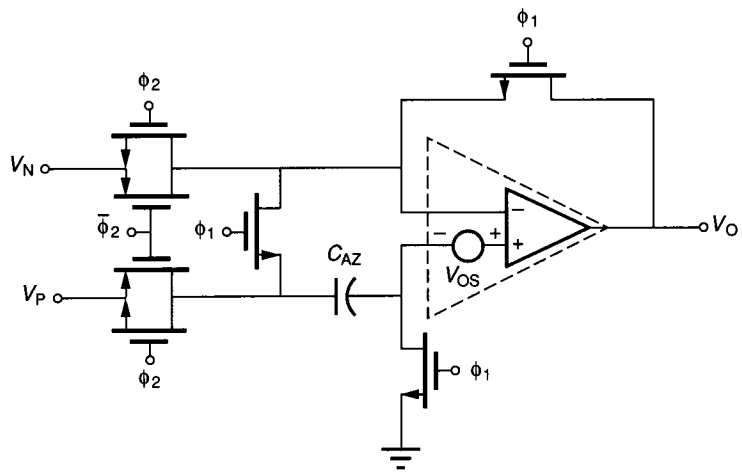


FIGURE 6.6-14
Practical implementation of an autozeroed comparator.

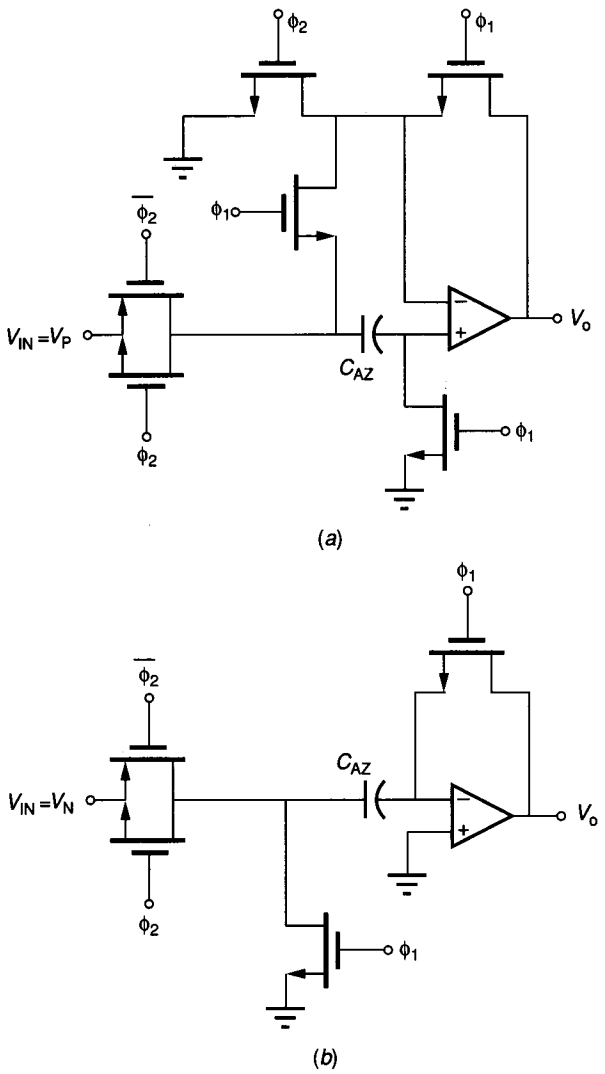


FIGURE 6.6-15
(*a*) Noninverting autozeroed comparator, (*b*) Inverting autozeroed comparator.

The design principles of voltage comparators and various architectures that can be employed have been presented in this section. The important parameters of the comparator are its resolving capability, its input offset voltage, its propagation delay time, and its common-mode input range. The performance of the various circuits was related to these parameters. Except for the considerations of propagation delay time, the comparator requirements were found to be similar to those of the op amp. The comparators in this section represent simple but practical designs. This section represents the starting point in the design of more complex comparators. It should allow the designer the ability to select the design most suitable for the specification. The next step is a thorough simulation of the comparator using a simulator.

6.7 SUMMARY

Basic circuits that form the high-level building blocks of analog integrated circuit design have been presented in this chapter. These circuit blocks include the inverter, the differential amplifier, the output amplifier, the op amp, and the comparator. Design procedures, principles, and examples were given for each type of circuit for both BJT and CMOS technologies. Most of the circuits considered used n-channel or npn devices as the input devices. This choice typically will lead to better performance. The use of p-channel or pnp input devices is straightforward and exactly follows the design concepts presented in this chapter.

It was shown that the design cycle of these blocks starts with the specifications of the circuit performance. Next, an architecture is proposed to implement the circuit. This architecture is always made up from building blocks or circuit blocks with which the designer is familiar. The proposed architecture is then analyzed (typically by hand) and modified by the designer, leading to a first-cut design. This design is then simulated with much more accuracy and detail using a circuit simulator such as SPICE2. The simulation is a very important part of the design cycle and is where the designer can explore process parameter variation and second-order effects.

The circuits presented in this chapter along with the building blocks of Chapter 5 form the blocks or components which the designer uses to achieve a circuit realization. Most of the analog circuits and systems presented in the remainder of this text are simply combinations of these blocks or components. In fact, some of the circuits in this chapter are combinations of previous circuits. For example, the op amp was implemented as a combination of the differential amplifier and the inverter or cascode amplifier.

The material presented in this chapter represents the simplest level of design because of limited space. In many applications, these simple circuits are sufficient. The basic design sequence has been illustrated and has given the reader an appreciation for the design process. This material should be a good starting point in the design of more complex analog integrated circuits.

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PROBLEMS

Section 6.1

6.1 Assume that Eq. 6.1-1, which corresponds to the circuit of Fig. 6.1-3*a*, is given as

$$I_O = V_{IX}^2 + \frac{V_{OX}}{100}$$

and that

$$I_L = \frac{V_P - V_{OUT}}{100}$$

Solve for the small signal voltage gain when $V_{IN} = V_{OUT} = 0$ V.

6.2 Use the relationships given in Prob. 6.1 and develop a linear small signal model similar to that of Fig. 6.1-6. Assuming $V_{IN} = V_{OUT} = 0$ V, find the small signal voltage gain.

6.3 Assume that $r_1 = 1\ \text{M}\Omega, r_2 = 100\ \text{k}\Omega, C_1 = 1$ pF, $C_2 = 1$ pF, and $g_m = 0.001$ S. Find the root (poles and zero) locations if $C_3 = 0$ and $C_3 = 1$ pF for the circuit of Fig. 6.1-8.

6.4 Repeat Example 6.1-1 if $W_1/L_1 = 100\ \mu/10\ \mu$ and $W_2/L_2 = 5\ \mu/10\ \mu$.

6.5 Repeat Example 6.1-2 if $W_1/L_1 = W_2/L_2 = 10\ \mu/10\ \mu$.

6.6 Repeat Example 6.1-2 for the inverter of Fig. P6.6. Assume the active area extends 10 μ beyond the polysilicon.

6.7 Figure P6.7 shows several MOS inverters. Assume that $K_N = 2K_P$, that $\lambda_N = \lambda_P$, and that the dc bias current through each inverter is equal. Qualitatively select, without using extensive calculations, which inverter(s) has (*a*) the largest ac small signal gain, (*b*) the lowest ac small signal gain, (*c*) the highest ac output resistance, and (*d*) the lowest ac output resistance. Assume all devices are in saturation.

6.8 Repeat Example 6.1-4 for $V_{BB2} = 4.3$ V.

6.9 Repeat Example 6.1-4 for the BJT inverter of Fig. 6.1-18*b*.

6.10 Figure 6.1-18 shows two BJT inverters. If $V_{AFN} = 2V_{AFP}$ and $\beta_{FN} = 2\beta_{FP}$, which inverter has (*a*) the highest ac voltage gain, (*b*) the smallest ac voltage gain, (*c*) the

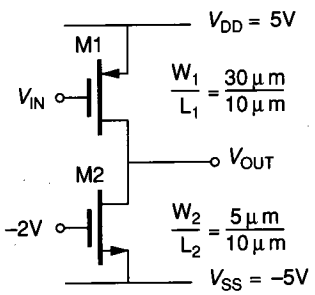

FIGURE P6.6

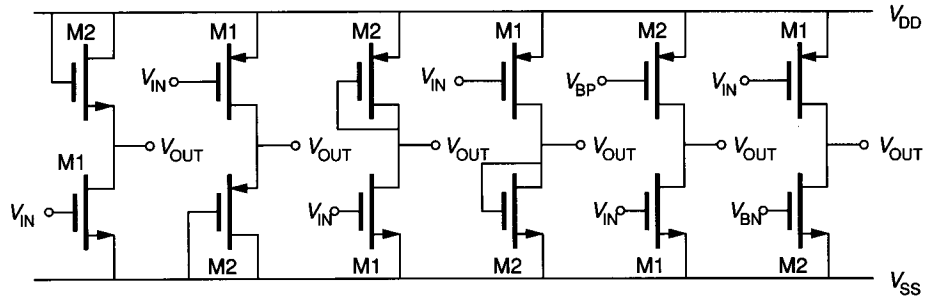

FIGURE P6.7

highest ac output resistance, and (*d*) the lowest ac output resistance. Assume that the bias currents are equal.

Section 6.2

6.11 Find the ac voltage gain and the output resistance for the circuit of Fig. 6.2-2 if the bias current is 100 μA, $W_1/L_1 = 100\ \mu/10\ \mu$, $W_2/L_2 = 100\ \mu/10\ \mu$, and $W_3/L_3 = 10\ \mu/10\ \mu$. Use the model parameters of Table 3.1-2 and assume all devices are saturated.

6.12 Repeat Example 6.2-1 with all W/L values equal to 20 $\mu/20\ \mu$.

6.13 Find the small signal voltage gain and output resistance for the circuit of Fig. 6.2-8 if $I_C = 1$ mA.

6.14 Repeat Prob. 6.13 for the circuit of Fig. 6.2-10.

Section 6.3

6.15 If the active loads of the circuit of Fig. 6.3-1 were replaced by identical drain–gate-connected enhancement n-channel transistors, sketch the large signal voltages, V_{D1} and V_{D2}, as a function of the differential input voltage V_{ID} if K_N' is 20 μA/V^2, $W_1/L_1 = W_2/L_2 = 10\ \mu/10\ \mu$, $W_3/L_3 = W_4/L_4 = 10\ \mu/40\ \mu$ (M3 and M4 are the drain–gate-connected active loads), and $I_{SS} = 50$ μA. Assume $V_{DD} = 10$ V. Ignore the bulk effects of M3 and M4 in this problem.

6.16 Substitute Eq. 6.3-7 into Eq. 6.3-18 and develop an expression for V_{D1} as a function of V_{ID} as a function of $(\beta_1/I_{SS})^{1/2}V_{ID}$. Evaluate the large signal, differential to single-ended voltage gain at $V_{id} = 0$ V of Fig. 6.3-4*a* and compare with Eq. 6.3-20.

6.17 Develop expressions for the maximum and minimum input voltages, V_{G1}(max) and V_{G1}(min), for the differential amplifier of Fig. 6.3-4*a* assuming $V_{G1} = V_{G2}$. Develop expressions for the maximum and minimum output voltages, V_{D2}(max) and V_{D2}(min). Assume that these limits are found by keeping the appropriate devices in the saturation region.

6.18 Verify the small signal voltage gain, A_{vds} (Eqs. 6.3-20 and 6.3-28), and the output resistance, r_{out} (Eqs. 6.3-25 and 6.3-31) for the circuit of Fig. 6.3-4*a* and *b*.

6.19 Interchange the p-channel and n-channel devices in Fig. 6.3-4*c*. Assume that $W_1/L_1 = W_2/L_2$ and $I_5 = 10$ μA. Using the parameters of Table 3.1-2 find the voltage gain, A_{vdd}, and output resistance, r_{out}.

6.20 Replace the current sink of Fig. 6.3-12*b* with the current mirror of Fig. 5.4-12*a*. I_{IN} is to be generated by connecting an arbitrary resistor to V_{DD}, and I_{OUT} is to be used as I_5. Develop an expression for the CMRR and compare with Eq. 6.3-49.

6.21 Assume that two equal resistors designated as R_E are placed between the emitters of Q1 and Q2 at point A in Fig. 6.3-9. Construct a plot similar to that of Fig. 6.3-10 of the normalized value of I_{C1} as a function of V_{ID}. Express the differential-in, single-ended-out transconductance for this case, g'_m, in terms of the transconductance, g_m, given by Eq. 6.3-55.

6.22 Find the small signal, differential-in, differential-out voltage gain, input differential resistance, and output resistance for the circuit of Fig. 6.3-11 if Q1 and Q2 are matched, Q3 and Q4 are matched, $I_{EE} = 100\ \mu A$, $\beta_F = 100$, $V_{AFN} = 100$ V, and $V_{AFP} = 50$ V. Assume room temperature. Repeat for $I_{SS} = 10\ \mu A$.

6.23 Verify the small signal expressions for A_{vds}, and A_{vc} and derive an expression for r_{out} and r_{id} of the circuit of Fig. 6.3-13.

6.24 Assume that $\lambda = 0.01$ V, $C_{gs} = 0.2$ pF, $C_{gd} = 0.1$ pF, and $C_L = 0.5$ pF for the MOS differential amplifier of Fig. 6.3-4*b*. Find the -3 dB frequency in Hertz and the low-frequency gain (A_{vds0}) if (*a*) $I_5 = 10\ \mu A$ and (*b*) $I_5 = 1$ mA.

6.25 Assume that $\beta_{FN} = 100$, $\beta_{FP} = 50$, $V_{AN} = 100$ V, $V_{AP} = 50$ V, $C_\mu = 1$ pF, $C_\pi = 2$ pF, $C_{CS} = 1$ pF, and $C_L = 5$ pF for the BJT differential amplifier of Fig. 6.3-11. Find the -3 dB frequency in Hertz and the low-frequency gain (A_{vds0}) if (*a*) $I_{EE} = 10\ \mu A$ and (*b*) $I_{EE} = 1$ mA.

6.26 Assume that the MOS differential amplifier of Fig. 6.3-4*c* has the parameters $K'_N = 2K'_P = 25\ \mu A/V^2$, $\lambda = 0.01$ V, $W_1/L_1 = W_2/L_2 = 10$, $W_3/L_3 = W_4/L_4 = 1$, $C_{gs} = 0.2$ pF, $C_{gd} = 0.1$ pF, and $I_{SS} = 100\ \mu A$. Find $A_{vds0}, \omega_1, \omega'_1$, and ω_2 defined in Eq. 6.3-84. Find the -3 dB frequency in Hertz for A_{vds}.

6.27 Assume that the BJT differential amplifier of Fig. 6.3-11 has the parameters of $\beta_F = 100$, $V_{AN} = 100$ V, $V_{AP} = 50$ V, $C_\pi = 5$ pF, $C_\mu = 1$ pF, and $I_{EE} = 100\ \mu A$. Find $A_{vds0}, \omega_1, \omega'_1$, and ω_2 defined in Eq. 6.3-84. Find the -3 dB frequency in Hertz for A_{vds}.

Section 6.4

6.28 If the specifications of an output amplifier include the ability to output a voltage of ± 5 V and a slew rate of 10 V/μs, what is the maximum required output current if (*a*) $R_L = 10\ k\Omega$ and $C_L = 50$ pF, (*b*) $R_L = 5\ k\Omega$ and $C_L = 50$ pF, and (*c*) $R_L = 10\ k\Omega$ and $C_L = 100$ pF?

6.29 If the dc bias current in a Class A amplifier is 400 μA and the power supplies are ± 5 V, find the signal power dissipated in a 10 kΩ load resistance for the maximum output sinusoidal signal. Calculate the power given by the power supplies and divide this value into the signal power to calculate the maximum efficiency of the Class A amplifier.

6.30 Use the small signal models for the MOS and BJT transistors to develop the expression given in Eqs. 6.4-24 and 6.4-25 for the circuit of Fig. 6.4-9*a* and *b*.

6.31 If the n-channel transistors in Fig. 6.4-9*a* have $K'_N = 25\ \mu A/V^2$, $V_{TO} = 1$ V, $V_{GG2} = -3V_g$, $V_{DD} = -V_{SS} = 5$ V, $\gamma = 0.5\ V^{1/2}$, $\phi_N = 0.6\ V$, $W_1/L_1 = 10$, and $W_2/L_2 = 40$, find the maximum peak-to-peak output voltage swing if R_L is 10 kΩ, assuming that the gate of M1 can be driven to within 1 V of the $+5$ V power supply. What are the maximum positive and negative slew rates when the output voltage is passing through zero for a load capacitor of 50 pF (assuming that V_{IN} can be driven to $+4$ V)?

6.32 Show how the MOS differential amplifier of Fig. 6.3-4*c* can be used to implement the error amplifiers of Fig. 6.4-15*a*. Note that the implementation of one of the error amplifiers will require opposite-type devices. If all *W/L* ratios are 1 and each transistor has a bias current of 50 μA, calculate the loop gain and the small signal output resistance of the circuit of Fig. 6.1-15*a* if $K'_N = 2K'_P = 25\ \mu A/V^2$.

Section 6.5

6.33 Assume that V_1 of Fig. 6.5-1 is zero and that a resistor R_1 is connected between a voltage source, V_{IN}, and V_2, and a resistor R_2 is connected from the output, V_O, back to the negative input of the op amp. Use the null port concept to find V_O/V_{IN}.

6.34 Repeat Prob. 6.33 if the resistor R_1 is connected from the negative input to the op amp to ground, and the voltage source, V_{IN}, is connected to the positive input of the op amp. R_2 is still connected between V_O and the negative input to the op amp.

6.35 Analyze the circuit of Fig. 6.5-6*b* and verify the expression given in Eq. 6.5-17. Use the techniques illustrated to derive the root locations as given in Eqs. 6.5-18, 6.5-19, and 6.5-20.

6.36 Determine the ratios of the emitter areas of Q6 to Q8 and Q7 to Q8 of Fig. 6.5-4*a* if I_{C1} is 5 μA and I_{C5} is 25 μA, and the 100 kΩ resistors are connected from the collector of Q8 to $V_{CC} = 5$ V and $V_{EE} = -5$ V.

6.37 For the two-stage BJT op amp, let $A_o = 100{,}000$, $R_{id} = 1$ MΩ, and $C_c = 20$ pF. Find I_{C1}, I_{C5}, GB (in MHz), and SR. Assume that the BJT parameters are $\beta_N = 200, \beta_P = 50, V_{AN} = 100$ V, and $V_{AP} = 50$ V. Give the ratios of the emitter area of Q6 to Q8 and Q7 to Q8, and determine the value of resistance to be connected from the collector of Q8 to V_{CC} if $V_{CC} = -V_{EE} = 5$ V.

6.38 Repeat Prob. 6.37 if each npn and pnp transistor is replaced with a pnp and a npn transistor, respectively.

6.39 On a log-log scale with the vertical axis running from 10^{-3} to 10^3 and the horizontal axis running from 1 μA to 100 μA, plot the low-frequency gain (A_o), the unity-gain bandwidth (GB), the power dissipation (P_d), the slew rate (SR), the output resistance (r_{out}), the magnitude of the dominant pole (p_1), and the magnitude of the RHP zero (z) normalized to their values at a bias current ($I_B = I_{DB}$) of 1 μA as a function of I_B for values of I_B from 1 μA to 100 μA for the CMOS two-stage op amp of Fig. 6.5-5*a*. Assume the op amp uses a Miller compensation capacitor, C_c, with no R_z.

6.40 If $W_1/L_1 = W_2/L_2 = 10\ \mu/10\ \mu$, complete the design of the two-stage CMOS op amp of Fig. 6.5-5*a* (i.e., find $W_3, L_3, W_4, L_4, W_5, L_5, C_c$, and R_z). Assume a minimum transistor dimension of 10 μ and use the smallest devices possible. The dc current is 100 μA in M7 and 200 μA in M8. The op amp is to have a low-frequency gain of 5000 and a unity-gain bandwidth of 1 MHz. In addition, all devices should be in saturation under normal operating conditions, and the effects of the RHP zero should be canceled. The pertinent model parameters are $K'_N = 2K'_P = 10\ \mu$A/V^2, $V_{TN} = -V_{TP} = 1$ V, and $\lambda_N = \lambda_P = 0.01$ V^{-1}. Estimate how much load capacitance, C_L, this amplifier should be able to drive without suffering a significant change in the phase margin. What is the slew rate of this op amp?

6.41 Find all currents in the circuit of Fig. P6.41, A_o, GB, SR, r_{out}, power dissipation (P_d), the dominant pole location (p_1), and the value of R_z required to cancel out the effects of the RHP zero. Assume $V_{DD} = -V_{SS} = 5$ V and $C_L = 10$ pF. The device parameters for this problem are $V_{TN} = -V_{TP} = 1$ V, $K'_N = 2K'_P = 24\ \mu$A/V^2, and $\lambda_N = \lambda_P = 0.01$ V^{-1}. Assume that $W_9/L_9 = 2W_{10}/L_{10}$, and find the value of the ratios that will implement R_z.

6.42 Design a folded cascode CMOS op amp that meets the following specifications: $A_o = 50{,}000$, GB $= 5$ MHz, and SR $= \pm 1$ V/μs for a load capacitance of 20 pF. Assume the device parameters of $K'_N = 2K'_P = 25\ \mu$A/V^2, $V_{TN} = -V_{TP} = 1$ V, $\lambda_N = \lambda_P = 0.01$ V^{-1}, all $V_{SB} = O$ V, and give the values of the W/L ratio and the dc currents for each device. What is the power dissipation of your design if the power supplies are ± 5 V?

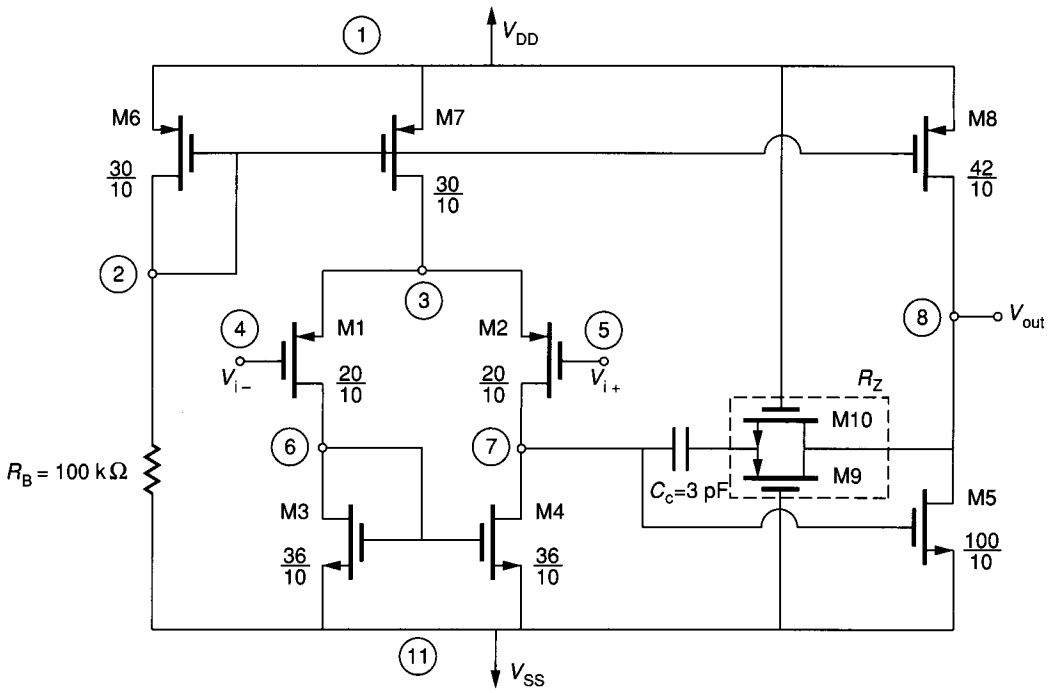

FIGURE P6.41

6.43 Use SPICE to obtain the open-loop magnitude and phase response of the two-stage CMOS op amp of Fig. 6.5-5*a* with a 20 pF load capacitance using the W and L values of Table 6.5-2. What is the phase margin of this op amp?

6.44 Propose and justify a method of measuring the open loop output resistance of an op amp.

Section 6.6

6.45 If $C_{II} = 0.7$ pF and $I_{SS} = 10\ \mu$A, find the time required for the CMOS differential comparator of Fig. 6.6-7*a* to slew 5 V. If $C_{II} = 7$ pF and $I_{EE} = 20\ \mu$A, find the time required for the BJT differential comparator of Fig. 6.6-7*b* to slew 5 V. Assume $I_6 = 10I_7$ and $C_I = 0$.

6.46 Repeat Example 6.6-1 for the calculation of the systematic offset for the BJT two-stage comparator. Use the device numbering scheme of Fig. 6.6-7. Also, assume that $V_{CC} = 10$ V, $V_{EE} = 0$ V, $V_{CE7} = 3$ V, and $V_{CE3} = V_{CE4} = 2$ V. The values of V_{AFN} and V_{AFP} are 100 V and 50 V, respectively, and the bias current in Q7 is 20 μA.

6.47 If $C_{gd} = 0.2$ pF, $C_{gs} = 0.3$ pF, and $C_L = 1$ pF, find the propagation delay times T_p^+, T_p^-, and T_p for the two-stage CMOS comparator of Example 6.6-3.

6.48 If $C_\mu = 1$ pF, $C_\pi = 5$ pF, and $C_L = 5$ pF, find the following propagation delay times T_p^+, T_p^-, and T_p for the two-stage BJT comparator of Example 6.6-3 if $I_7 = 40\ \mu$A and $I_5 = 100\ \mu$A.

Design Problems

6.49 Design a voltage-driven, inverting voltage amplifier that will provide a gain of at least -10 and a -3 dB frequency of at least 100 kHz when driving a load of 50 pF in parallel with 50 kΩ. Use the device parameters of Table 3.1-2 or Table 6.1-1.

6.50 Design a BJT inverter that will meet the specifications of Example 6.1-5.

6.51 Repeat Example 6.2-2 using a MOS current-sourcing cascode inverter.

6.52 Design a BJT differential amplifier with a differential to single-ended voltage gain of at least 100 and a common-mode voltage gain of at most 0.1. The differential input resistance should be greater than 100 kΩ. Use the parameters of Table 6.1-1.

6.53 Design a CMOS op amp using the topology of Fig. 6.5-5*a* that meets the following specifications:

$$A_v > 4000$$

$$V_{DD} = +5 \text{ V}$$

$$V_{SS} = -5 \text{ V}$$

$$\text{GB} \geq 1 \text{ MHz } (C_2 = 20 \text{ pF})$$

$$\text{SR} > 2 \text{ V}/\mu\text{s } (C_2 = 20 \text{ pF})$$

$$\text{Input common-mode range} \geq \pm 3 \text{ V}$$

$$\text{Output voltage swing} \geq \pm 4 \text{ V} (R_L = 200 \text{ k}\Omega)$$

$$P_{\text{diss}} < 10 \text{ mW}$$

Use the parameters of Table 3.1-2, and let all drawn channel lengths be 10 μ.

6.54 Design a BJT op amp that will meet the specifications of Prob. 6.6. Use the parameters of Table 6.1-1.