Figure 6.3-5*a* is simplified in Fig. 6.3-5*b*, where symmetry between M1 and M2 has been assumed, which implies $g_{m1} = g_{m2}$ and $v_{gs1} = -v_{gs2} = v_{gs}$. Also the controlled sources, $g_{m3}v_{gs3}$ and $g_{m4}v_{gs4}$, have been replaced with their equivalent resistances of $1/g_{m3}$ and $1/g_{m4}$, respectively. If the current contributions of r_{ds1} and r_{ds2} to the sources of M1 and M2 and the drain of M5 can be ignored, then the controlled sources, $g_{m1}v_{id}/2$, can be rerouted in the model of Fig. 6.3-5*c* to show that point A is in fact an ac ground. Therefore, all the model to the left of the vertical dotted line can be ignored. The final form of the small signal model is shown in Fig. 6.3-5*d*. The calculations for v_{d1} and v_{d2} are independent of each other and are given as

$$A_{v1} = \frac{v_{d1}}{v_{id}} = \frac{-g_{m1}}{2(g_{m3} + g_{ds1} + g_{ds3})} \approx \frac{-g_{m1}}{2g_{m3}} = \frac{-1}{2}\left[\frac{K'_N(W_1/L_1)}{K'_P(W_3/L_3)}\right]^{1/2} \tag{6.3-22}$$

and

$$A_{v2} = \frac{v_{d2}}{v_{id}} = \frac{g_{m1}}{2(g_{m4} + g_{ds2} + g_{ds4})} \approx \frac{g_{m1}}{2g_{m4}} = \frac{1}{2}\left[\frac{K'_N(W_1/L_1)}{K'_P(W_4/L_4)}\right]^{1/2} \tag{6.3-23}$$

Comparing Eq. 6.3-22 or 6.3-23 with Eq. 6.3-20 shows that the small signal analysis agrees with the large signal analysis. The differential voltage gain is given as

$$A_{vdd} = \frac{v_{od}}{v_{id}} = \frac{v_{d1} - v_{d2}}{v_{id}} = -\frac{g_{m1}}{2g_{m3}} - \frac{g_{m1}}{2g_{m4}} = -\frac{g_{m1}}{g_{m3}} \tag{6.3-24}$$

if M3 and M4 are also matched so that $g_{m3} = g_{m4}$.

The dc differential input resistance, r_{id}, is that resistance seen by the input voltage source, v_{id}. In this case, r_{id} is infinite. The single-ended output resistance comprises those resistances seen looking back into the output terminals of Fig. 6.3-5*d*. These resistances are

$$r_{out1} = \frac{1}{g_{m3} + g_{ds1} + g_{ds3}} \approx \frac{1}{g_{m3}} \tag{6.3-25}$$

and

$$r_{out2} = \frac{1}{g_{m4} + g_{ds2} + g_{ds4}} \approx \frac{1}{g_{m4}} \tag{6.3-26}$$

The differential output resistance, r_{od}, is equal to the ac resistance seen between the drains of M1 and M2 and can be written as

$$r_{od} = r_{out1} + r_{out2} \approx \frac{1}{g_{m3}} + \frac{1}{g_{m4}} \approx \frac{2}{g_{m3}} \tag{6.3-27}$$

It is assumed in the above calculations that all the transistors of the differential amplifier are operating in the saturation region. We shall shortly examine the voltage ranges at the input and output over which this condition holds.

The voltage gain of the differential amplifier considered in Fig. 6.3-4*a* can be increased using current sources as loads. This differential amplifier is shown in Fig. 6.3-4*b*. The previous small signal analysis holds if we let $g_{m3} = g_{m4} = 0$. The small signal performance is summarized as

$$A_{vds1} = A_{v1} = \frac{v_{d1}}{v_{id}} = \frac{-g_{m1}}{2(g_{ds1} + g_{ds3})} \tag{6.3-28}$$

$$A_{vds2} = A_{v2} = \frac{v_{d2}}{v_{id}} = \frac{g_{m1}}{2(g_{ds2} + g_{ds4})} \tag{6.3-29}$$

$$A_{vdd} = \frac{v_{od}}{v_{id}} = \frac{-g_{m1}}{g_{ds1} + g_{ds3}} = \frac{-g_{m2}}{g_{ds2} + g_{ds4}} \tag{6.3-30}$$

$$r_{out1} = \frac{1}{g_{ds1} + g_{ds3}} \tag{6.3-31}$$

$$r_{out2} = \frac{1}{g_{ds2} + g_{ds4}} \tag{6.3-32}$$

and

$$r_{od} \cong \frac{2}{g_{ds1} + g_{ds3}} \tag{6.3-33}$$

It is seen that this differential amplifier has a performance that is identical to the current-source-load sinking inverter of Fig. 6.1-11*b*.

Another configuration of the load for a differential amplifier is shown in Fig. 6.3-4*c*. This method uses a current mirror to form the load devices. The advantage of this configuration is that the differential output signal is converted to a single-ended output signal with no extra components required. In this circuit, the output voltage or current is taken from the drains of M2 and M4. The operation of this circuit is as follows. If a differential voltage, V_{ID}, is applied between the gates as defined in Eq. 6.3-21, then half is applied to the gate-source of M1 and half to the gate-source of M2. The result is to increase I_{D1} and decrease I_{D2} by equal increments, ΔI. The ΔI increase I_{D1} is mirrored through M3-M4 as an increase in I_{D4} of ΔI. As a consequence of the ΔI increase in I_{D4} and the ΔI decrease in I_{D2}, the output must sink a current of $2\Delta I$. Therefore, the transconductance of the circuit of Fig. 6.3-4*c*, I_{out}/V_{id}, is equal to that of a single transistor. This differential amplifier is a very useful circuit and will be used further in analog integrated circuit design.

The small signal analysis of the circuit of Fig. 6.3-4*c* requires a modification of the model of Fig. 6.3-5. The model suitable for small signal analysis of the circuit of Fig. 6.3-4*c* is shown in Fig. 6.3-6. The small signal, differential-in, differential-out voltage gain (A_{vdd}) is

$$\frac{v_{out}}{v_{id}} = A_{vdd} = \frac{1}{2}\left(g_{m1} + \frac{g_{m1}g_{m4}}{g_{ds1} + g_{m3} + g_{ds3}}\right)\left(\frac{1}{g_{ds2} + g_{ds4}}\right) \tag{6.3-34}$$

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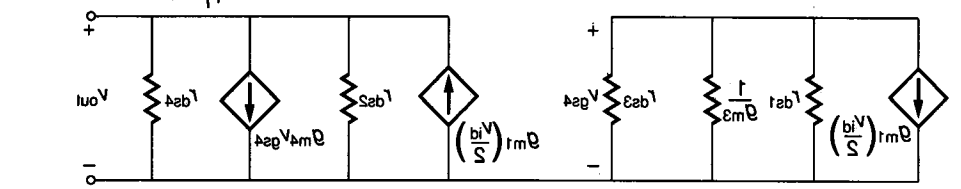


FIGURE 6.3-6
Small signal model for Fig. 6.3-4*c*.

If we assume that M3 and M4 are matched, then $g_{m3} = g_{m4}$, and since g_{m3} is much larger than either g_{ds1} or g_{ds3}, Eq. 6.3-34 can be simplified to

$$A_{vdd} \simeq \frac{g_{m1}}{g_{ds2} + g_{ds4}} \tag{6.3-35}$$

Substituting for the small signal parameters of Eq. 6.3-35 with the relationships specified in Table 3.1-3 gives

$$A_{vdd} = \frac{2(K'I_{SS}W_1/L_1)^{1/2}}{(\lambda_2 + \lambda_4)I_{SS}} = \frac{2}{(\lambda_2 + \lambda_4)}\left(\frac{K'W_1}{I_{SS}L_1}\right)^{1/2} \tag{6.3-36}$$

Again we note the dependence of the small signal performance on $I_{SS}^{-1/2}$ similar to that of the inverter. Assuming that $W_1/L_1 = 1$ and that $I_{SS} = 10\ \mu$A, the small signal, differential-in, differential-out voltage gain of the circuit of Fig. 6.3-4*c* is 103. The differential-in, single-ended out voltage gain is equal to half the value of Eq. 6.3-36, although in the case of Fig. 6.3-4*c* this voltage is not available as it would be for the differential amplifiers of Fig. 6.3-4*a* and *b*. The small signal output resistance is found from Fig. 6.3-6 as

$$r_{out} = \frac{1}{g_{ds2} + g_{ds4}} = \frac{2}{(\lambda_2 + \lambda_4)I_{SS}} \simeq \frac{1}{\lambda I_{SS}} \tag{6.3-37}$$

Of course, the small signal, low-frequency input resistance of the MOSFET differential amplifier is infinity.

Another important characteristic of the MOS differential amplifier is the input common-mode voltage range, defined earlier. For our purposes, we will assume that the input common-mode range is defined by the input voltage range over which both M1 and M2 remain in saturation. Let us consider the input common-mode voltage range of Fig. 6.3-4*c*. Assume that $V_{G1} = V_{G2}$ and that M1 is on the threshold of saturation when $V_{DG1} = V_{T1}$. We may write V_{DG1} as

$$V_{DG1} = V_{DD} - V_{SD3} - V_{G1} = V_{DD} - V_{SG3} - V_{G1} \tag{6.3-38}$$

or

$$V_{DG1} = V_{DD} - \left(\frac{2I_{D3}}{\beta_3}\right)^{1/2} - |V_{TO3}| - V_{G1} \tag{6.3-39}$$

where V_{TO3} implies that M3 is unaffected by the bulk potential. If V_{DG1} is set equal to $-V_{T1}$, then we can solve for the maximum input voltage, $V_{G1}(\max)$, as

$$V_{G1}(\max) = V_{DD} - \left(\frac{I_{SS}}{\beta_3}\right)^{1/2} - |V_{TO3}| + V_{T1} \tag{6.3-40}$$

As V_{G1} approaches V_{SS}, M1 will be in the saturation region and close to cutoff. Therefore, it makes more sense to relate $V_{G1}(\min)$ to V_{GG} when M5 is no longer in saturation. Solving for the drain-gate voltage of M5 gives

$$V_{DG5} = V_{G1} - V_{GS1} - V_{GG} \tag{6.3-41}$$

Set $V_{DG5} = -V_{TO5}$ to get

$$V_{G1}(\min) \cong V_{GG} + \left(\frac{2I_{SS}}{\beta_1}\right)^{\frac{1}{2}} + V_{TO1} - V_{TO5} \tag{6.3-42}$$

The large signal swing limitations of the output are also of interest. In this case, the swing limitations will be based on keeping both M2 and M4 in saturation. When V_{G1} is taken above V_{G2}, the output voltage, V_{OUT}, increases. The drain-gate voltage of M4 is given as

$$V_{DG4} = V_{DD} - V_{SD3} - V_{OUT} = V_{DD} - V_{SG3} - V_{OUT} \tag{6.3-43}$$

M4 is at the edge of saturation when $V_{DG4} = -|V_{TO4}|$. Using this relationship and the value for V_{SD3} used in Eqs. 6.3-38 and 6.3-39 gives the maximum output voltage as

$$V_{OUT}(\max) = V_{DD} - \left(\frac{I_{SS}}{\beta_3}\right)^{1/2} - |V_{TO3}| + |V_{TO4}| \cong V_{DD} - \left(\frac{2I_{SS}}{\beta_3}\right)^{1/2} \tag{6.3-44}$$

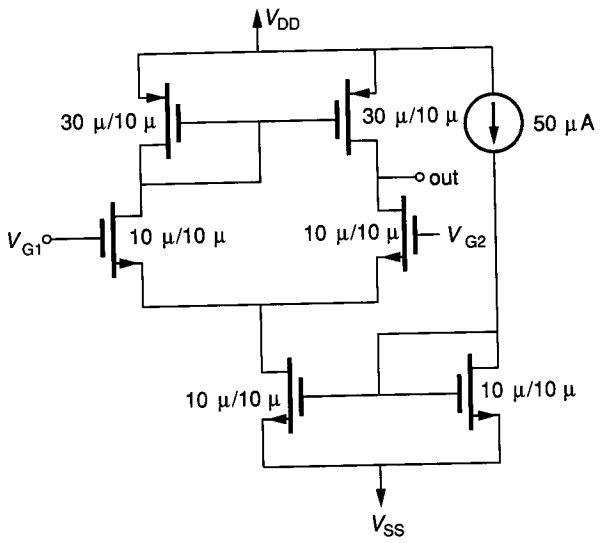
The minimum output voltage is found by determining when M2 is at the edge of saturation. The minimum output voltage for Fig. 6.3-4*c* is

$$V_{OUT}(\min) = V_{G2} - V_{T2} \tag{6.3-45}$$

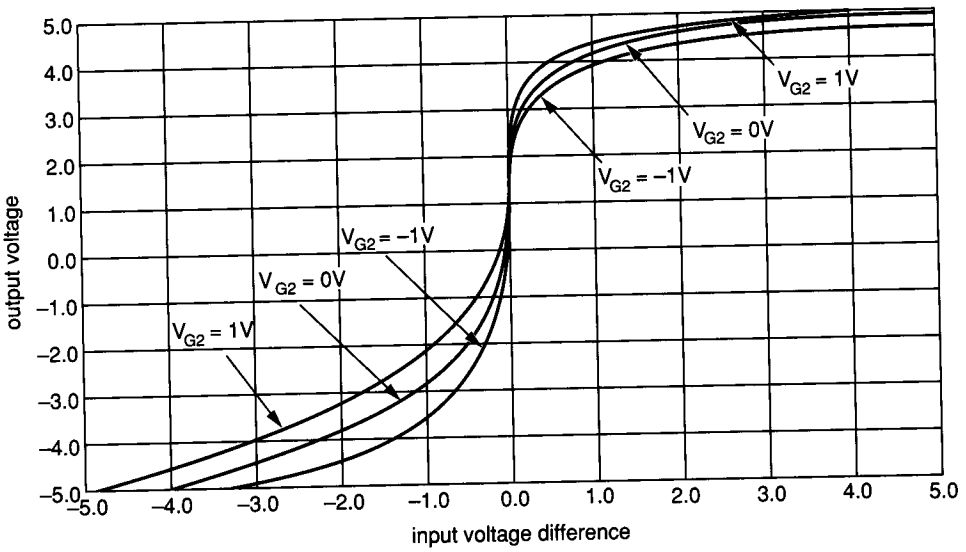
Figure 6.3-7*a* shows a differential amplifier similar to Fig. 6.3-4*c*. The simulated voltage transfer characteristic corresponding to the *W/L* values given in the schematic is shown in Fig. 6.3-7*b*. The influence of V_{G2} upon V_{OUT} (min) is illustrated in this figure. The input and output signal limits of the differential amplifiers in Fig. 6.3-4*a* and *b* can be found in a similar manner.

The small signal common-mode gain of the differential amplifier can be found by connecting both inputs together and applying a single-ended input voltage. The small signal model for the differential amplifier of Fig. 6.3-4*b* is shown in Fig. 6.3-8*a*. If we assume that M1 and M2 are matched, then the model simplifies to that shown in Fig. 6.3-8*b*. To find the common-mode gain, we wish to solve for v_{d2} in terms of v_c. If the current contribution through r_{ds1} and r_{ds2} can be neglected, then the voltage across r_{ds5} can be written as

$$v_s \approx 2g_{m1}r_{ds5}v_c \tag{6.3-46}$$



(*a*)



(*b*)

FIGURE 6.3-7
(*a*) n-channel input differential amplifier, (*b*) Simulation of voltage transfer curve for $V_{G2} = -1$, 0, and 1 V ($V_{DD} = 5$ V, $V_{SS} = -5$ V, $K'_N = 2K'_P = 28$ μA/V, $V_T = \pm 0.7$ V, and $\lambda_N = \lambda_P = 0.01\ V^{-1}$).

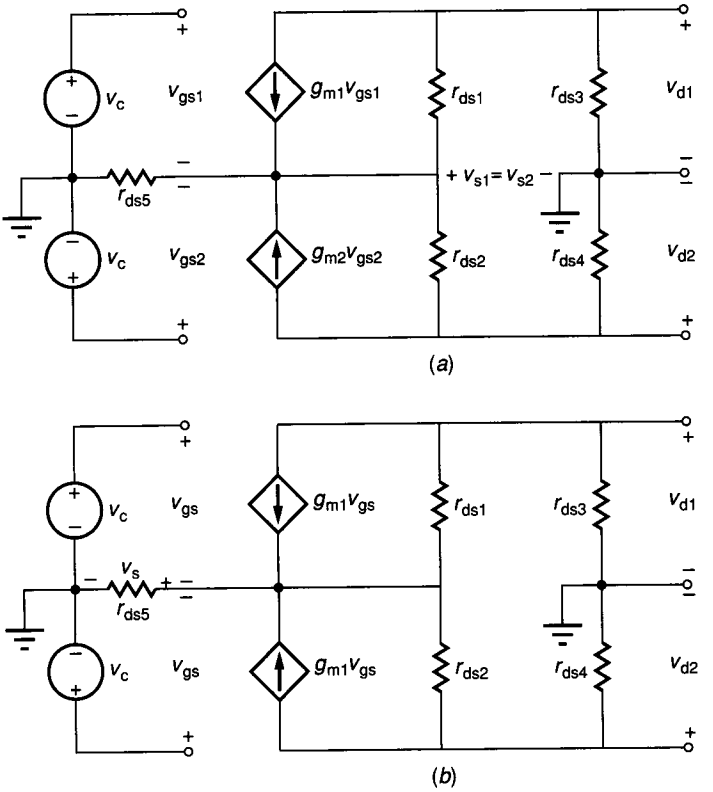


FIGURE 6.3-8
(*a*) Small signal model of Fig. 6.3-4*b* for common mode operation, (*b*) Simplified version of (*a*).

Using the relationship that $v_{gs} = v_g - v_s$, we may write

$$v_{gs} = \frac{1}{1 + 2g_{m1}r_{ds5}} v_c \tag{6.3-47}$$

The voltage, v_{d2}, can be found by the superposition of the two sources, v_{gs}. The problem is considerably simplified if we ignore r_{ds1} and r_{ds2}. Therefore, the voltage gain, v_{d2}/v_c, can be expressed as

$$\frac{v_{d2}}{v_c} = A_{vc} \simeq \frac{-g_{m1}r_{ds3}}{1 + 2g_{m1}r_{ds5}} \tag{6.3-48}$$

The common-mode voltage gain of the circuit of Fig. 6.3-4*a* can be found in a similar manner. However, the preceding method does not work for the differential amplifier of Fig. 6.3-4*c* because there is no point at which the single-ended output is available. In practice, Fig. 6.3-4*c* will exhibit a nonzero common-mode gain because of the fact that M1 and M2, and M3 and M4 are not perfectly matched. The mismatch effect for the differential amplifiers of Fig. 6.3-4*a* and Fig. 6.3-4*b* may dominate the actual common-mode gain.

The common-mode rejection ratio can be found by using the definition given earlier in this section. For the differential amplifier of Fig. 6.3-4*b*, the CMRR is found to be

$$\text{CMRR} = \frac{|A_{vds}|}{|A_{vc}|} = \frac{g_{ds3}(1 + 2g_{m1}r_{ds5})}{g_{ds2} + g_{ds4}} \tag{6.3-49}$$

If $g_{ds2} \simeq g_{ds3} \simeq g_{ds4}$, then the CMRR of Fig. 6.3-4*b* becomes approximately equal to $g_{m1}r_{ds5}$. It is desirable to have the CMRR as large as possible, which suggests that if r_{ds5} or g_{m1} can be increased, the differential amplifier will have a greater ability to reject the common-mode signal in favor of the differential-mode signal.

6.3.2 BJT Differential Amplifiers

The preceding concepts concerning the differential amplifier can also be applied to bipolar technology. Figure 6.3-9 shows a general bipolar differential amplifier configuration similar to that of Fig. 6.3-1 for MOS technology. We will briefly illustrate some of the large signal and small signal properties of the BJT differential amplifier. Under the assumption that Q1 and Q2 are operating in the forward active region and that the Early voltage effects are negligible, it follows from Eqs. 3.3-10 and 3.3-11 that the large signal characteristics can be found from the following relationships:

$$V_{ID} = V_{B1} - V_{B2} = V_{BE1} - V_{BE2} = V_t \ln\left(\frac{I_{C1}}{I_{S1}}\right) - V_t \ln\left(\frac{I_{C2}}{I_{S2}}\right) = V_t \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{6.3-50}$$

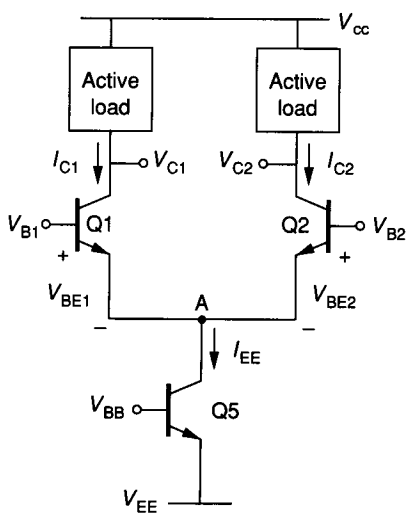


FIGURE 6.3-9
A general configuration for a BJT differential amplifier.

$$I_{EE} = \frac{I_{C1}}{\alpha_F} + \frac{I_{C2}}{\alpha_F} \tag{6.3-51}$$

where we have assumed that Q1 and Q2 are matched ($I_{S1} = I_{S2}$ and $\alpha_{F1} = \alpha_{F2} = \alpha_F$), and $V_t = kT/q$. Solving for I_{C1} and I_{C2} results in the following.

$$I_{C1} = \frac{\alpha_F I_{EE}}{1 + \exp(-V_{ID}/V_t)} \tag{6.3-52}$$

$$I_{C2} = \frac{\alpha_F I_{EE}}{1 + \exp(V_{ID}/V_t)} \tag{6.3-53}$$

From these two equations, it follows as in the MOS case that I_{C1} and I_{C2} are independent of the common mode excitation and the characteristics of the active load. Figure 6.3-10 shows a plot of the normalized collector current of Q1 and Q2 as a function of V_{ID}/V_t. The range of linear operation is seen to be limited to $|V_{ID}| \leq 2V_t$, or approximately ± 50 mV at room temperature.

Differentiating Eq. 6.3-52 gives the differential-in, single-ended transconductance as

$$g_m = -\frac{\alpha_F I_{EE}}{2V_t}\left[\frac{1}{1 + \cosh(V_{ID}/V_t)}\right] \tag{6.3-54}$$

If V_{ID} is set to zero, we obtain

$$g_m(V_{ID} = 0) = \frac{-\alpha_F I_{EE}}{4V_t} \tag{6.3-55}$$

The differential-in, differential-out transconductance (g_{md}) is found by multiplying the expressions given in Eqs. 6.3-54 and 6.3-55 by 2.

The large signal limits for the input and output of the BJT differential amplifier are found in a similar manner as for the MOS differential amplifier. The

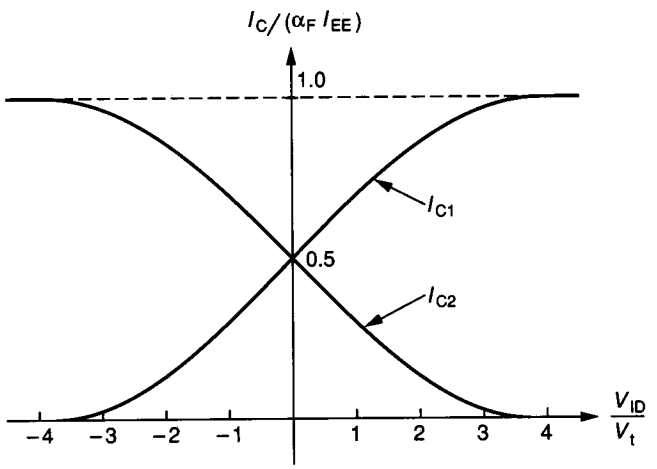


FIGURE 6.3-10
Large signal transconductance characteristics of the BJT differential amplifier.

objective again is to keep the BJT devices in the forward active region of operation, that is, the BE junction forward-biased and the BC junction reverse-biased.

Figure 6.3-11 shows the BJT differential amplifier that is topologically identical to the MOS differential amplifier of Fig. 6.3-4*c*. Assume that $V_{B1} = V_{B2}$. The highest value of V_{B1} is equal to

$$V_{B1}(\max) \simeq V_{CC} - V_{BE3} - V_{CE2}(\text{sat}) + V_{BE2} = V_{CC} - 0.2 \text{ V} \quad (6.3\text{-}56)$$

This relationship was developed under the conditions where Q1 is saturated. The lowest value of V_{B1} is given by

$$V_{B1}(\min) \simeq V_{BE1} + V_{CE5}(\text{sat}) + V_{EE} = V_{EE} + 0.8 \text{ V} \quad (6.3\text{-}57)$$

The output voltage of the circuit of Fig. 6.3-11 is limited to the range between

$$V_O(\max) \simeq V_{CC} - V_{CE4}(\text{sat}) = V_{CC} - 0.2 \text{ V} \quad (6.3\text{-}58)$$

and

$$V_O(\min) \simeq V_{B2} - 0.5\ V \quad (6.3\text{-}59)$$

where V_{B2} is the dc potential connected to the base of Q2.

Figure 6.3-12*a* shows a model suitable for small signal differential input excitation of the circuit of Fig. 6.3-11 neglecting r_μ and the frequency-dependent parameters of the model. If Q1 and Q2 are matched, we can assume that $r_{\pi 1} = r_{\pi 2} = r_\pi$, $g_{m1} = g_{m2}$, and $v_{be1} = -v_{be2}$. Neglecting the contribution of current through r_{o1} and r_{o2} into their common node allows the simplification of the small signal model to that shown in Fig. 6.3-12*b*. Since there is no ac current flowing through r_{o5}, it may be neglected. Also, we have replaced the current source, $g_{m3}v_{be3}$, by a resistor of $1/g_{m3}$ since v_{be3} is the voltage across this source. The final simplified small signal model for the BJT differential amplifier shown in Fig. 6.3-11 is given in Fig. 6.3-12*c*. The differential-out, differential-in voltage gain is

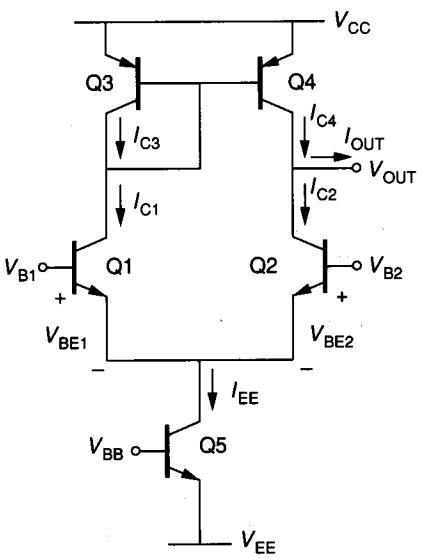


FIGURE 6.3-11
Practical version of the BJT differential amplifier.

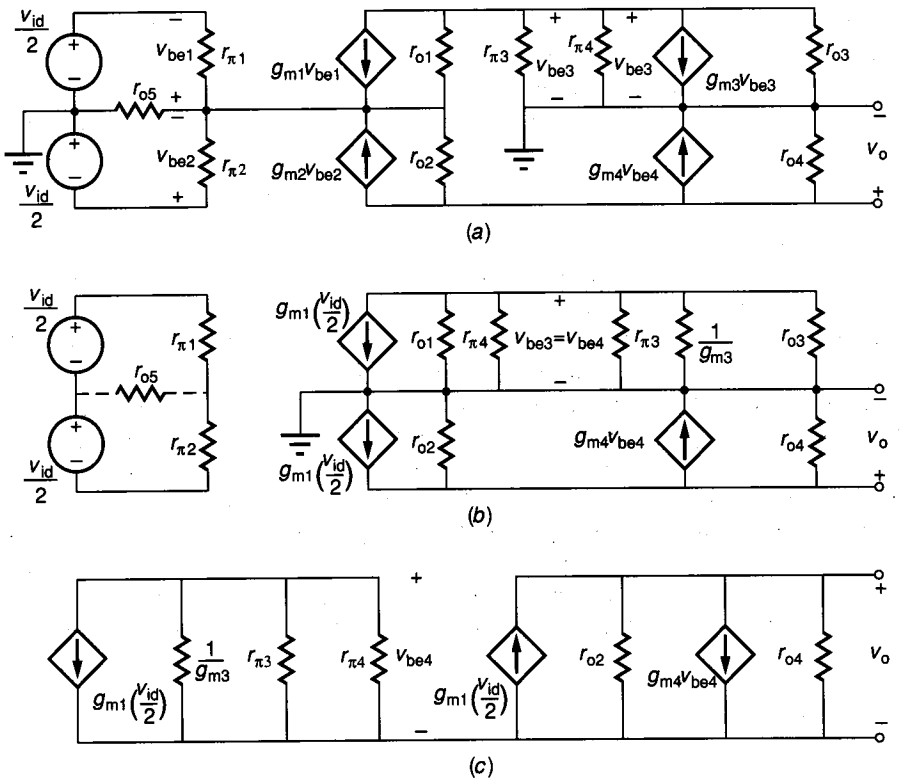


FIGURE 6.3-12
Small signal model for the BJT differential amplifier of Fig. 6.3-11: (*a*) Complete small signal model, (*b*) Simplification of (*a*), (*c*) Final small signal model.

$$\frac{v_o}{v_{id}} = A_{vdd} = \frac{1}{2}\left[g_{m1} + \frac{g_{m1}g_{m4}}{g_{m3} + g_{\pi 3} + g_{\pi 4}}\right]\left[\frac{1}{g_{o2} + g_{o4}}\right] \tag{6.3-60}$$

If we assume that Q3 and Q4 are matched, then $g_{m3} = g_{m4}$, and since g_{m3} is larger than $g_{\pi 3}$ or $g_{\pi 4}$, Eq. 6.3-60 can be simplified to

$$A_{vdd} \simeq \frac{g_{m1}}{g_{o2} + g_{o4}} = \frac{1}{(V_t/V_{AFN}) + (V_t/V_{AFP})} \tag{6.3-61}$$

where V_{AN} and V_{AP} are the Early voltages defined for the npn and pnp bipolar junction transistors. The small signal, differential-in, differential-out voltage gain of Fig. 6.3-11 is seen to be equal in magnitude to the BJT inverter of Sec. 6.1 (see Eq. 6.1-71). The small signal output resistance of the circuit of Fig. 6.3-11 is found as

$$r_{out} = \frac{1}{g_{o2} + g_{o4}} = \frac{1}{(I_{C2}/V_{AFN}) + (I_{C4}/V_{AFP})} = \frac{2V_{AFN}V_{AFP}}{I_{EE}(V_{AFN} + V_{AFP})} \tag{6.3-62}$$

The differential input resistance of the circuit of Fig. 6.3-11 can be expressed as

$$r_{id} = 2r_{\pi 1} = \frac{\beta_F V_t}{I_{C1}} = \frac{2\beta_F V_t}{I_{EE}} \tag{6.3-63}$$

A BJT differential amplifier topologically identical to the MOS differential amplifier of Fig. 6.3-4*b* is shown in the circuit of Fig. 6.3-13. A biasing scheme using Q6, R_{BIAS}, and Q7 is illustrated. It can be shown that the differential-in, single-ended-out voltage gain is given by

$$A_{vds} = \frac{v_{c1}}{v_{id}} = \frac{-g_{m1}r_{o1}r_{o3}}{r_{o1} + r_{o3}} \tag{6.3-64}$$

The common-mode voltage gain of Fig. 6.3-13 can be found by use of the small signal model shown in Fig. 6.3-14*a*. If we assume that Q1 and Q2 are matched and neglect the contribution of currents through r_{o1} and r_{o2}, we obtain the following relationships between v_c and v_{be}.

$$v_{be} = \frac{v_c}{1 + 2(g_{m1} + g_{\pi 1})r_{o5}} \tag{6.3-65}$$

The voltage at the collector of Q1 may be written as

$$v_{c1} \simeq -g_{m1}r_{o3} \tag{6.3-66}$$

where we have neglected r_{o1} and r_{o2}. Combining Eqs. 6.3-65 and 6.3-66 gives the common-mode voltage gain, A_{vc}, for Fig. 6.3-13 as follows.

$$A_{vc} = \frac{-g_{m1}r_{o3}}{1 + 2(g_{m1} + g_{\pi 1})r_{o5}} \simeq \frac{-g_{m1}r_{o3}}{1 + 2g_{m1}r_{o5}} \tag{6.3-67}$$

The common-mode gain for the BJT differential amplifier of Fig. 6.3-11 is theoretically zero because the only output node is differential, similar to Fig. 6.3-4*c*. Mismatch effects will the common-mode gain to be nonzero.

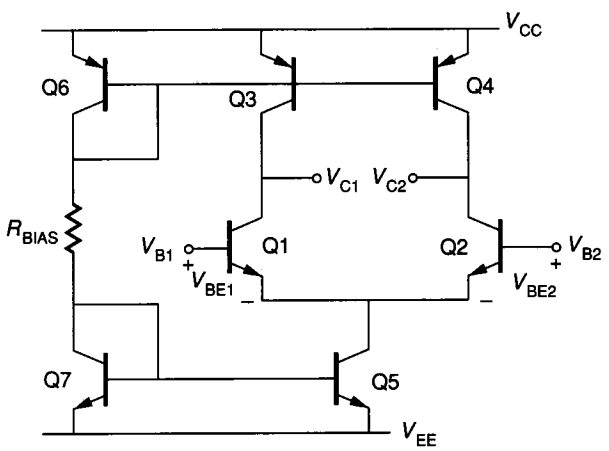


FIGURE 6.3-13
BJT differential amplifier using current-source active loads and illustrating one possible bias method.

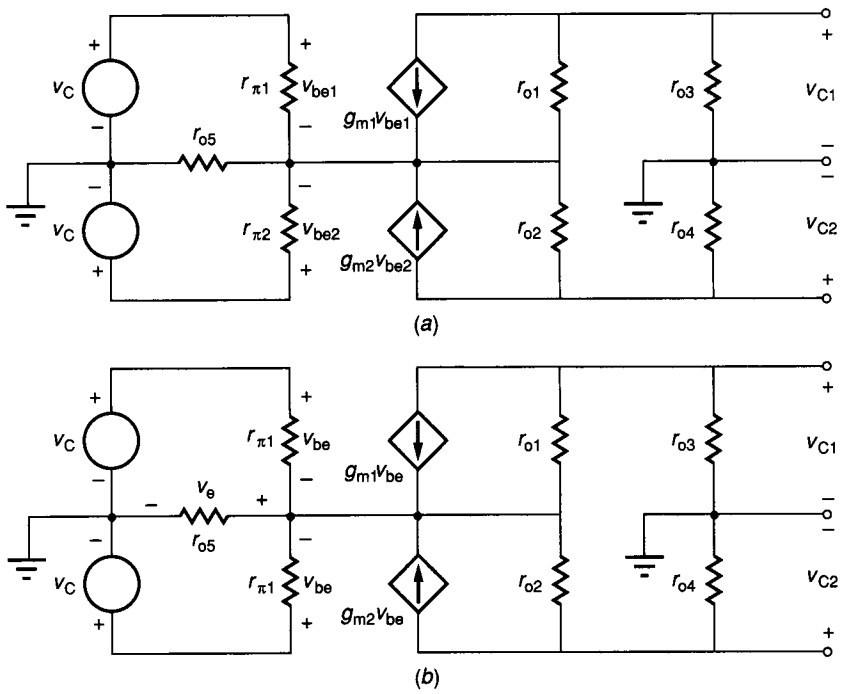


FIGURE 6.3-14
(*a*) Small signal model of Fig. 6.3-13 for common-mode operation, (*b*) Simplified version of (*a*).

The low-frequency CMRR for Fig. 6.3-13 can be found from Eqs. 6.3-64 and 6.3-67 and is expressed as

$$\text{CMRR} = \frac{|A_{vds}|}{|A_{vc}|} \simeq \frac{r_{o1}(1 + g_{m1}r_{o5})}{2(r_{o1} + r_{o3})} \simeq \frac{1 + g_{m1}r_{o5}}{4} \tag{6.3-68}$$

It is seen that as g_{m1} or r_{o5} increases, the CMRR will increase. The CMRR can be increased using a current sink with an output resistance greater than r_{o5}.

6.3.3 Frequency Response of Differential Amplifiers

The next subject of this section will be the frequency response of the differential amplifier. Figure 6.3-15*a* shows a frequency-dependent model of the differential-mode operation of either the MOS or BJT differential amplifier shown in Fig. 6.3-4*b* or 6.3-13, respectively. This model is suitable for finding v_{d1}/v_{id} or v_{d2}/v_{id}. For the MOS differential amplifier of Fig. 6.3-4*b*, R_1 is given in terms of Fig. 6.3-4*b* as

$$R_1 = r_{ds1} || r_{ds3} \tag{6.3-69}$$

and C_1 is given by

$$C_1 = C_{gd1} + C_{gd3} + C_{db1} + C_{db3} + C_L \tag{6.3-70}$$

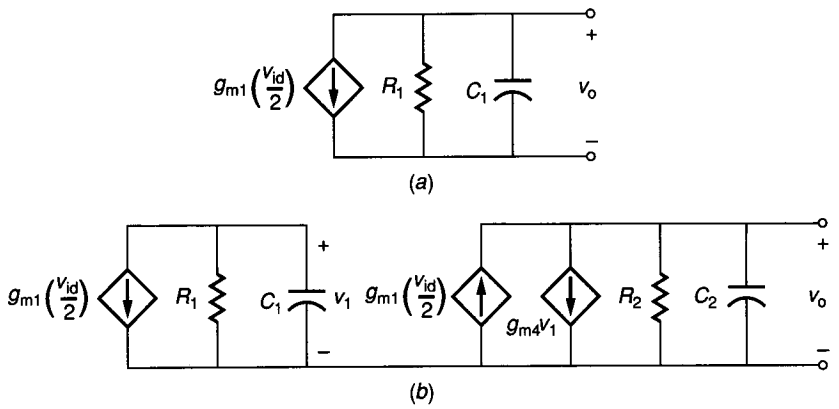


FIGURE 6.3-15
Frequency-dependent models for: (*a*) Differential amplifiers of Fig. 6.3-4*b* and Fig. 6.3-13, (*b*) Differential amplifiers of Fig. 6.3-4*c* and Fig. 6.3-11.

where C_L is the load capacitance attached to the junction of the drains of M1 and M3. If the output voltage is taken at v_{d2}, then the subscripts 1 and 3 of Eqs. 6.3-69 and 6.3-70 should be replaced by 2 and 4, respectively.

For the BJT differential amplifier of Fig. 6.3-13, the values of R_1 and C_1 are

$$R_1 = r_{o1} || r_{o3} \tag{6.3-71}$$

and

$$C_1 = C_{\mu 1} + C_{CS1} + C_{CS3} + C_{\mu 3} + C_L \tag{6.3-72}$$

The same comment regarding subscript interchange holds for the BJT differential amplifier of Fig. 6.3-13.

The differential-mode frequency response of the circuit of Fig. 6.3-15*a* can be written as

$$A_{vds}(s) = \frac{A_{vds}(0)\omega_1}{s + \omega_1} = \frac{A_{vds0}\omega_1}{s + \omega_1} \tag{6.3-73}$$

where

$$A_{vds0} = -g_{m1}R_1 \tag{6.3-74}$$

and

$$\omega_1 = \frac{1}{R_1 C_1} \tag{6.3-75}$$

For a MOS differential amplifier with $I_{SS} = 100\ \mu A$, $\lambda = 0.01\ V^{-1}$, $C_{db} = 100$ fFg, $C_{gs} = 0.2$ pF, $C_{gd} = 50$ pF, and $C_L = 0.5$ pF, we find that $R_1 = 1\ M\Omega$ and $C_1 = 0.8$ pF. The -3 dB frequency of this MOS differential amplifier is 199 kHz. If $I_{EE} = 100\ \mu A$, $V_{AFN} = 100$ V, $V_{AFP} = 50$ V, $C_\mu = 1$ pF, $C_{CS} = 1$ pF,

and $C_L = 5$ pF, then R_1 and C_1 are 0.667 MΩ and 9 pF, respectively. This gives a -3 dB frequency of 26.5 kHz for the BJT differential amplifier.

The differential-mode frequency response of the MOS differential amplifier of Fig. 6.3-4*c* and the BJT differential amplifier of Fig. 6.3-11 can be found from the small signal model given in Fig. 6.3-15*b*. For the MOS version, R_1, R_2, C_1, and C_2 can be written as

$$R_1 = \frac{1}{g_{m3}} || r_{ds1} || r_{ds3} \simeq \frac{1}{g_{m3}} \tag{6.3-76}$$

$$R_2 = r_{ds2} || r_{ds4} \tag{6.3-77}$$

$$C_1 = C_{gd1} + C_{gs3} + C_{gs4} + C_{bd1} + C_{b23} \tag{6.3-78}$$

and

$$C_2 = C_{gd2} + C_{gd4} + C_{bd2} + C_{bd4} + C_L \tag{6.3-79}$$

For the BJT differential amplifier, R_1, R_2, C_1, and C_2 are

$$R_1 = \frac{1}{g_{m3}} || r_{o3} || r_{\pi 3} || r_{\pi 4} || r_{o1} \simeq \frac{1}{g_{m3}} \tag{6.3-80}$$

$$R_2 = r_{o2} || r_{o4} \tag{6.3-81}$$

$$C_1 = C_{\mu 1} + C_{CS1} + C_{\pi 3} + C_{\pi 4} + C_{CS3} \tag{6.3-82}$$

and

$$C_2 = C_{\mu 2} + C_{CS2} + C_{\mu 4} + C_{CS4} + C_L \tag{6.3-83}$$

The frequency response for Fig. 6.3-15*b* can be written as

$$A_{vds}(s) = \frac{v_o}{v_{id}} = \frac{-g_{m1}R_2\omega_2}{2(s + \omega_2)}\left[1 + \frac{g_{m4}R_1\omega_1}{s + \omega_1}\right] =$$

$$\frac{-g_{m1}R_2\omega_2[s + \omega_1(1 + g_{m4}R_1)]}{2(s + \omega_1)(s + \omega_2)} = \frac{A_{vds0}[(s/\omega_1') + 1]}{[(s/\omega_1 + 1)][(s/\omega_2) + 1]} \tag{6.3-84}$$

where

$$A_{vds0} = -0.5g_{m1}R_2(1 + g_{m4}R_1) \tag{6.3-85}$$

$$\omega_1 = \frac{1}{R_1C_1} \tag{6.3-86}$$

$$\omega_1' = (1 + g_{m4}R_1)\omega_1 \tag{6.3-87}$$

and

$$\omega_2 = \frac{1}{R_2C_2} \tag{6.3-88}$$

It is of interest to note that the configuration of Fig. 6.3-15*b* introduces an extra pole-zero pair. The zero is in the left-hand plane and is equal to $(1 + g_{m4}R_1)$ times the pole. Since R_1 is approximately equal to the value of $1/g_{m3}$, the value of the zero is approximately twice that of the pole (called a *doublet*). In most cases, the effect of ω_1 and ω_2' approximately cancel each other out. Assume that $K_N' = 2K_P' = 25\ \mu A/V^2$, all W/L ratios are unity $C_{gs} = 100$ fF, and $I_{SS} = 100\ \mu A$. The MOS parameters used earlier permit the calculation of R_1, R_2, C_1, and C_2 as 19.6 kΩ, 1 MΩ, 0.35 pF, and 0.8 pF, respectively. This leads to a low-frequency gain magnitude of 100 and a −3 dB frequency of 199 kHz. If the current gain of the BJTs is $\beta_F = 100$, $C_\pi = 5$ pF, and $I_{EE} = 100\ \mu A$, using the previous parameters permits the calculation of R_1, R_2, C_1, and C_2 for the BJT differential amplifier as 490 Ω, 0.67 MΩ, 13 pF, and 9 pF, respectively. This gives a low-frequency gain magnitude of 1340 and a −3 dB frequency of 26.4 kHz.

6.3.4 Noise Performance of Differential Amplifiers

The last consideration of this section deals with the noise performance of the differential amplifier. Because of the similarity in small signal performance between the differential amplifier and the inverting amplifier, we expect the noise performance to be similar. Let us consider the noise analysis of Fig. 6.3-4*c* and Fig. 6.3-11. The noise models for each of these circuits are shown in Fig. 6.3-16. The noise of I_{SS} and I_{EE} is neglected because they are common-mode inputs and have a much smaller influence on the output noise. A dc battery, V_{out}, has been connected to the output through which an output-noise-current spectral density flows. It can be shown for both amplifiers that

$$\overline{I}_{on}^2 = g_{m1}^2 \overline{V}_{n1}^2 + g_{m2}^2 \overline{V}_{n2}^2 + g_{m3}^2 \overline{V}_{n3}^2 + g_{m4}^2 \overline{V}_{n4}^2 \tag{6.3-89}$$

This result is developed by using superposition techniques. The equivalent input-noise-voltage spectral density can be found by dividing Eq. 6.3-89 by g_{m1}^2 to get

$$S_{eq} = S_{VN1} + S_{VN2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 (S_{VN3} + S_{VN4}) \tag{6.3-90}$$

where $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$ has been assumed. Assuming that $S_{VN1} = S_{VN2}$ and $S_{VN3} = S_{VN4}$ gives

$$S_{eq} = 2S_{VN1}\left[1 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{S_{VN3}}{S_{VN1}}\right)\right] \tag{6.3-91}$$

Although the type of noise has not been identified, in general the noise will be reduced if $g_{m3} \leq g_{m1}$.

The differential amplifier is a very useful building block which will be used in analog circuits that follow. The differential amplifier is an excellent choice as an input stage for several reasons. It allows the application of difference signals and rejects the common mode signals. This means that an unwanted singal

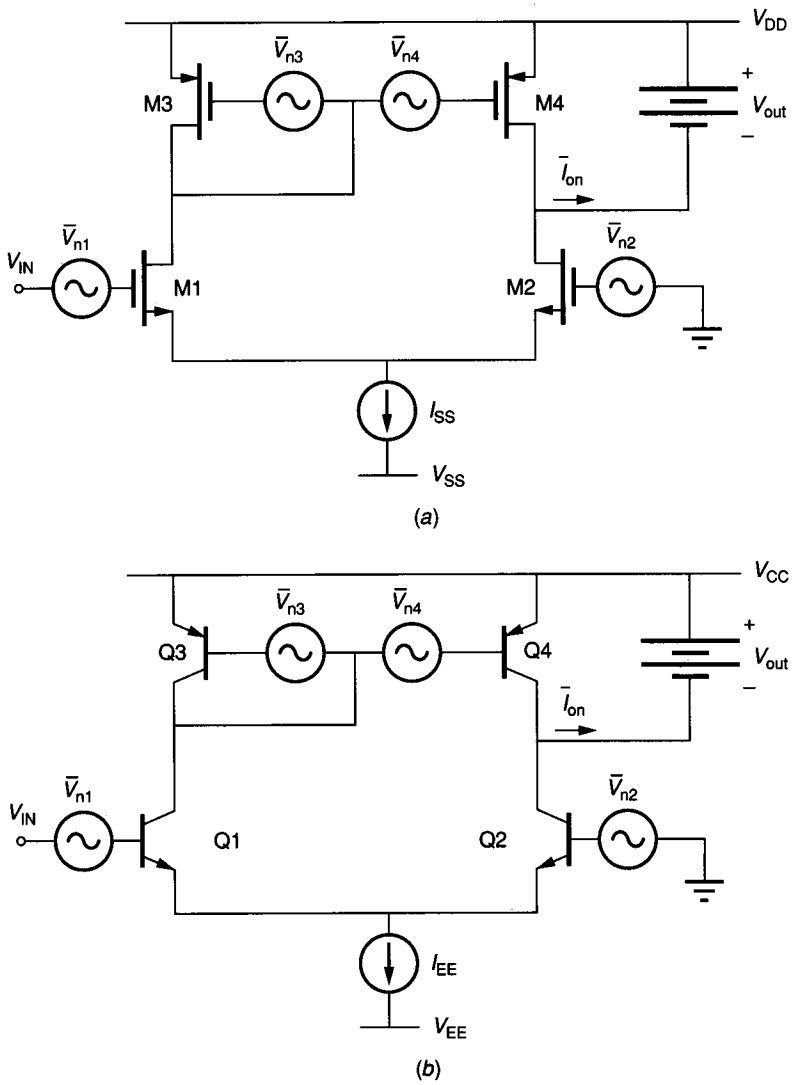


FIGURE 6.3-16
(*a*) Noise model for the CMOS differential amplifier of Fig. 6.3-4*c*. (*b*) Noise model for the BJT differential amplifier of Fig. 6.3-11.

present at both inputs will be rejected. The large input common-mode range allows the ac performance to be independent of the dc input voltage. A third advantage is that larger output signal swings can be obtained differentially. This is important as the trend to reduce power supplies makes it difficult to have sufficient dynamic range. Table 6.3-1 summarizes the performance of the differential amplifiers presented in this section.

TABLE 6.3-1
Comparison of small signal voltage gains for the differential amplifiers of Sec. 6.3

Differential amplifier	Figure	Differential-in, single-ended-out voltage gain, A_{vds}	Differential-in, differential-out voltage gain, A_{vdd}
MOS active load	6.3-4*a*	$\frac{g_{m1}}{2g_{m3}}$	$\frac{g_{m1}}{g_{m3}}$
MOS current source load	6.3-4*b*	$\frac{g_{m1}}{2(g_{ds2} + g_{ds4})}$	$\frac{g_{m1}}{g_{ds2} + g_{ds4}}$
MOS current mirror load	6.3-4*c*	$\frac{g_{m1}}{g_{ds2} + g_{ds4}}$	—
BJT current mirror load	6.3-11	$\frac{g_{m1}}{g_{o2} + g_{o4}}$	—
BJT current source load	6.3-13	$\frac{g_{m1}}{2(g_{o1} + g_{o3})}$	$\frac{g_{m1}}{g_{o1} + g_{o3}}$

6.4 OUTPUT AMPLIFIERS

In many applications, the output load of a circuit can significantly influence the performance of the circuit. The output load generally consists of a load resistor, R_L, in parallel with a load capacitor, C_L. If R_L is small or if C_L is large, the previous amplifiers may not be able to meet the output signal requirements. The objective of an output amplifier is to provide a large output voltage swing across the load. The requirements of the output amplifier can be divided into static requirements and dynamic requirements. The static requirement can be stated as the ability to maintain a dc voltage somewhere between the power supply limits across a specified load resistor. This implies that the output stage should have a low Thevenin output resistance and should be efficient in order to avoid large power dissipation in the amplifier. The dynamic requirement is the ability to charge or discharge a large capacitance at a specified voltage rate. This requirement is often associated with slew rate or the maximum output voltage rate of an analog circuit. The dynamic requirement does not require a low output resistance but does demand high currents to achieve the desired slew rate.

There are two distinct approaches to implementing output stages. These approaches depend on whether or not feedback is used. We will first consider the approach that does not use feedback. The first nonfeedback output amplifier type consists of the inverting amplifiers of Sec. 6.1. We will examine the large signal performance of these amplifiers to determine their suitability as output amplifiers. Figures 6.1-11*a*, 6.1-11*b*, 6.1-11*c*, and 6.1-18*a* represent the inverting amplifiers we will consider. In Sec. 6.1 we analyzed the small signal performance. Since the output amplifier is likely to have large output voltage swings, let us first consider the limitations of the output stage.

6.4.1 Output Amplifiers without Feedback

A conservative approach to characterize the output signal swings of MOS amplifiers is to assume that all devices must be in saturation. This constrains the operation to the transition region of the voltage transfer function of the amplifier. Figures 6.1-12 and 6.1-14 show that the resulting output range is not as large as that which could be achieved if some of the devices are allowed to operate in the active or ohmic region.

Consider the output swing limits of Fig. 6.1-11*a*. We assume that V_{IN} can have values between V_{DD} and V_{SS}. (This aggressive assumption partially compensates for the conservative approach of assuming all devices are saturated.) When $V_{IN} = V_{SS}$, M1 is off and the maximum output voltage is

$$V_{OUT}(\max) \approx V_{DD} - |V_{TP}| \tag{6.4-1}$$

When $V_{IN} = V_{DD}$, M1 is on and in fact is in the ohmic region because V_{DS1} will be small. The current in M2 which is in the saturation region is

$$I_{D2} = \frac{\beta_2}{2}(V_{SG2} - |V_{TP}|)^2 = \frac{\beta_2}{2}(V_{DD} - V_{OUT} - |V_{TP}|)^2 = \frac{\beta_2}{2}(V_{OUT} - V_{DD} + |V_{TP}|)^2 \tag{6.4-2}$$

The current in M1 is

$$\begin{aligned} I_{D1} &= \beta_1\left[(V_{GS1} - V_{TN})V_{DS1} - \frac{V_{DS1}^2}{2}\right] \\ &= \beta_1\left[(V_{DD} - V_{SS} - V_{TN})(V_{OUT} - V_{SS}) - \frac{(V_{OUT} - V_{SS})^2}{2}\right] \end{aligned} \tag{6.4-3}$$

Equating Eq. 6.4-2 to Eq. 6.4-3 and solving for V_{OUT} gives

$$V_{OUT}(\min) = V_{DD} - V_T - \frac{V_{DD} - V_{SS} - V_T}{\sqrt{1 + (\beta_2/\beta_1)}} \tag{6.4-4}$$

where it has been assumed that $V_T = V_{TN} = |V_{TP}|$. Using the model parameters and voltages specified in Fig. 6.1-12 the above equations give a $V_{OUT}(\max)$ of 4.25 V and a $V_{OUT}(\min)$ of -4.52 V. If we used the saturation constraint, the lower voltage limit would be higher (approximately -2.8 V).

The MOS inverting amplifier of Fig. 6.1-11*c* has approximately the same large signal behavior, with one exception. Because the source of M2 is not connected to the bulk, V_{T2} will be larger than normal, causing the maximum value of V_{OUT} to be less, as seen from Eq. 6.4-1.

The MOS inverting amplifier of Fig. 6.1-11*b* has a higher ac gain than the previous two amplifiers. It can be seen that when $V_{IN} = V_{SS}$, M1 is off and V_{OUT} is at V_{DD}. Therefore,

$$V_{OUT}(\max) \approx V_{DD} \tag{6.4-5}$$

Using the approach outlined by Eqs. 6.4-2 and 6.4-3 we can show that

$$V_{OUT}(\min) = (V_{DD} - V_{SS} - V_{TN}) \cdot \left[1 - \sqrt{1 - \left(\frac{\beta_2}{\beta_1}\right)\left(\frac{V_{DD} - V_{GG2} - |V_{TP}|}{V_{DD} - V_{SS} - V_{TN}}\right)^2}\right] + V_{SS} \quad (6.4\text{-}6)$$

if $V_{IN} = V_{DD}$. Evaluating these limits under the conditions given in Fig. 6.1-14, we get $V_{OUT}(\max) \approx 5$ V and $V_{OUT}(\min) \approx -4.97$ V, which agree with the results of Fig. 6.1-14.

The maximum output swing of the BJT inverting amplifier of Fig. 6.1-18*a* can be found in a similar manner. When $V_{IN} = V_{EE}$, Q1 is off and V_{OUT} is at V_{CC}. Therefore,

$$V_{OUT}(\max) \approx V_{CC} \quad (6.4\text{-}7)$$

When V_{IN} is increased so that Q1 becomes saturated, then V_{OUT} is equal to

$$V_{OUT}(\min) \approx V_{SS} + V_{CE1}(\text{sat}) \approx V_{SS} + 0.2 \text{ V} \quad (6.4\text{-}8)$$

It is seen that the BJT inverting amplifiers generally have a larger output swing than the MOS inverting amplifiers.

The previous considerations emphasized the ability to have large output voltage swings. However, no load was considered, so the results just given are appropriate for large resistance loads. Of perhaps more importance is the signal swing for small values of load resistance. Unfortunately, this is difficult to analyze. Instead, let us examine the ability to source or sink current when the output swings are small. Once again we consider the inverting amplifiers. Figures 6.4-1*a* and *b* show MOS and BJT amplifiers using a current-source load sometimes called a "pull-up". It will be assumed that current flows in both output devices during the entire swing of the output voltage. This is called Class

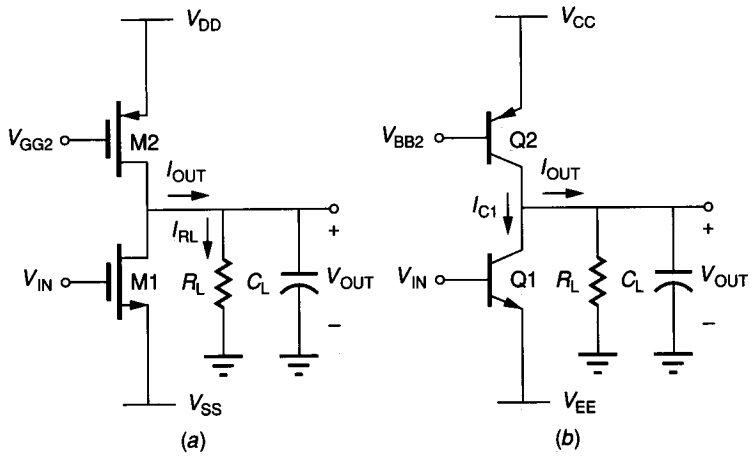


FIGURE 6.4-1
Class A output amplifiers: (*a*) Common-source configuration, (*b*) Common-emitter configuration.

A operation. Let us first consider the static performance (the ability to source and sink currents at a dc output voltage for which the output devices are both in saturation or forward active region).

The maximum source current, I_{OUT}^{+}, that can be obtained from the circuit of Fig. 6.4-1*a* occurs when M1 is off and M2 is saturated, is given as

$$I_{OUT}^{+} = \frac{K_P' W_2}{2L_2}[V_{DD} - V_{GG2} - |V_{T2}|]^2 \tag{6.4-9}$$

It is important to note that as long as M2 is saturated this current always flows in M2 regardless of the value of V_{IN}. The maximum sinking current, I_{OUT}^{-}, for Fig. 6.4-1*a* occurs when M1 is saturated and $V_{IN} = V_{DD}$ and is given as

$$I_{OUT}^{-} = \frac{K_N' W_1}{2L_1}(V_{DD} - V_{SS} - V_{T1})^2 - I_{OUT}^{+} \tag{6.4-10}$$

It should be observed that I_{OUT}^{-} must also include I_{OUT}^{+} because of the Class A nature of the biasing. Fortunately, the current-sinking capability of M1 can easily exceed I_{OUT}^{+} because the gate-source voltage of M1 can be very large.

If V_{OUT} approaches V_{SS}, then M1 will pass from the saturation to the ohmic region where $V_{DS1} < V_{GS1} - V_{T1}$. If a load resistance R_L is connected to the output, V_{DS1} is small, and $V_{IN} = V_{DD}$, then Eq. 6.4-10 for the ohmic region becomes

$$I_{D1} \approx \frac{K_N' W_1}{L_1}(V_{DD} - V_{SS} - V_{T1})(-I_{OUT}^{-} R_L - V_{SS}) \tag{6.4-11}$$

Since I_{D1} is the sum of I_{OUT}^{+} and I_{OUT}^{-}, we can solve for I_{OUT}^{-} as

$$I_{OUT}^{-} \approx \frac{-K_N'(W_1/L_1)(V_{DD} - V_{SS} - V_{T1})V_{SS} - I_{OUT}^{+}}{1 + K_N'(W_1/L_1)(V_{DD} - V_{SS} - V_{T1})R_L} \tag{6.4-12}$$

When V_{OUT} approaches V_{DD}, I_{OUT}^{+} will become dependent on R_L and have a smaller value than that of Eq. 6.4-9. Figure 6.4-2 shows a plot of the output voltage of the circuit of Fig. 6.1-11*b* as a function of the input for a 1 kΩ load resistor. Note that the *W/L* values have been increased to provide more current sinking and sourcing capability. Using the parameter values given in Fig. 6.4-2, I_{OUT}^{+} is 202 μA and I_{OUT}^{-} is 2.53 mA. When multiplied by 1 kΩ, these currents give the maximum output voltages. It is seen that the sinking current is approximately 10 times the sourcing current. The sourcing current could be increased by decreasing the gate voltage on M2 or increasing W_2/L_2. In either case, the bias current that flows would increase, causing the power dissipation in the inverter to increase. It should be noted that the load resistance of 1 kΩ has caused the inverter voltage gain to be less than unity.

The small signal output resistance of the inverting voltage amplifier is a measure of how the ac gain will be influenced by the presence of a small load resistance. For example, consider the MOS inverter of Fig. 6.1-11*b* with the parameters given in Fig. 6.4-2, where $R_L = 1$ kΩ. Using Eq. 6.1-50, we find that at $V_{OUT} = 0$ V the ac voltage gain should be −36.3, assuming that R_L is

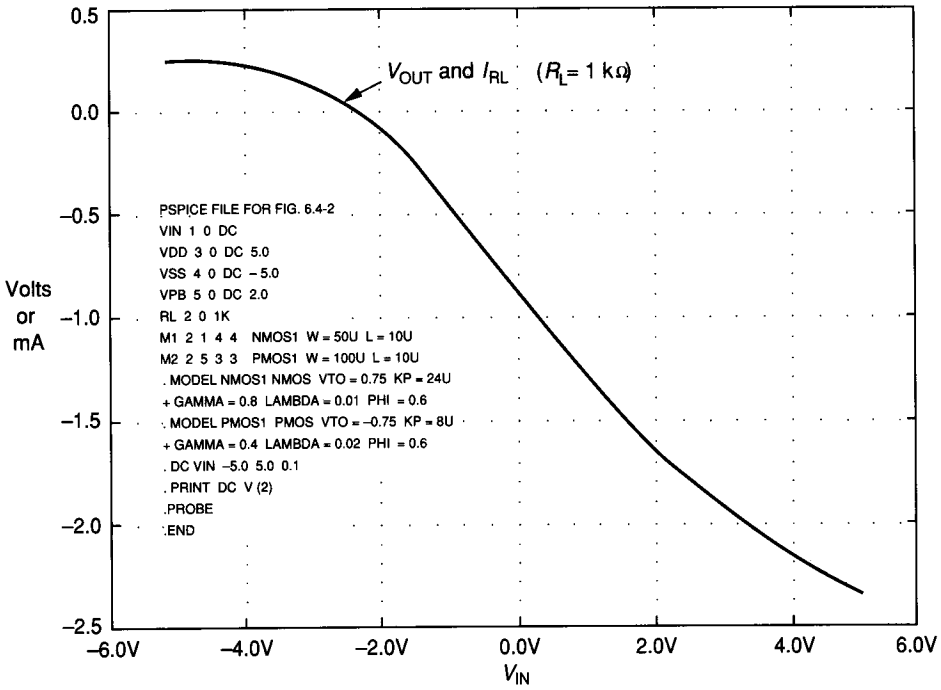


FIGURE 6.4-2
Simulation of Fig. 6.4-1*a*.

infinite. The output resistance under these conditions is found from Eq. 6.1-52 as $r_{out} = 165\ \text{k}\Omega$. When loaded with R_L, the new ac gain is given as

$$A_v' = A_v\left(\frac{R_L}{R_L + r_{out}}\right) \tag{6.4-13}$$

where A_v is the ac voltage gain for $R_L = \infty$ and A_v' is the gain for a finite R_L. In this case, A_v' is equal to $-36.3(1/166) = -0.22$. This value compares favorably with the simulated result of Fig. 6.4-2 at $V_{OUT} = 0$ V. Consequently, another desirable characteristic of an output amplifier is to have a small value of r_{out} so that the small signal voltage gain predicted by Eq. 6.4-13 is not reduced.

The maximum source/sink output currents and the ac output resistance characterize the static performance of the output amplifier. These two measures are related by the quiescent bias current (I_{BIAS}) of the amplifier. For example, suppose we want to sustain +4 V across a 10 kΩ load resistance. This would require an I_{BIAS} of at least 400 μA (assuming M1 is off). With a 400 μA bias current, the small signal output resistance is 125 kΩ if λ is 0.01 V^{-1}. Because of the large, small signal output resistance, the output of the common-source configuration is best modelled by a controlled current source in parallel with the 125kΩ output resistance.

Under dynamic conditions, the output sinking/sourcing current needed to charge or discharge C_L may be greater than that required to maintain a given dc

voltage across R_L. It is assumed in the following analysis that the output voltage is in the range where both output transistors are in saturation. The current required to charge a capacitor C_L at a rate of dV_{OUT}/dt is given by

$$| I_{OUT} | = C_L \left[\frac{dV_{OUT}}{dt} \right] \tag{6.4-14}$$

If the desired rate of rise is 10 V/μs and C_L is 50 pF, then the bias current must be at least 500 μA. This consideration is valid for $V_{OUT} \approx 0$. As the output voltage deviates from 0 V, the current available for charging C_L is reduced by the current necessary to sustain a nonzero value of V_{OUT} across R_L.

Similar conditions hold for the BJT Class A inverting voltage amplifier of Fig. 6.4-1*b*. The maximum sourcing current is determined by Q2 and is given as

$$I_{OUT}^{+} = I_{S2} \exp \left[\frac{V_{CC} - V_{BB2}}{V_t} \right] \tag{6.4-15}$$

There is an important distinction between this relationship and the similar one for the MOS amplifier in Eq. 6.4-9. That difference is that V_{BB2} must be able to sink from the base of Q2 a current of I_{OUT}^{+}/β_{F2}. Typically, Q2 is part of a current mirror so that I_{OUT}^{+} is defined by the input current to the mirror. The maximum sinking current can be determined as V_{IN} is increased. As V_{BE1} is increased, the sinking current becomes very large. A more appropriate measure of the sinking current would be to examine more closely the circuit that is driving the amplifier of Fig. 6.4-1*b*. In general, any driver can be characterized by an equivalent voltage source, V_S, and series resistance, R_S. The maximum sinking current can be expressed as

$$I_{OUT}^{-} = \left[\frac{V_S(\max) - V_{EE} - V_{BE1}}{R_S} \right] \beta_{F1} - I_{OUT}^{+} \tag{6.4-16}$$

where $V_S(\max)$ is the maximum positive swing of V_S and $V_{BE1} \approx 0.7$ V. Assuming $V_S(\max) \approx -2$ V and $R_S = 10$ kΩ for the conditions of Fig. 6.1-18*a* and Fig. 6.1-19, we get $I_{OUT}^{+} \approx 1.39$ mA and $I_{OUT}^{-} = 21.6$ mA. For a 1 kΩ load resistance, the output voltage swing would be from +1.39 V to −5 V. Figure 6.4-3 shows a simulation of the circuit of Fig. 6.4-1*b* using the same parameters as for Fig. 6.1-19, except that a load resistance of 1 kΩ has been added. We note that the current in Q1 increases from 0 to 6.6 mA, which is sufficient to overcome I_{OUT}^{+} and to sink 5 mA through $R_L = 1$ kΩ. We also note that the ac gain has been greatly reduced. The output sinking/sourcing analysis of Fig. 6.4-1*b* is similar to that of Fig. 6.4-1*a* and will not be repeated here.

The small signal output resistance can be used to predict the reduction of gain using Eq. 6.4-13. For example, the gain for $R_L = \infty$ and output resistance for the circuit of Fig. 6.4-1*b* were calculated in Example 6.1-4 for $V_{OUT} = 0$ V as −1544 and 26 kΩ, respectively. Using Eq. 6.4-13 we predict the new ac gain (at $V_{OUT} = 0$ V) as −57. This compares very well with the slope of Fig. 6.4-3 at $V_{OUT} = 0$.

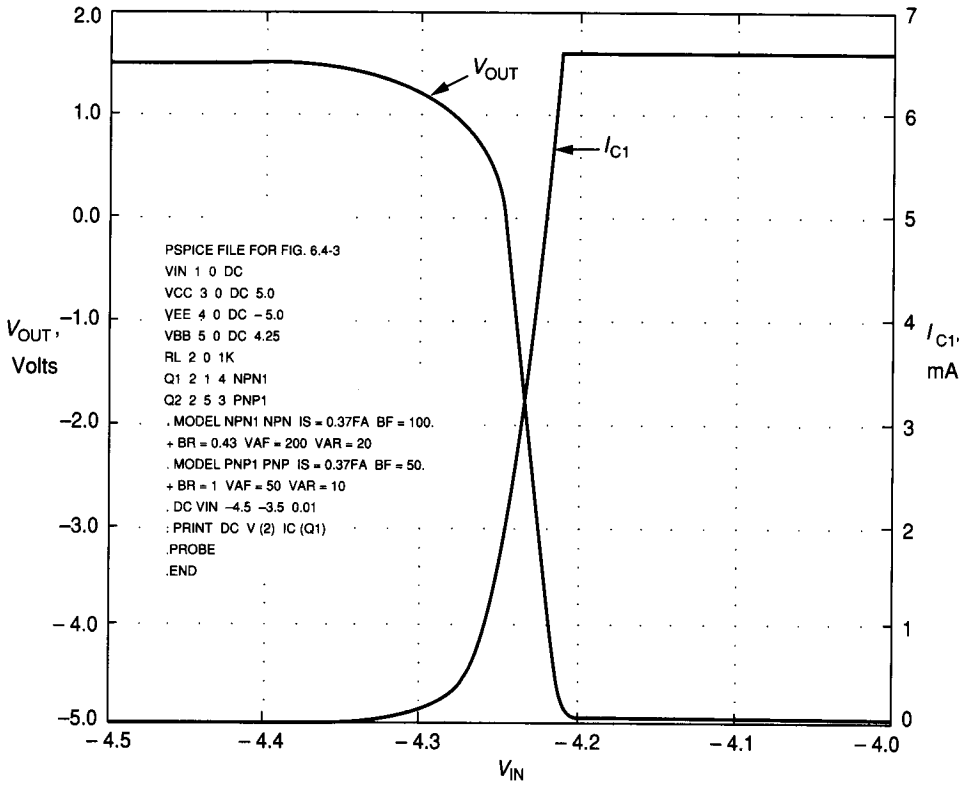


FIGURE 6.4-3
Simulation of Fig. 6.4-1*b*.

One of the disadvantages of the Class A inverting amplifiers of Fig. 6.4-1 is that considerable quiescent power is dissipated. It is well known that the maximum efficiency of the Class A amplifier is 25% for a sinusoidal signal. This means that under best conditions, for every milliwatt of ac power applied to R_L, 3 mW are dissipated in the transistors. For example, consider the two amplifiers of Fig. 6.4-1 with 1 kΩ load resistances. With the output signal at 0 V, the amplifier of Fig. 6.4-1*a* dissipates 2 mW and that of Fig. 6.4-1*b* dissipates 13.9 mW. The maximum symmetrical output voltage signal swing is 0.2 V (peak-to-peak) and 1.39 V (peak-to-peak) for Fig. 6.4-1*a* and *b*, respectively. Unfortunately, we have had to take the smaller of the positive or negative signal swing to avoid distortion. Assuming a sinusoidal output, the maximum power delivered to R_L is 0.04 mW and 1.93 mW, respectively. Correspondingly, the best sinusoidal efficiencies of the circuit of Fig. 6.4-1*a* and *b* are 2% and 13.9%, respectively. It is clear that the bias currents should be increased to reach the maximum output voltage signal swings if one wishes to approach more closely the maximum possible efficiency of 25%.

One advantage of the Class A amplifier is low distortion. This is a result of operating both MOS transistors in the saturation region or operating both BJT transistors in the normal active region over most of the output voltage swing.

A second method of implementing an output amplifier without feedback is the common-source or common-emitter, Class B or Class AB amplifiers. The circuits of Fig. 6.4-4*a* and *b* show MOS and BJT implementations, respectively. V_B is a floating battery used to establish the proper bias of the devices. The sinking/sourcing output current capability of such amplifiers is very large and is limited primarily by the power dissipation capability of the devices. If the transistors are biased so that no drain or collector current flows when V_{IN} is zero, the stage is termed Class B. When V_{IN} is positive, the lower device is on and the upper device is off. When V_{IN} is negative, the lower device is off and the upper device is on. The maximum possible efficiency of the Class B amplifier for a sinusoidal output signal is 78.5%, where the efficiency is defined as the ratio of the signal power dissipated in R_L to the power provided from the power supplies for sinusoidal input.

The primary advantage of the implementations of Fig. 6.4-4 is that the maximum sourcing/sinking current is not limited by the bias current. This allows output amplifiers to have I_{OUT}^{-} limitations similar to the I_{OUT}^{+} levels of the Class A output amplifiers. Figure 6.4-5 shows the simulated output swing capability for the circuit of Fig. 6.4-4*a* with $V_B = 0$, $W_1/L_1 = 50\ \mu/10\ \mu$, $W_2/L_2 = 150\ \mu/10\ \mu$, and $R_L = 1\ \text{k}\Omega$. This circuit has a maximum sink/source current limit given by Eq. 6.4-12 of 2.53 mA, resulting in a ±2.53 V output signal swing. These calculations agree well with the simulation results of Fig. 6.4-5. The drain

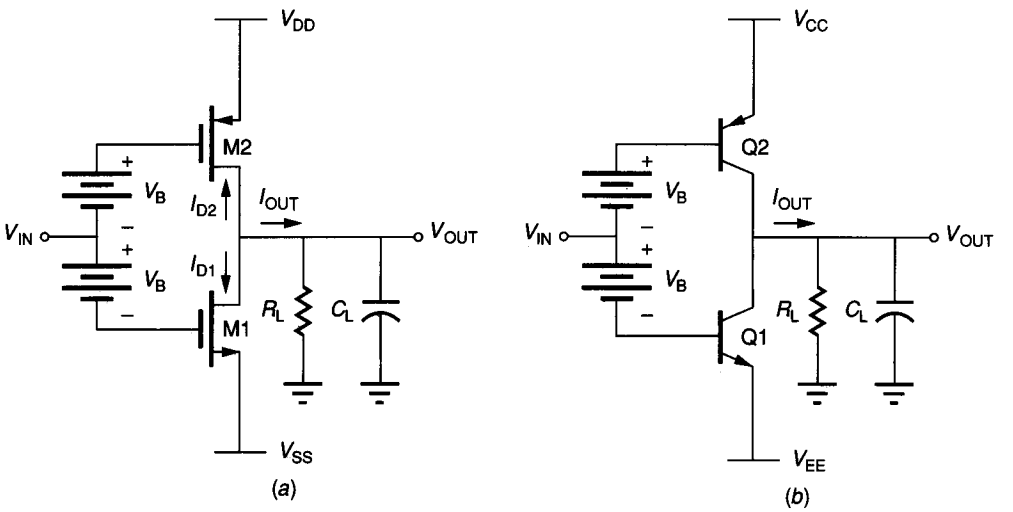


FIGURE 6.4-4
Class B and AB output amplifiers: (*a*) MOS common-source configuration, (*b*) BJT common-emitter configuration.

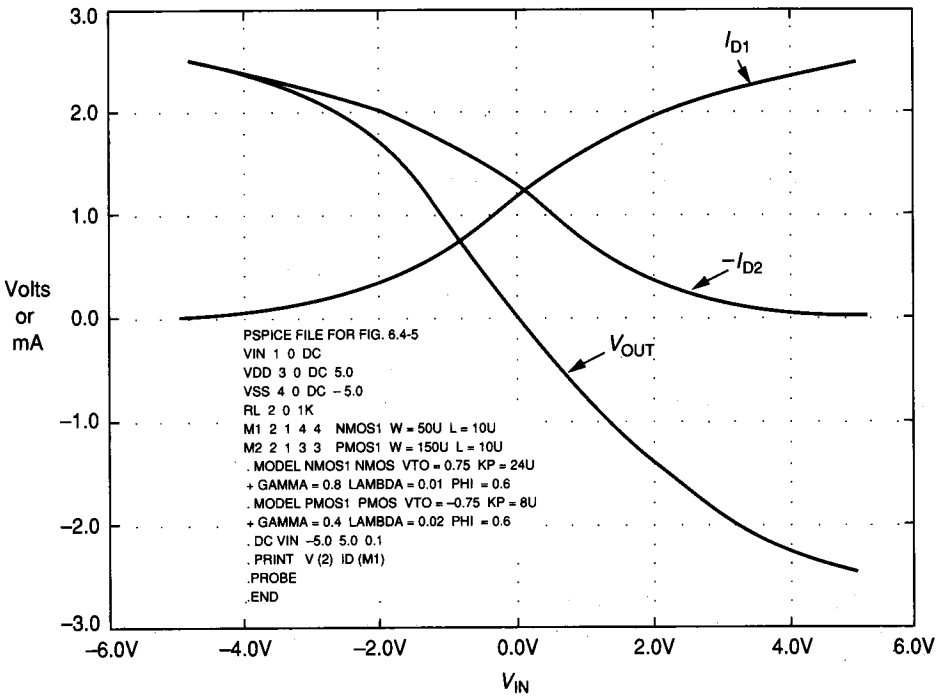


FIGURE 6.4-5
Simulation of Fig. 6.4-4*a* with $V_B = 0$ V.

currents in M1 and M2 are also plotted in Fig. 6.4-5. Because both M1 and M2 are conducting in the region around $V_{IN} \approx 0$, this amplifier is called Class AB. The results of Fig. 6.4-5 can be used to show that if $V_B \approx 4$ V, then the amplifier will be operating in Class B mode. Figure 6.4-6 shows a simulation corresponding to that of Fig. 6.4-5 for $V_B = 4$ V. Several things should be noted. The first is that M1 is off when M2 is on and vice versa. The second is that V_B has caused the maximum source and sink currents to be reduced from 2.53 mA to 1.6 mA. Also note that the transfer function is nonlinear about $V_{IN} = 0$. This nonlinearity will introduce distortion in the output signal. A good compromise for this amplifier would be to go back to Class AB operation by choosing $V_B \approx 3$ V.

As we have seen in previous sections, the battery V_B is necessary for the push-pull BJT inverting amplifier. The range of values for V_B of the BJT circuit of Fig. 6.4-4*b* is

$$V_{CC} - V_{IN} - 0.7 < V_B < V_{CC} - V_{IN} \tag{6.4-17}$$

Similar considerations to those discussed for Fig. 6.4-4*a* hold for Fig. 6.4-4*b*.

Class AB and B amplifiers represent a good method of implementing the output amplifier having the ability to provide ±3 V across 1 kΩ with ±5 V power supplies. Consider now the sizing of M1 and M2 in the circuit of Fig. 6.4-4*a*. We can use Eq. 6.4-11 with $I_{D1} = I_{\overline{OUT}}$ to calculate W_1/L_1. Let us assume

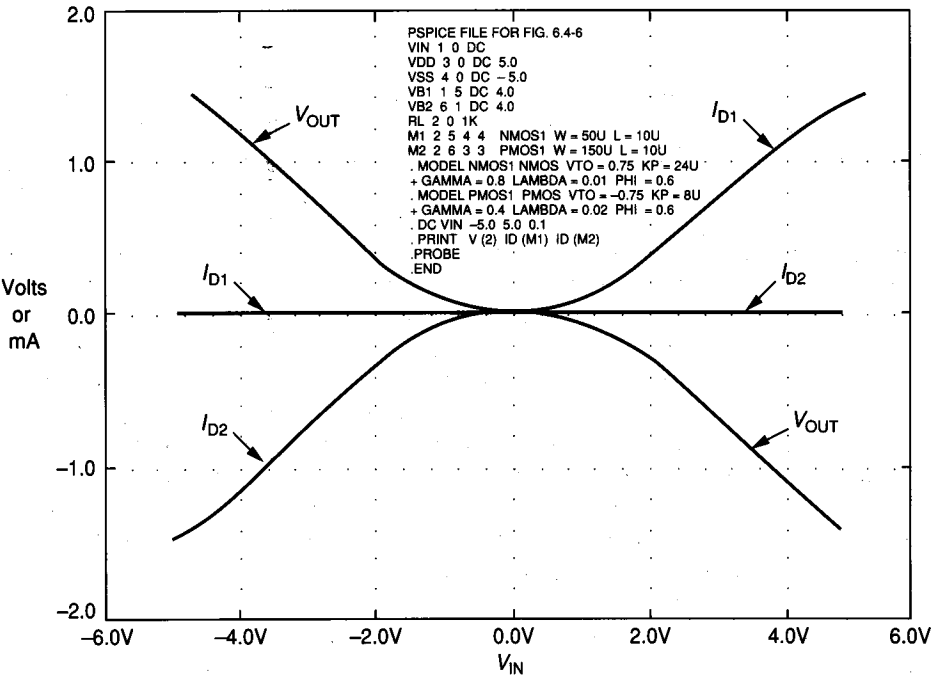


FIGURE 6.4-6
Simulation of Fig. 6.4-4*a* with $V_B = 4$ V.

that $I_{OUT}^{-} = 4$ mA to anticipate the reduction in $I_{OUT}^{-}(I_{OUT}^{+})$ that will occur when V_B is non-zero. The results give $W_1/L_1 = 180\ \mu/10\ \mu$. In order to balance the ability of the amplifier to source and sink current, $W_2/L_2 = (K_N/K_P)(W_1/L_1)$, or $W_2/L_2 = 540\ \mu/10\ \mu$. From the results shown in Figs. 6.4-5 and 6.4-6, we will choose $V_B = 3$ V. Figure 6.4-7 gives the simulated results. While this design can provide an output swing of ± 3 V across 1 kΩ, it experiences distortion above ± 2.2 V. This distortion is caused by the fact that the transistor sourcing or sinking the current is entering the ohmic region, and the current increase is linearly related to the gate voltage rather than to the square of the voltage. This can be clearly seen by the current results in Fig. 6.4-7. Consider the positive output voltage swing. The current is being sourced by M2, and at about $V_{IN} = 2$ V, which corresponds to $V_{OUT} = 2.2$ V, the rate of current increase in M2 falls off. This circuit is more suitable for ± 2 V output swings. To achieve a linear ± 3 V output voltage swing, we would have to increase the power supply to ± 6 V. It should also be noted that the voltage gain turned out to be approximately -1. Since it is not necessary for the output amplifier to have a large gain, this is not a problem; however, the voltage gain, $-g_{m1}R_L(=-g_{m2}R_L)$, depends on the value of R_L and may be less than unity.

Although the small signal output resistance of the Class B amplifier is high, it represents a good solution to the output amplifier, except for the implementation

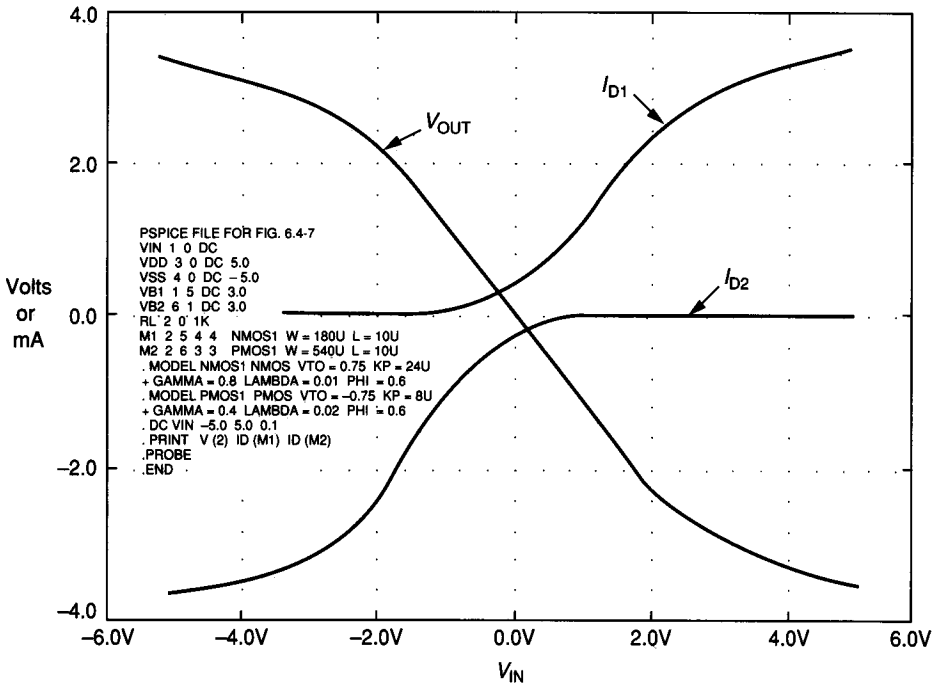


FIGURE 6.4-7
Simulation of Fig. 6.4-4*a* with $V_B = 3$ V.

of the floating battery, V_B. Figure 6.4-8 shows how the cross-coupling of four devices can allow the design of Class AB or B operation. The operation (Class AB or B) is determined by the voltages V_{GG4} and V_{GG5} (V_{BB4} and V_{BB5}), which are used to establish the bias current in the output devices M1 and M2 (Q1 and Q2). When the input voltage is taken positive, the current in M8 (Q8) increases and the current in M7 (Q7) decreases. If the operation is Class B, then M7 (Q7) turns off. As the current in M8 (Q8) increases, it is mirrored as an increasing current in M1 (Q1), which provides the sinking capability for the output current. When V_{IN} is decreased, M2 (Q2) can source output current. The output signal swing is limited to within a V_T value of V_{DD} or V_{SS} (V_{BE} of V_{CC} or V_{EE}).

The frequency response of the inverting amplifiers is generally determined by the load resistance and the shunt capacitance at the output including the load capacitance. Since $R_L(=1/G_L)$ is typically much less than r_{out} and C_L is typically much larger than the capacitances at the output node of the amplifier, the bandwidth is given as

$$\omega_{-3dB} = \frac{g_{out} + G_L}{C_{out} + C_L} \approx \frac{1}{R_L C_L} \tag{6.4-18}$$

which is primarily a function of the loading. If $C_L = 100$ pF and $R_L = 1$ kΩ, then the −3 dB bandwidth is 10 Mrps or 1.59 MHz.

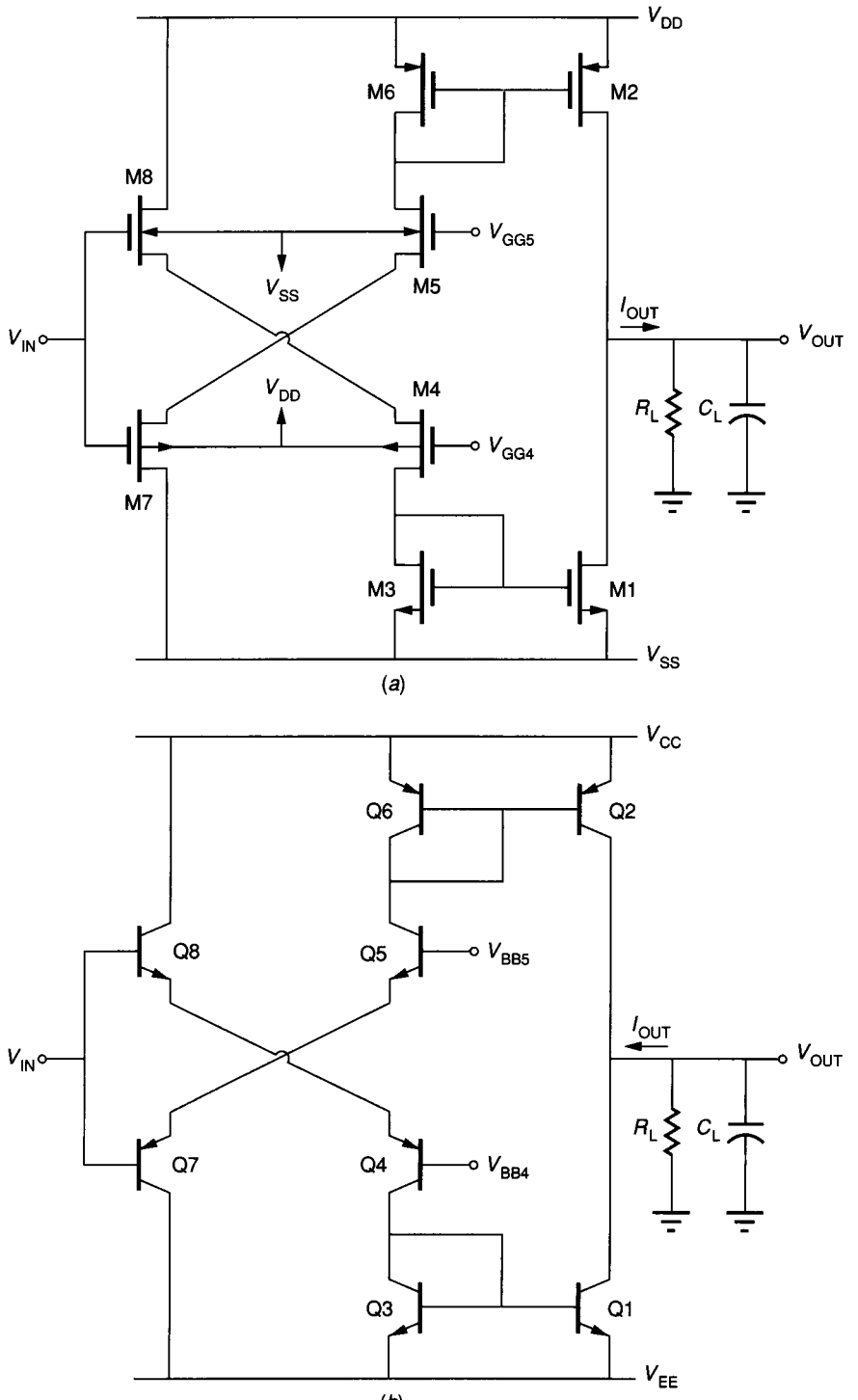


FIGURE 6.4-8
Class B or AB output amplifiers showing implementation of the floating battery for (*a*) Fig 6.4-4*a* and (*b*) Fig. 6.4-4*b*.

6.4.2 Output Amplifiers with Feedback

The second approach to the design of an output amplifier uses the principle of shunt feedback. Shunt feedback can be shown to reduce the output resistance by the following relationship

$$r'_{\text{out}} = \frac{r_{\text{out}}}{1 + \text{LG}} \tag{6.4-19}$$

where r_{out} is the output resistance without feedback and LG is the loop gain of the negative feedback loop. The simplest implementation of shunt feedback at the output is the Class A source follower and emitter follower configurations shown in Fig. 6.4-9. The follower configuration has both large current gain and low output resistance. Unfortunately, since the source is the output node, the source follower of Fig. 6.4-9*a* is dependent on the body effect, γ. The body effect causes the value of V_T to increase as the output voltage is increased. This creates a situation where the maximum output voltage of an n-channel source follower is considerably lower than $V_{DD} - V_{TO}$.

The emitter follower is also limited in its ability to obtain large positive output swing. It turns out that as the output voltage increases, more current is demanded from Q1. This emitter current is related to the base current by $I_E = (1 + \beta_F)I_B$. As the base voltage approaches V_{CC}, it becomes impossible to provide sufficient base current to sustain large positive swings. In this case, the maximum positive swing of the npn emitter follower is limited by the lack of current-sourcing capability at the peak of the positive swing. In both types of followers, the maximum negative swing is determined by the bias current sink. Usually, for appropriate size devices, the maximum negative swing is $V_{SS} + V_T$ for the MOS follower and $V_{EE} + V_{BE}$ for the BJT follower.

One advantage of the follower configuration as an output amplifier is a low small signal output resistance. This low resistance causes the ac voltage gain (and

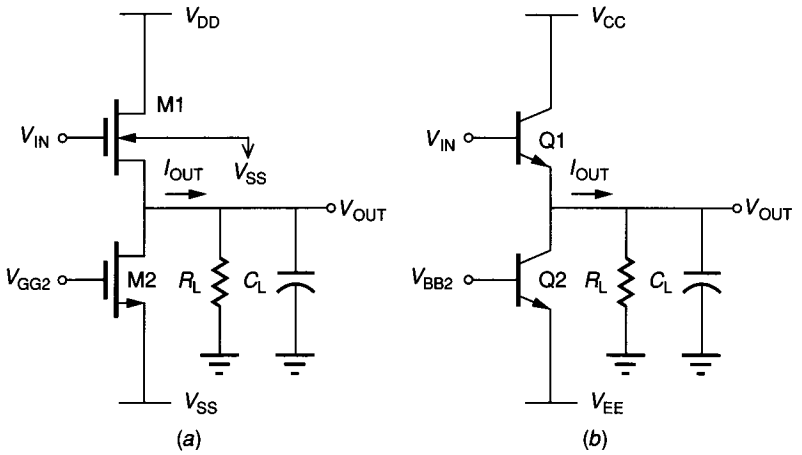


FIGURE 6.4-9
(*a*) Class A source follower, (*b*) Class A emitter follower.

frequency response) to be less dependent on R_L. The small signal model for the circuit of Fig. 6.4-9*a* is shown in Fig. 6.4-10. Figure 6.4-11 shows the small signal model for the emitter follower of Fig. 6.4-9*b*. Both of these circuits can be analyzed using Fig. 6.4-12 along with the appropriate values for the resistances and capacitances. For the source follower, we have

$$C_1 = C_{gd1} \tag{6.4-20a}$$

$$R_2 = \infty \tag{6.4-20b}$$

$$C_2 = C_{gs1} \tag{6.4-20c}$$

$$R_3 = \left[g_{m1} + g_{mb1} + g_{ds1} + g_{ds2} + G_L\right]^{-1} \approx \left[g_{m1} + G_L\right]^{-1} \tag{6.4-20d}$$

and

$$C_3 \simeq C_L \tag{6.4-20e}$$

For the emitter follower, we have

$$C_1 = C_{\mu 1} \tag{6.4-21a}$$

$$R_2 = r_{\pi 1} \tag{6.4-21b}$$

$$C_2 = C_{\pi 1} \tag{6.4-21c}$$

$$R_3 = \left[g_{m1} + g_{o1} + g_{o2} + G_L\right]^{-1} \approx \left[g_{m1} + G_L\right]^{-1} \tag{6.4-21d}$$

and

$$C_3 \simeq C_L \tag{6.4-21e}$$

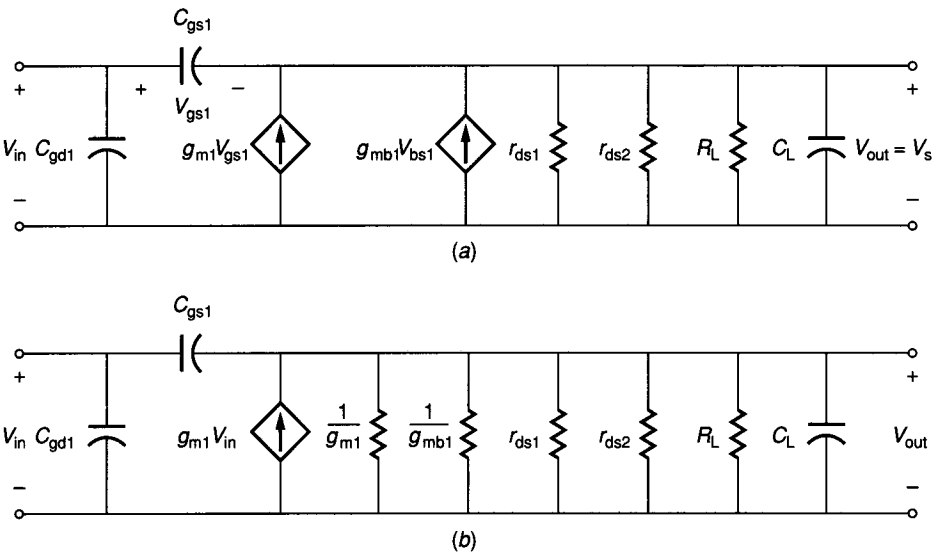


FIGURE 6.4-10
(*a*) Small signal model of Fig. 6.4-9*a*, (*b*) Simplified equivalent of (*a*).