
INDEX

- Abstraction, design, 526–528
- ac resistors, 303
 - used in differential configuration, 309, 310, 312
 - realization of, 308–317
- ac switching power, 597
- Acquisition time, 644
- Active mask, 74
 - CMOS circuit, 56
- Active region, MOSFET, 145
- Active resistors, 213, 218–221, 302–318
- Active substrates, 10
- A/D converters. *See* Analog-to-digital converters
- Advanced Low-Power Schottky TTL (ALSTTL), 588
- Algorithmic A/D converter, 656–659
- Algorithmic D/A converters, 638, 639, 640, 651
- Algorithmic layout generation
 - Bristle Blocks silicon compiler, 938–941
 - Algorithmic layout generation (*Cont.*):
 - commercial silicon compilers, 943–944
 - MacPitts silicon compiler, 941–943
- Alignment errors, 20
- Amplifiers, 378–379
 - cascode, 414–431
 - differential, 431–454
 - inverting, 379–414
 - operational, 473–499
 - output, 454–473
- Analog signal processing, 612–615
 - bandwidths of signals used in, 613, 614
 - modulators and multipliers, 735–747
 - oscillators, 747–762
 - phase-locked loops, 762–764
 - precision breakpoint circuits, 729–735
 - use in data systems, 615, 616
- Analog-to-digital converters, 642–648
 - algorithmic, 656–659
 - comparison of the performance of the various types of, 663

- Analog-to-digital converters (*Cont.*):
 converter analog multiplier, 743, 744
 dynamic characteristics of, 644, 646
 flash, 659–663
 high-performance, 664–671
 oversampled, 664, 668–671
 parallel, 659–663
 pipeline, 661, 664, 665–668
 serial, 648–651
 successive approximation, 651–659
- AND function, 533
- AND plane, PLA, 784–790
 folding, 791, 792, 793
- AND-gate logic, switch-level
 simulation using, 913
- Anisotropic etch, 38, 39
- Antimoat, NMOS circuit, 52
- Aperture uncertainty, 646
- Arithmetic logic unit (ALU), 858–860
- Autozeroing, 514–517
- Avalanche injection, 826
- Band-elimination filter, 673, 674
- Bandgap voltage reference, 366–371
- Bandpass filters, 688–692
- Bar, 3
- Barrel shifter, 857–858, 859
- Base-diffused resistor, 213, 216–217
- BellMac microprocessor
 domino CMOS and, 819
 gate matrix layout of, 799
 PLAs used in, 853
- Berkeley Oct tool set, 880
- Berkeley RISC processor, 856, 857
- Bilinear switched capacitor realization,
 317, 695, 696
- BiMos, 12, 42, 613
- Binary-weighted D/A converters,
 624–625, 626
 cascading, 625, 627
 master-slave ladder, 625, 626, 627
- Bipolar current mirror, 334
- Bipolar junction transistor. *See* BJT
- Bipolar process, 10
 design rules for, 119–120
- Bipolar process (*Cont.*):
 process parameters for, 120–122
 process steps in, 118–119, 124–126
 SPICE model parameters of, 123
- Biquad structure, 718–721, 726
 signal flow diagram of, 719
- Bird's beaking, 60
- Bistable in untuned oscillators,
 752–759
- Bit-serial processing elements, 863, 865
- BJT, 2, 10, 42, 43, 255–256
 active resistor, 305, 306, 307
 cascode amplifier, 426–431
 cascode op amp, 488
 Class A inverting voltage amplifier,
 459, 460
 combining MOS technology with,
 614
 current mirror, 336, 337, 338, 343,
 344, 345
 current reference, 360
 current sink, 319–320, 322–323,
 324, 325, 328
 current source, 363
 D/A converter techniques, 615–641
 differential amplifiers, 444–449, 450
 high-frequency, 261–262
 inverting amplifiers, 407–414
 large signal, 256–260
 modulator using a differential
 amplifier, 735–736
 noise model, 262–263
 op amp, 287, 288, 478, 479,
 481–485
 parameter definitions, 282–286
 parasitic capacitance in, 206, 207, 262
 process, 64–68
 as a switch, 291–292
 temperature dependence of, 263–264
 voltage reference, 355, 356
- BJT device models, 191–192
 dc, 192–202
 high-frequency, 205–207
 measurement of model parameters,
 208–210
 small signal, 202–205

- Bonding pads, NMOS circuit, 54
- Boolean algebra, 532
- Bootstrapping, 327
 - BJT current sink, 328, 361, 362, 363
 - CMOS current source, 363
 - JFET current source, 329, 330
 - MOS current sink, 328, 329, 361, 362, 363, 364–365
- Bottom capacitance, 582
- Bottom-up approach, 13
- Boxes, geometrical specification language, 876
- Bristle Blocks silicon compiler, 938–941
- BSIM model, 240
- Bulk-to-channel junction capacitance, 163
- Buried contacts, NMOS circuit, 52
- Butterworth filter approximation, 675, 576, 678, 679, 681, 682, 685
- Butting contacts, 83

- Calibration D/A converter, 664
- Calls, geometrical specification language, 876
- Caltech Intermediate Form. *See* CIF
- Capacitance density, 161
- Capacitive loading, 584
 - cascaded drivers, 590–593, 594
 - distributed drivers, 587–588
 - driving off-chip loads, 588–590
 - logic fanout delays, 585–586
 - typical, 588
- Capacitive noise coupling, 601–602
- Capacitors, 67–68, 210
 - monolithic, 211–212
 - ratio-matching considerations of, 81–82
- Cascade configuration
 - binary-weighted D/A converters, 625, 627
 - charge-scaling D/A converters, 631–633, 634
- Cascaded drivers, 590–593, 594

- Cascode amplifiers, 378, 414–431
 - BJT, 426–431
 - current-driven CMOS, 416–418
 - improving voltage gain of CMOS, 419–426
 - voltage-driven CMOS, 418–419
- Cascode current mirror
 - BJT, 338–339, 344
 - MOS, 348, 349
- Cascode op amp, 478, 479, 488–491
 - BJT, 488
 - CMOS, 488–491
- Channel, MOSFET, 48
- Channelless gate array, 801
- Charge pump, 826
- Charge redistribution D/A converters, 638
- Charge sharing, 818
- Charge-scaling D/A converters, 629–633, 634, 651, 653, 654
 - cascade configuration applied to, 631–633, 634
 - used in combination with voltage-scaling D/A converters, 633, 635–638
- Chebyshev filter approximation, 676, 679, 680, 685
 - switched capacitor realization of fifth-order low-pass, 714–715
- Chemical etches, 36
- Chemical vapor deposition (CVD), 35
- Chip, 3
- Chip regularity factor, 780–783
- CIF, 874, 880, 933
- Circuit extraction, 901
 - circuit extractor output, 903–907
 - interface to other programs, 908
 - simple algorithm, 902–903
- Circuit schematics, 526, 527
- Circuit simulation
 - BJT model, 255–264
 - comparison of logic simulation with, 910
 - DIODE model, 252–255
 - MOSFET model, 240–252

- Class A inverting voltage amplifier, 459, 460, 461, 470
- Class A shunt feedback, 469
- Class AB inverting voltage amplifier, 461, 462, 464, 465, 470
- Class B inverting voltage amplifier, 461, 462, 463, 464, 465, 470
- Clocked CMOS logic
 - C2MOS, 815–816
 - domino CMOS, 819–821
 - precharge-evaluate logic, 817–819
- Clocking schemes, MOS, 805–808
 - four-phase, 806
 - ideal clock signal, 806
 - multi-phase, 806
 - single-phase, 806
 - two-phase, 806–807, 808
 - typical oscilloscope display of clock, 806
- Closed loop gain, 749
- CMOS, 10, 12, 42
 - bandgap reference voltage, 370
 - cascode amplifier, 416–426
 - cascode op amp, 488–491
 - clocked logic circuits of, 815–821
 - combination of analog and digital techniques in, 613
 - current source, 363
 - depletion transistor capability, 390
 - design rules for, 73–78, 110–111
 - differential amplifier, 432–444
 - domino, 819–821
 - dynamic storage circuit, 809, 810, 811
 - fabrication process in, 545
 - gate matrix layout structure in, 797
 - input protection, 62–63
 - inverters, 544–550
 - latch-up, 61–62
 - lateral well diffusion, 60–61
 - layer definitions, 876, 877
 - logic delays, 579–582
 - multi-input logic gates, 556–558
 - NAND logic gate, 553–556, 557, 581
- CMOS (*Cont.*):
 - noise margins, 605–607
 - NOR logic gate, 551–553, 554, 556, 557, 581
 - op amp, 287, 288, 478, 480, 485–487
 - pass transistor storage circuit, 809–810
 - p-channel as pullup device, 785
 - PLA structure in, 784
 - power dissipation, 595–599
 - precharge-evaluate logic, 818
 - process parameters for, 112–113, 149, 150
 - process steps in, 55–59, 108–109, 115–117
 - processing and packaging costs, 17
 - push-pull inverter, 401, 403
 - SPICE MOSFET model parameters of, 114
 - static storage cell, 843, 844
 - switch, 300–302
 - symbolic layout language description of inverter, 881–883
 - transmission gate, 562–564
 - voltage-driven cascode amplifier, 418–419
 - width and length reduction, 59–60
- Commercial silicon compilers, 943–944
- Common mode signal, 431
- Common-mode input voltage range, 477
- Common-mode rejection ratio (CMRR), 431
- Comparators, 378, 379
 - autozeroing, 514–517
 - characteristics of, 499–502
 - high-gain, 502–507
 - propagation delay of two-stage, 507–511
 - using positive feedback, 511–514
- Complement of the moat, NMOS circuit, 52
- Complementary metal oxide semiconductor. *See* CMOS

- Computer check plots, 889–894
- Computer design rule checks, 897–898
- Conditional branching capability, 850
- Conductors, 39–40
- Constant field scaling strategy, 9
- Constant voltage scaling strategy, 9
- Constant-propagation rule, 919–920
- Contact openings, 74–78
 - NMOS circuit, 54
- Continuous-time filters, 673–674
 - bandpass filters, 688–692
 - high-pass filters, 685–688
 - low-pass filters, 674–685
 - summary of design approaches, 692
- Continuous-time RC network, 697
- Control unit, 853, 855
- Controllers. *See* Microcoded controllers
- Converter resolution, 618
- Cosputtering, 35
- Costs
 - associated with wafer processing and fabrication, 17, 18
 - development, 16
 - processing and packaging, 17, 18
 - production, 16–18
- Counters, 799
- Critical paths, 918
- Cross talk, 83
- Crystal defects, 20, 22
- Crystal preparation, IC production process, 33
- Crystal timing analyzer, 919, 922
- Current amplifiers, 333–353
- Current mirror, 333–353
 - BJT, 336, 337, 338, 344, 345
 - MOS, 345, 346, 348, 349
 - Widlar, 343, 344, 345, 351
 - Wilson, 340, 341, 350, 351
- Current reference, 354–371
 - BJT, 360
 - MOS, 360
- Current sinks, 318–332, 343
 - BJT, 319–320, 322–323, 324, 325, 328
- Current sinks (*Cont.*):
 - bootstrapped, 361, 362
 - CMOS, 363
 - comparison of, 332
 - JFET, 329
 - MOS, 323, 324, 325, 328, 329
 - regulated cascode, 330, 331
- Current sources, 318–332
 - BJT, 363
 - MOS, 363, 364–365
- Current-controlled multivibrators, 758
- Current-driven CMOS cascode amplifier, 416–418
- Current-driven inverter, 388, 389, 390
- Current-scaling D/A converters, 623–626
 - using binary-weighted components, 624–625, 626
 - using R-2R ladder, 625, 626
- Cutoff region, MOSFET, 48
- C2MOS, 815–816

- D flip-flop logic block, 802, 804
- D/A converters. *See* Digital-to-analog converters
- Data paths, 780, 853, 855
 - description of, 856–857
- dc BJT model, 192–202
 - cutoff region, 198, 199, 200
 - forward and reverse active regions of operation, 195–197, 199, 200
 - saturation region, 197–198, 199, 200
- dc diode model, 189–190
- dc MOSFET model, 144–158
- dc resistors, 303
- dc switching power, 597
- Decoders, 799
- Deep collector diffusion, BJT circuit, 66
- Defect density, 21–23
- Delta-sigma modulator, 669–671
- DeMorgan's theorem, 786, 886
- Depletion region, MOSFET, 48, 49

- Depletion-load cell, NMOS, 833, 834
- Depletion-load inverter, 534–539
 - enhancement-load inverter versus, 539–540, 578–579
 - NAND gate, 542–543
 - NOR gate, 540–542
 - and signal propagation delay, 565–569
- Deposition, IC production process, 35
- Design abstraction, 526–528
- Design automation tools, 872, 873
- Design process, 12–16
- Design rule checks, 84
 - computer, 897–898
 - design rule checker output, 898–901
 - design rule error definitions, 900
 - geometrical design rules, 894–897
- Design rules, 72–73
 - for bipolar process, 119–120
 - CMOS, 73–78, 110–111
 - geometrical, 894–897
 - NMOS, 96–97
- Design verification tools, 872, 873
- Development costs, 16
- Device modeling, 132–143
 - BJT, 191–210
 - DIODE, 187–191
 - MOS, 143–187
 - passive component, 210–221
- Device sizing
 - for clock drivers, 808
 - gate matrix layout, 797
 - Weinberger arrays, 794
- Diagonal layout structures, 876
- Die, 3
- Die attachment, 41
- Die bonding, 41
- Difference-mode signal, 431
- Differential amplifier, 378, 379, 431–432
 - BJT, 444–449, 450
 - CMOS, 432–444
 - comparison of small signal voltage gains for, 454
- Differential amplifier (*Cont.*):
 - frequency response of, 449–452
 - MOS, 436
 - noise performance of, 452–453
- Differential nonlinearity, 620, 621, 622, 644
- Differential-in single-ended output transconductance, 434
- Differential-out transconductance, 434
- Diffusion, IC production process, 39
- Diffusion capacitance, 582, 583
- Diffusion mask, NMOS circuit, 52
- Digital circuits
 - digital logic analysis of, 532–534
 - inverter-pair characteristics of, 530–532
 - logic fan-out characteristics of, 532
 - logic level standards of, 528–530
 - noise in, 599–607
 - simulation of, 908–909
- Digital logic analysis, 532–34
- Digital-to-analog converters, 615–623
 - algorithmic, 638, 639, 640, 641
 - binary-weighted, 625, 627
 - block diagram of, 618, 619
 - calibration, 664
 - charge redistribution, 638
 - charge-scaling, 629–633, 634, 651, 653, 654
 - clocked, 616, 617
 - conceptual block diagram of, 616, 617
 - conversion using the algorithmic method, 640
 - converter analog multiplier, 743, 744
 - current-scaling, 623–626
 - dynamic characteristics of, 621, 623
 - nonmonotonic, 621
 - serial, 638–642, 651
 - settling time for, 623
 - static and dynamic properties of, 618
 - sub, 664, 665
 - transfer characteristic of, 618, 619
 - use in data systems, 615, 616

- Digital-to-analog converters (*Cont.*):
 using combinations of scaling approaches, 633, 635–638
 voltage-scaling, 626–629, 633, 635–638, 651, 653, 654
- Digitizer, 875
- Dimensions of the channel, 145
- Diode bridge, 758
- Diode equation, 188
- Diode model, SPICE, 252–253
 dc, 187–190
 high-frequency, 190–191, 254–255
 large signal diode current, 253–254
 parameter definitions, 280–282
 small signal, 190
- Display media, 889–893
- Distributed drivers, 587–588
- Domino CMOS, 819–821
 cascade of, 820–821
- Drain, NMOS circuit, 55
- DRAM, 823, 835–839
 comparator circuit, 837, 838
 1M-bit, 779, 781
 one-transistor, 836
 sensing voltage versus cell capacitance, 839
 three-transistor, 835–836
- Drawn features, 73
- Dry etching, 38
- Dual inline packages (DIPs), 18
- Dual-slope serial A/D converters, 648, 649–651
- Dust particles and wafer yield, 20
- Duty cycle, 806
- Dynamic MOS storage circuits, 559
 dynamic charge storage, 808–811
 simple shift register, 811–815
- Dynamic power dissipation, 596, 597
- Dynamic random access memory.
See DRAM
- Dynamic range (DR), 182, 619
- Ebers-Moll model, 192, 193, 194, 195, 197, 199, 201, 202, 255, 260
- EDIF, 873, 880, 930
 design description of, 930–931
 mask layout view of full adder, 931–934
 net list view of full adder, 931
- EEPROM, 822, 826–827 80386.
See Intel 80386
- Electric field strengths, 9
- Electrically erasable programmable ROM. *See* EEPROM
- Electrode mask, CMOS circuit, 57
- Electromigration, 39
- Electronic Design Interchange Format.
See EDIF
- Elliptic filter approximation, 676, 677, 679, 681
- Enhancement MOSFET, 49
- Enhancement-load inverter, 534, 535, 536
 depletion-load inverters versus, 539–540, 578–579
- Epitaxy, IC production process, 41
- EPROM, 822, 825–826
- Equal area, push-pull inverter, 401
- Equal resistance, push-pull inverter, 401
- Equilibrium values, 529
- Erasable programmable ROM. *See* EPROM
- Etching, IC production process, 36–39
- Evaporation, 35
- Execution unit. *See* Data path
- Fabrication costs, 17
- Fabrication materials, characteristics of, 36–37
- Fabrication process, 11, 14–15
- False state, 528
- FAMOS technology, 825–826
- Fan-out, 532, 533, 585–586
- Fast Fourier Transform (FFT) test, 647, 648
- Faults, 20–21, 22
- Fault-tolerant technology, 21

- Feedback
 - output amplifiers with, 466–473
 - output amplifiers without, 455–465
- Feedback transistor, 840
- Feedforward reference correction techniques, 667
- FET, 2, 4, 5
- Field, NMOS circuit, 52
- Field effect transistor. *See* FET
- Filter approximation functions, 675–682
- Finite-gain structure, 683, 684, 689, 690
- Finite-state machines
 - clocking rate in, 918
 - PLA-based, 845–848, 853
- Flash A/D converter, 659–663
- Flicker noise, MOSFETs, 180, 181, 182, 183, 184
- Flip-flops, 799
- Floating current source, 318
- Floating nodes, 684, 702–703
- Folded cascode configuration, 478, 479
- Folded cascode op amp, 488–491
- Folded PLAs, 791–792
- 4 : 1 inverter sizing rule, 537, 538, 539, 541, 543, 567, 578
- Four-phase clocking scheme, 806
- Four-quadrant multipliers, 738–743
- Frequency denormalization, 683, 686
- Full scale range (FSR), 619
- Functional blocks, 526, 527

- Gain error, 620, 621, 644, 645
- Gallium arsenide, 2, 10, 28
- Gate arrays, 15, 780, 799–805
 - logic elements of, 802, 803
 - topology for typical, 800
 - wiring channels of, 800, 801
- Gate delay, 564
- Gate layout. *See* Structured gate layout
- Gate matrix layout, 793, 796–799

- Gate oxide, 9
 - CMOS circuit, 57
 - NMOS circuit, 53
- Gate–bulk capacitance, 163
- Gate-to-channel capacitance, 163
- General linear system solver, 861, 863, 864
- Geometrical circuit layout, 526, 527
- Geometrical design rules, 894–897
- Geometrical specification languages, 875–878
 - comparison of symbolic layout language with, 880
- Germanium, 2
- Gilbert cell multiplier, 736–738, 740
- Glass mask
 - CMOS circuit, 58
 - NMOS circuit, 54
- Graphical symbolic layout, 884–885
- Graphics editor, 879–880
- Guard ring placement, CMOS circuit, 61–62
- Gummel-Poon model, 255

- Hard faults, 20, 21
- Hardware design languages, 908, 929–930
 - EDIF design description, 930–931
 - EDIF mask layout view of full adder, 931–934
 - EDIF net list view of full adder, 931
 - VHDL design description, 935–938
- Hardware logic simulation, 917
- HDL. *See* Hardware design languages
- Hierarchical simulation, 917
- High-frequency BJT model, 205–207
- High-frequency diode model, 190–191
- High-pass filters, 673, 674, 685–688
- High-performance A/D converters, 664–671
- High-sampling approximation, 695
- Histogram test, 647, 648
- Hold mode, 618

- HP 9000, 853
 Hybrid integrated circuit, 3, 10, 42,
 43, 68–72
- IGFET. *See* MOSFET
- Impedance denormalization, 683, 686
- Implant mask, NMOS circuit, 52
- Improved inverting amplifier, 378
- Inert substrates, 10
- Infinite-gain realization, 684, 685,
 689, 690
- Inks, thick film circuits, 69–70
- Input common-mode signal range, 431
- Input offset current, 431
- Input offset voltage, 431
- Input pass transistor, 840
- Input protection, CMOS circuit, 62–63
- Input-referred noise source, 182, 183
- Instruction set processor specification.
See ISPS
- Integral nonlinearity, 620, 622, 644
- Integrated circuit (IC), 3
 classification by device count, 4
 size and complexity of, 4–10
- Integrated circuit layout, 873–875
 geometrical specification languages,
 875–878
 layout styles, 878–880
- Integrated circuit modem, 765–770
- Integrated circuit production process,
 32
 conductors and resistors, 39–40
 crystal preparation, 33
 deposition, 35
 diffusion, 39
 epitaxy, 41
 etching, 36–39
 masking, 33
 oxidation, 40–41
 packaging and testing, 41
 photolithographic process, 33–35
- Intel 4004, 853, 854
 Intel 8008, 853
 Intel 8080, 779
- Intel 80386, 545, 853, 855, 860
 random logic of, 779–780
- Interconnection characteristics,
 582–584
 loading, 585–586
- Interconnection delay, 564
- Interface voltage levels, 529
- Intermediate data, 858
- Inverse function, principle of the, 746
- Inversion layer, MOSFET, 48
- INVERT function, 533
- Inverter device sizing, 537–539, 550,
 567
- Inverter sizing rule, 4 :1, 537, 538,
 539, 541, 543, 578
- Inverter-pair
 characteristics of, 530–532
 signal propagation delay, 581–582
 voltage transfer characteristic of,
 530, 531, 532, 533
- Inverters, 378, 379
 basic, 529, 534–536, 546
 BJT, 407–414
 cascade of, 529, 530–532, 547–548
 CMOS, 544–550
 comparison of small signal
 performance of MOS, 406
 with fan-out, 532, 533
 general concepts of, 379–389
 improving the performance of,
 414–431
 noise in, 389, 393–394, 400
 single-channel MOS, 534–540
 voltage transfer characteristic of,
 530
- Inverting amplifiers. *See* Inverters
- Inverting continuous-time integrator,
 703–704
- Inverting switched capacitor
 integrator, stray-sensitive,
 707–708, 716, 718
- Ion etching, 38
- Ion implantation, 39
- Isotropic etch, 38, 39
- ISPS, 526, 923, 925–926

- Iteration techniques, 640
- Iterative algorithmic A/D converter, 657, 658–659
- JFET
 - current sink, 329
 - current source, 329, 330
- Junction capacitances, 163
- Kirchoff's current law, 920
- k*-ratio rule for inverters, 920
- Latch-up, CMOS circuit, 61–62
- Lateral well diffusion, CMOS circuit, 60–61
- Layout editors, 55
- Layout techniques, 78–84, 878–880
- Layout verification programs, 84
- Layout versus schematic, 901
- Least significant bit (LSB), 618
- Level-restoring inverter, 811
- Levels, geometrical specification language, 876
- Linear region, MOSFET, 145
- LISP
 - partial definition of RISC processor, 928
 - RTL simulation with, 926, 928–929
- Literal data, 858
- LOCOS, 28, 52
- Logic diagrams, 526, 527
- Logic equation symbology, 885–889
- Logic fan-out, 532, 533
 - delays, 585–586
- Logic functions
 - AND, 533
 - INVERT, 533
 - NOR, 540–542, 551–553, 554
 - OR, 533
- Logic gate arrays, 799–805
- Logic gate delay, 564
- Logic gates, 534, 799
- Logic thresholds, 528
- Logic voltage specifications, 529
- Logic-level simulation, 909–912, 915
 - comparison of circuit simulation with, 910
- Logic-level standards, 528–530
- Loop gain, 748, 749
- Low-pass filter, 673, 674–685
 - realization, 724–728
 - switched capacitor realization of fifth-order Chebyshev, 714–715
- Low-Power Schottky TTL-compatible output pad driver, 593, 594
- Lumped parasitic capacitors, 162, 164
- LVS, 901
- MacPitts silicon compiler, 941–943
- Macros, geometrical specification language, 876
- MAGIC graphics editor, 84, 879–880
- Main D/A converter, 664
- Manhattan design style, 876
- Mask aligner, 34
- Mask bias, 74
- Mask defects, 20
- Masking, IC production process, 33
- Master-slave ladder, 625, 626, 627
- Matching principle, 333–334, 345
- Material characterization, semiconductor process, 43–46
- Maximum output signal swing, 477
- Maximum output sinking current, 477
- Maximum output sourcing current, 477
- Memories. *See* Semiconductor memories
- Memory address register (MAR), 850, 851
- Memory chips, 779
- Memory refresh, 835, 836
- Metal mask, CMOS circuit, 58
- Metal migration, 39
- Metal oxide semiconductor field effect transistor. *See* MOSFET
- Metal-diffusion capacitors, 211
- Microcoded controllers, 848–853, 860–861

- Microelectronics field, 10–12
- Microinstructions, 850
- Micron, 5
- Microprocessor design, 853–855
 - arithmetic logic unit, 858–860
 - barrel shifter, 857–858
 - data path description, 856–857
 - microcoded controller, 860–861
- Microprogram-controlled microprocessor, 852
- MicroROM, 780, 850, 851, 853
 - two-level, 851
- Miller effect, 389
- MIPS series of microprocessor chips, 921
- Moat
 - CMOS circuit, 56, 57
 - NMOS circuit, 52
- Modem, 765–770
- Modulators, 735–747
 - BJT, 735–736
- Monolithic capacitors, 211
 - characteristics of, 212
- Monolithic integrated circuit, 3
- Monolithic resistors, 213–221
- Monotonicity, 644, 645
- Moore machine, 845
- MOS, 10
 - active resistor, 304
 - cascaded differential multipliers, 740–743, 744
 - clocking schemes, 805–808
 - combining BJT technology with, 614
 - current mirror, 345, 346, 348, 349, 352–353
 - current reference, 360
 - current sink, 321–322, 323, 324, 325, 328, 329
 - current source, 363, 364–365
 - D/A conversion techniques, 615–641
 - device modeling, 143–144
 - differential amplifiers, 436
 - differential resistor, 311, 313
 - dynamic storage circuits, 808–815
 - inverting amplifiers, 389–414
- MOS (*Cont.*):
 - layer definitions, 876, 877
 - modulator compatible with, 746–747
 - noise model, 393
 - processes, 46–49
 - resistors, 214, 218
 - single-channel inverters, 534–540
 - transistor as a switch, 292–294
 - voltage reference, 355, 357
 - voltage transfer function of inverters, 390
- MOSFET, 240–241
 - dc model, 144–158
 - high-frequency, 161–167, 246–250
 - level 1 large signal model, 241, 243–244
 - level 2 large signal model, 244–246
 - low-frequency, 149, 179
 - measurement of model parameters, 167–171
 - modeling noise sources in, 180–185
 - noise model, 251
 - operation in third quadrant, 177–180
 - operation of the, 46–49
 - output characteristics for, 48, 49
 - parameter definitions, 271–280
 - short channel devices, 171–173
 - simple models for digital applications, 185–187
 - small signal model, 158–160
 - subthreshold operations, 174–177
 - temperature dependence of, 251–252
 - width and length reduction in, 59–60
- MOSIS, 42, 49, 55, 100, 114
- Motorola 6800, 779, 841
- Motorola 6802, 924
- Motorola 6809, 779, 780
- Motorola 68000, ISPS description of, 925, 926, 927
- Motorola 68020, 7
- Motorola 68030, 545, 860
 - random logic of, 779–780, 782
- Motorola 88000, 943
- Multi-phase clocks, 806

- Multipliers, 735–747
 - A/D–D/A converter analog, 743, 744
 - cascaded MOS differential, 740–743, 744
 - four-quadrant, 738–743
 - Murphy model, 23

- NAND gate
 - CMOS, 553–556, 556, 557, 581
 - gate matrix layout for, 796–798
 - NMOS, 533, 542–544, 545, 575–577
 - three-input in P-E form, 817
 - timing analysis signal propagation through, 918–919
 - two-input logic block, 802, 803
- NanoRom, 851
- n-channel MOS. *See* NMOS
- Negative photoresist, 34
- Net list, 901, 903, 905
- Next-address sequencer, 850, 851
- Nitride, 40–41
- NMOS, 10, 12, 42, 49
 - depletion transistor capability, 390
 - depletion transistor as pullup device, 785
 - depletion-load cell for, 833, 834
 - design rules for, 96–97
 - dynamic storage circuit, 809, 811
 - enhancement active resistor, 304
 - inverters, 534–536
 - k*-ratio rule for inverters, 920
 - layer definitions, 876, 877
 - multi-input logic gates, 543–544
 - NAND logic circuit, 542–543, 575–577
 - noise margins, 603–605
 - NOR logic circuits, 533, 540–544, 575–577
 - pass transistor, 559–562
 - PLA structure in, 784
 - power dissipation, 595–596
 - process parameters for, 98–99, 149, 150
- NMOS (*Cont.*):
 - process steps in, 49, 51–55, 95–96, 101–107
 - reference inverter, 539
 - SPICE MOSFET model parameters of, 100
 - static storage cell, 842–843
 - transistors, 49, 143, 144, 549
 - TV timing analyzer for, 919–920
- Node current rule, 920
- Noise in digital logic circuits
 - capacitive noise coupling, 601–602
 - CMOS noise margins, 605–607
 - definition of noise margins, 602–603
 - NMOS noise margins, 603–605
 - resistive noise coupling, 599–600
- Noise in inverting amplifiers, 389, 393–394, 400
 - BJT, 410–411
 - cascode BJT, 428
 - cascode CMOS, 418–419
 - differential amplifiers, 452–453
 - push-pull, 403–404
- Noise margins, 602–603
- Noise model
 - BJT, 262–263
 - MOSFET, 180–185, 251
- Noninverting switched capacitor amplifier, 733, 734
- Noninverting switched capacitor integrator, 706–707
 - stray-insensitive, 716, 718
- Nonlinearity, 620, 621, 644, 645
- Nonmonotonicity, 620, 621, 623
- Nonoverlapping two-phase clock, 806, 807, 808
- Nonrestoring logic, 531
- Nonvolatile memory, 825
- NOR array, Weinberger, 794–795
- NOR gate
 - CMOS, 551–553, 554, 556, 557, 581
 - gate matrix layout for, 797
 - NMOS, 533, 540–544, 575–577
 - PLA, 785–786

- NOR gate (*Cont.*):
 time analysis signal propagation through, 918–919
 used in Weinberger array, 885, 886
- N*-to-1 selector circuit, 560
- Null port, 475
- Oct tool set, 880
- Offset error, 620, 621, 644, 645
- Ohmic region
 inverter, 396
 MOSFET, 48, 145, 151
 1M-bit dynamic RAM, 779, 781
- Op amps, 378, 379
 BJT, 287, 288, 478, 479, 481–485
 cascode, 488–491
 characterization of, 473, 475–480
 CMOS, 287, 288, 478, 480, 485–487
 with an output stage, 491–494
 simulation and measurement of, 494–499
- Open-loop controller, 850
- Operational amplifiers. *See* Op amps
- OR function, 533
- OR plane, PLA, 784–790
 folding, 791, 792, 793
- Oscillators, 747–762
 classification of, 748
 quadrature, 752
 RC, 748, 749, 750, 751
 relaxation, 752
 single-loop feedback system, 748, 749
 tuned, 747–751, 752
 untuned, 748, 752–760
 voltage-controlled, 748, 758
 Wien bridge, 749, 751
- Output amplifiers, 378, 379, 454
 performance comparison of, 474
 with feedback, 466–473
 without feedback, 455–465
- Output characteristics, MOSFET, 49, 201
- Oversampled A/D converters, 664, 668–671
- Oxidation, IC production process, 40–41
- Packaging costs, 17, 18
- Packaging of integrated circuits, 41
- Pad drivers, 593
- Pads, 74
- Parallel A/D converters, 659–663
- Parallel plate capacitors, 162
- Parallel switched capacitor integrator, 704
- Parallel switched capacitor realization of resistor, 314, 315, 693, 695, 696
- Parameter drifts, 20
- Parameterized layout representation, 880–883
- Parameterized module generators, 883
- Parasitic capacitance, 386
 of BJT model, 206, 207, 262
 of interconnection layers, 582
 in MOS structures, 161–167
- Parasitics, 82–83
- Particulate-related defects, 22
- Pass transistors, 558
 CMOS, 562–564
 NMOS, 559–562
 series string of, 561
 switch-level simulation using, 913
- Passband, 673
- Passive component models, 210–211
 monolithic capacitors, 211–212
 monolithic resistors, 213–221
- Passive RLC filter realization, 689, 691
- Passive RLC prototype ladder filter, 708–711
- Passive RLC prototype switched capacitor filters, 703–716
- Path-trace analysis, 922
- Pattern generation, 33
- P-E logic. *See* Precharge-evaluate logic

- Pelicle, 35
- p-glass
 - CMOS circuit, 58
 - NMOS circuit, 54
- Phase margin, 476
- Phased-locked loops (PLL), 762–764, 768, 769
 - loop and capture ranges for, 764
- Phosphosilicate glass (PSG), 40
- Photolithographic process, IC production process, 33–35
- Photoresist, 33, 34
- Physical vapor deposition, 35
- Pinch resistors, 213, 216–217
- Pipeline A/D converters, 661, 664, 665–668
- PLA(s), 780, 783
 - AND plane, 784–790
 - automatic generation, 790–791
 - combination with shift register, 812
 - comparison of Weinberger array with, 886
 - conversion of logic equations into layout topology, 885
 - double-rail input driver, 788
 - finite-state machine based on, 845–848, 853
 - folded, 791–792
 - inverting output buffer, 788
 - large, 792–793
 - NOR structure, 785–786
 - OR plane, 784–790
 - organization of, 784–790
 - programmable transistor section, 788
 - pullup cell, 788
- Plasma etching, 38
- Plastic lead chip carriers (PLCC), 18
- PMOS, 10, 12, 42, 49
 - enhancement active resistor, 304
 - transistors, 49, 143, 144, 549
- POLY I, 53, 57, 74, 75
- Poly overlap rules, 74
- POLY II, 53, 57, 74, 75
- Polygonal checks, 897
- Polyimides, 41, 58
- Polysilicon, 40, 53, 57
- Polysilicon load resistor, 833, 834
- Poly-to-moat contacts, 83
- Positive feedback, 325, 327
- Positive photoresist, 34
- Power dissipation, 593, 595
 - CMOS, 597–599
 - NMOS, 595–596
- Power spectral densities, 181
- Power supply rejection ratio (PSRR), 476, 477
- Precharge-evaluate logic, 817–819, 832
- Precision breakpoint circuits, 729–735
- Preferential etch, 38, 39
- Process control bar (PCB), 3
- Process control monitor (PCM), 3
- Process parameters, 72–73
 - bipolar, 120–122
 - CMOS, 112–113
 - dc BJT model, 192, 193
 - NMOS, 98–99
- Production costs, 16–18
- Programmable logic arrays. *See* PLAs
- Pulldown device, 534, 551, 553, 556
- Pullup device, 534, 536, 546, 551, 553, 556
- Push-pull inverter, 382, 383, 385, 386, 401, 402, 403
 - cascoded BJT, 429–431
- p-well, 74
- Quadrature oscillator, 752
- Quantization noise, 618, 620
- Quasi-static memory cells, 884–885
- Quasi-static register cells, 840–841
- Radian frequency of oscillation, 749
- Random logic
 - of Motorola 6809, 779
 - structured logic versus, 779–783
- Raster scan checks, 897–898
- Ratio logic device, 548, 567, 578

- Ratio-independent algorithmic D/A converter, 640
- Ratioless logic device, 548
- RC oscillators, 748, 749, 750, 751
- Read-only memory. *See* ROM
- Redistribution switch, 638
- Reference inverter, 539
- Refractory metals, 40
- Register storage circuits, 839–840
 - quasi-static register cells, 840–841
 - static register cell, 842–845
- Register transfer level, 526, 527
 - ISPS specification and simulation, 925–926
 - simple, 923–925
 - simulation with LISP, 926, 928–929
- Regularity factor, chip, 780–783
- Regulated cascode current mirror, 352–353
- Regulated cascode current sink, 330, 331
- Relaxation oscillator, 752
- Replication techniques, 342, 352, 640
- Resistive noise coupling, 599–600
- Resistivity, 43, 44
- Resistor realization, 693–703
- Resistors, 39–40, 68, 210
 - active, 302–318
 - monolithic, 213–221
 - ratio-matching considerations of, 79–80
 - sizing considerations of, 78–79
- Resolution, converter, 618
- Resonator structure, 684, 685, 689, 690
- Restoring logic, 531
- Reticle, 33, 34
- RISC processor, 856, 857, 883, 921
 - partial LISP definition of, 928
- RLC filter realization, 689, 691
- RLC prototype ladder filter, 708–711
- RLC prototype switched capacitor filters, 703–716
- ROM, 822, 824–825
 - EEPROM, 826–827
 - EPROM, 825–826
- RTL. *See* Register transfer level
- R-2R ladder, 625, 626
- Sah's model, 145, 146
 - comparison of Shichman-Hodges model with, 150
- Sallen and Key structure, 683, 684, 689, 690
- Sample mode, 618
- Sample-and-hold circuit, 297, 617–618, 642, 644–646, 661
 - waveforms illustrating the operation of, 617
- Saturation region
 - BJT, 197–198, 199, 200, 201
 - inverter, 396
 - MOSFET, 48, 49, 145, 146, 151
- Scaling strategies, 9
- Scribe lines, 41
- Sea-of-gates array, 15, 801–802
- Second-source requirement, logic level standards, 528
- Seeds model, 23
- Selector circuit, *N*-to-1, 560
- Self-aligned process, 53
- Self-calibrating A/D converters, 664, 665
- Semiconductor memories, 821–822
 - organization of, 822–823
- Semiconductor processes, 42–46
 - bipolar process, 64–68
 - CMOS process, 55–59
 - hybrid technology, 68–72
 - MOS process, 46–49
 - NMOS process, 49, 51–55
 - practical process considerations, 59–63
- Semi-empirical model, 240
- Sequential circuits, 805
- Sequential machine, 845
- Serial A/D converters, 648–651

- Serial D/A converters, 638–642, 651
 - conversion sequence for, 655
- Series switched capacitor realization, 695, 696
- Series-parallel switched capacitor resistor realization, 316, 317, 695–696
- Settling time, 477, 623, 645
- Sheet resistance, 43, 44, 45
 - for POLY I and II, 53
- Shichman-Hodges model, 147, 240
 - comparison of Sah's model with, 150
- Shift register(s), 811–815
 - combination with PLA, 812
 - four-bit shift-over, shift-up, 814–815
 - parallel set of linear, 812, 813
 - symbolic layout diagram for parallel set of linear, 812, 813, 814
- Short channel devices, MOSFET, 171–173
- Shunt feedback, 466, 471
- Sidewall capacitance, 164, 582
- Signal paths, 918, 920–921
- Signal propagation delays, 564–565
 - inverter-pair delay, 570–573
 - process characteristic time constant, 570
 - ratio-logic model, 565–569
 - superbuffers, 573–575
- Signal-flow rules, 919–920
- Signal-to-noise ratio (S/N), 182, 620
- Silicides, 40
- Silicon, 2, 9, 10
- Silicon compiler, 13, 15–16, 782, 878
 - Bristle Blocks, 938–941
 - commercial, 943–944
 - MacPitts, 941–943
- Silicon Controlled Rectifier (SCR), CMOS circuit, 61
- Silicon dioxide, 9, 40
- Silicon on insulator (SOI), 29
- Single-channel MOS inverters
 - basic inverter, 534–536
- Single-channel MOS inverters (*Cont.*):
 - enhancement-load versus depletion-load inverters, 539–540
 - inverter device sizing, 537–539
- Single-phase clock, 806
- Single-slope serial A/D converters, 648, 649
- Sinking inverter, 381, 382, 383, 386, 389, 391, 392, 397
 - current-source-load, 391, 396, 398, 400
 - depletion-load, 400
 - 68030. *See* Motorola 68030
 - small signal performance of the, 395–396, 399–400
- Size adjust, 73, 74
- Sizing rule. *See* Inverter sizing rule, 4 : 1
- SLAP, 885, 886–889
- Slew rate, 477
- Slice, 3
- Small outline integrated circuit (SOIC), 18
- Small signal BJT model, 202–205
- Small signal diode model, 190
- Soft faults, 20, 23
- Source, NMOS circuit, 55
- Sourcing inverter, 382, 383, 386
- SPICE simulation program, 237–240
 - BJT model, 123, 255–264, 282–286
 - CMOS model, 114
 - DIODE model, 252–255, 280–282
 - MOS realization of a current sink, 321–322
 - MOSFET model, 240–252, 271–280
 - NMOS model, 100
- Sputter etching, 38
- Sputtering, 35
- Square-law delay effect, series string of pass transistors, 561–562
- SRAM, 822, 827–835
 - address-to-column selector, 830
 - address-to-row decoder, 829–830
 - depletion-load cell for NMOS, 833, 834

SRAM (*Cont.*):

- optimum precharge voltage for data lines, 832–833
- polysilicon load resistor, 833, 834
- select line delay calculation, 831–832
- storage cell array of, 828–829
- Standard cells, 13, 780
- Standard cell synthesis, 878
- State-independent path tracing, 918, 919, 922
- States, digital circuits, 528
- Static analysis, 919
- Static power dissipation, 595, 597
- Static random access memory. *See* SRAM
- Static register cell, 842–845
 - cross-coupled NOR latch, 842
- Sticks, 884, 885
- Stopband, 673
- Stray insensitivity, 706
 - inverting switched capacitor integrator, 707–708, 716, 718
 - noninverting integrators, 716, 718
 - SC filters, 211
- Strong inversion, 174–177
- Structured gate layout, 793
 - gate matrix layout, 793, 796–799
 - Weinberger arrays, 793, 794–796
- Structured logic, random logic versus, 779–783
- Sub-D/A converter, 664, 665
- Substrate, 3, 10
- Substrate transistors, 67
- Subthreshold operation, MOSFET, 174–177
- Successive approximation A/D converters, 651–659
- Successive approximation register (SAR), 652, 653
- Superbuffers, 573–575
- Switch(es), 289–302
 - application of an n-channel MOS transistor as a, 295, 296
 - bipolar transistor as a, 291–292

Switch(es), (*Cont.*):

- CMOS, 300–302
- feedthrough, 298–299
- graphical characterization of, 290–291
- illustration of the on state of, 294, 296, 297
- leakage current, 297–298
- model of ideal voltage-controlled, 289–290
- MOS transistor as a, 292–294
 - use of dummy transistor to cancel clock feedthrough, 299–300
- Switched capacitor (SC), 314
- Switched capacitor amplifier, noninverting, 733, 734
- Switched capacitor filters, 692–693
 - design of, 673
 - passive RLC prototype, 703–716
 - resistor realization, 693–703
 - total capacitance required, 715–716
 - z-domain synthesis techniques, 716–728
- Switched capacitor integrators, normalized frequency versus, 706
- Switched capacitor realization of resistors, 314–318
- Switching threshold voltage, 531
- Switch-level simulation, 913–917
- Symbolic circuit representation
 - graphical symbolic layout, 884–885
 - logic equation symbology, 885–889
 - parameterized layout representation, 880–883
 - parameterized module generation, 883
- Symbolic layout language (SLL), 880–883
 - comparison of geometrical specification language with, 880
- Symmetric output drive, 548
- Synchronous modulators, 738
- Systolic arrays
 - bit-serial processing elements, 863, 865

- Systolic arrays (*Cont.*):
 - general linear system solver, 861, 863, 864
- Systolic matrix multiplication, 861, 862
- Temperature coefficient of capacitance (TCC), 45
- Temperature coefficient of differential nonlinearity, 646
- Temperature coefficient of gain, 646
- Temperature coefficient of linearity, 646
- Temperature coefficient of resistance (TCR), 45
- Temperature dependence
 - BJT, 263–264
 - MOS, 357–358
 - MOSFET, 251–252
- Test cell, 3
- Test lead, 3
- Test plug, 3, 41
- Testing of integrated circuits, 41
- Texas Instruments, 779, 781
 - chip size of 1M DRAM, 7
- Thermal noise
 - inverter, 393–394
 - MOSFETs, 180–181, 183, 184
- Thick film process, 10, 69–71, 127–129
- Thin film process, 10, 71–72, 130–131
- Threshold voltage, MOSFET, 48
- Time-interleaving, 659, 660, 661
- Timing analysis
 - methodology of, 918–919
 - tools used in, 919–923
- Top-down approach, 13
- Tow-Thomas circuit, 684, 685, 689, 690, 752
- Transfer operation, RTL, 923
- Transfer switch, 734
- Transition region
 - low-pass filters, 674
 - sinking inverter, 382
- Transmission gates, 301, 558
 - CMOS transmission gate, 562–564
 - NMOS pass transistor, 559–562
- Trench isolation, 68
- True state, 528
- Tuned oscillators, 747–751, 752
- TV circuit-level timing analysis
 - program, 919, 921
- Two-phase clocking schemes, 806–807
 - nonoverlapping, 806, 807, 808
- Unity-gain bandwidth, 476
- Untuned oscillators, 748
 - bistable in, 752–760
- Varactor diode, 190
- Vari-cap diode, 190
- Verification proofs, 917
- VHDL, 873, 930
 - design description of, 935–938
- Via, 74
- Via mask, CMOS, 58
- Volatile memory, 825
- Voltage dependence of resistors and capacitors, 46
- Voltage reference, 354–371, 646
 - BJT, 355, 356
 - MOS, 355, 356, 357
- Voltage specifications, logic, 529
- Voltage transfer characteristic, 729–735
- Voltage-controlled oscillator (VCO), 748, 758, 759, 761, 762
- Voltage-dependent junction
 - capacitances, 211
 - resistors and capacitors, 46
- Voltage-driven CMOS cascode
 - amplifier, 418–419
- Voltage-driven inverter, 388, 389, 396
- Voltage-scaling D/A converters, 626–629, 651, 653, 654
 - 3-bit, 627, 628
 - used in combination with charge-scaling approaches, 633, 635–638

- Wafer, 3
- Wafer processing costs, 17
- Wafer scale integration (WSI), 4, 23
- Wafer yield, 19
- Waveshaping circuits, 729–735
- Weak inversion, 152, 174–177, 369, 370, 371
- Weinberger arrays, 793, 794–796
 - comparison of PLA with, 886
 - generating geometrical layouts from logic equations using, 885–886, 887
- Wet etches, 36
- White noise, MOSFETs, 180, 181, 182
- Widlar bandgap voltage reference, 367, 368
- Widlar current mirror, 343, 344, 345, 351, 367
- Wien bridge oscillator, 749, 750, 751
- Wilson current mirror, 340, 341, 350, 351
- Yield, 19–27
 - effect of defects on, 21
- Yorktown Simulation Engine (YSE), 917
- Z-domain synthesis techniques, 716–728
- Zener diodes, 188–189