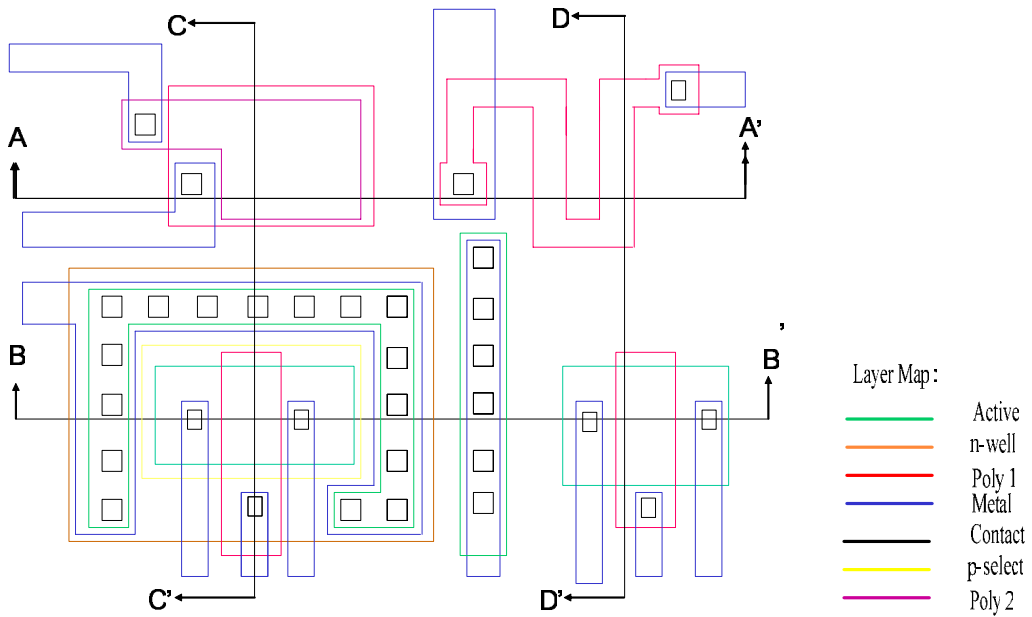


EE 434  
Homework 4  
Fall 2006

Problem 1 Sketch a cross-sectional view along the BB' cross-section for the CMOS layout shown below. Assume a basic CMOS process in which the n-select mask is generated from the compliment of the p-select mask.

Problem 2 Repeat Problem 1 along the DD' cross-section



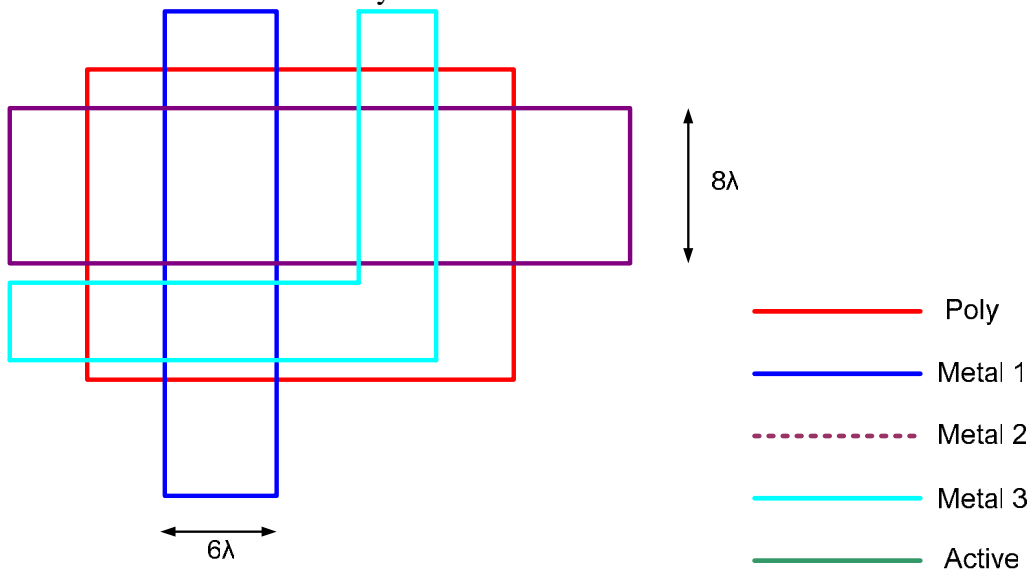
Problem 3 Exercise 3.1 W&H

Problem 4 Exercise 3.2 W&H

Problem 5 Exercise 3.6 W&H

Problem 6 Exercise 3.7 W&H

Problem 7 Four non-contacting regions are shown. Identify the parasitic capacitances and their size if this is fabricated in the 0.5u CMOS process. Use the process electrical parameters given on the MOSIS WEB site for the T55W process run. Don't forget that there is substrate below all layers.



Problem 8 Repeat Problem 7 if active is included as shown.

