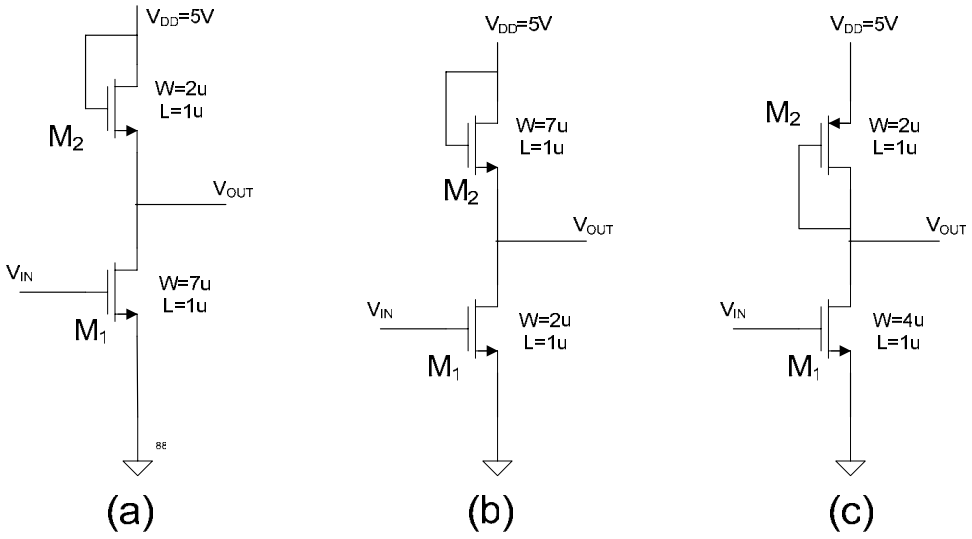
EE 434
Assignment 7
Fall 2005

Problem 1 Give all of the two-input Boolean functions and identify which of those are useful.

Problem 2 The circuits shown have been proposed as digtal inverters. Determine which will behave as digital inverters and which will not. If the circuit performs as a digital inverter, determine V_H and V_L. Assume the devices are all in the process with $\mu C_{OX}=100uA/V^2$, $V_T=1V$, $\gamma=0$ and $\lambda=0$.



Problem 3 Extra Credit Only

What is the maximum value of W_1 in the circuit (a) of the previous problem that can be used if this circuit is to perform as a digital inverter?

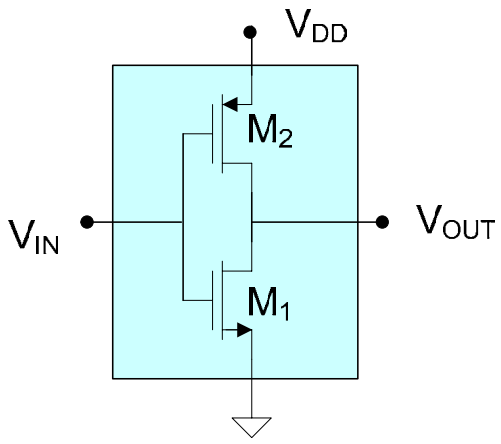
Problem 4 A Boolean System is supposed to have an output F that is high when the Boolean inputs A and B are high or when the inputs Cand D are high and E is low or when the input A is low and the input E is high.

a) Give a behavioral description of this system in terms of the input variables A,B,C,D,E and F.
b) Write Verilog code describing this system at the behavioral level
c) Give a gate-level structural descripton of this system if the only gates that are available are NOR gates with any number of inputs.
d) Write Verilog code describing this system at the gate level
e) Give a transistor-level physical description of this system. You may use any logic style you are familiar with. You need not size the devices.

Problem 5 Determine the trip-point, V_H, and V_L of the inverter under the following scenarios and comment on how device dimensions affect these key points.

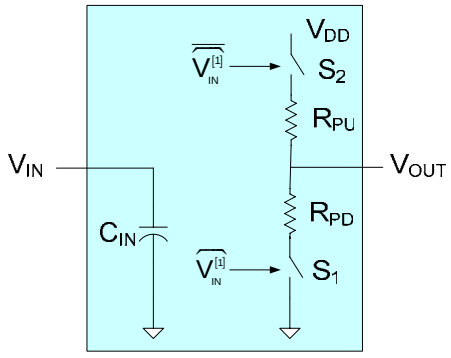
a) W_1=0.6u, W_2=1.8u. L_1=0.6u, L_2=0.6u
b) W_1=3u, W_2=9u. L_1=3u, L_2=3u
c) W_1=0.6u, W_2=0.6u. L_1=0.6u, L_2=0.6u
d) W_1=0.6u, W_2=0.6u. L_1=0.6u, L_2=6u

Assume $\mu_n C_{OX}$=100uA/V^2, V_{Tn}=1V, V_{Tp}=-1V, μ_n/μ_p=3, γ=0 and λ=0.



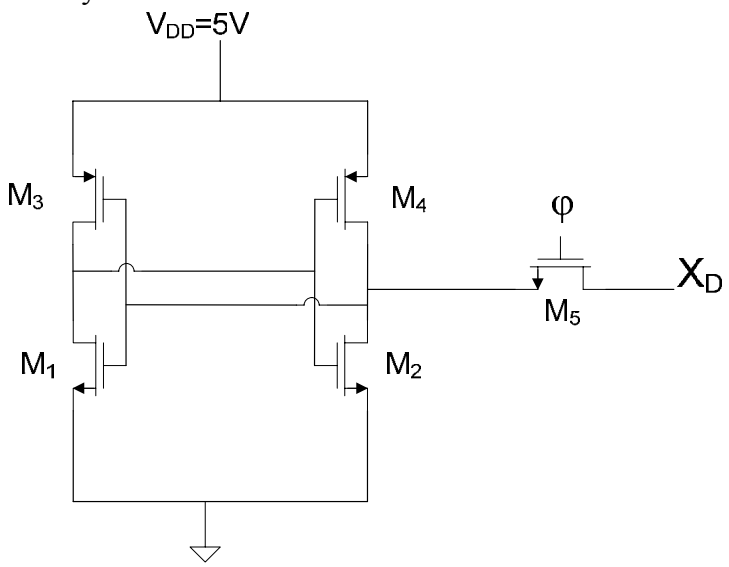
Problem 6 A switch-level model of an inverter is shown where the resistors R_{PU} and R_{PD} are the "Pull-up" and "Pull-down" resistors, C_{IN} is the input capacitance to the inverter, and where the notation $\widehat{X^{[m]}}$ indicates a quantized value of the quantity X, quantized to the m-bit level. Thus $\widehat{V_{IN}^{[1]}}$ is a 1-bit (i.e. two-level) quantization of V_{IN} and is thus a Boolean variable. Assume the quantization level if V_{TRIP}.

a) Find the switch-level model of the inverters described in Problem 5 if C_{OX}=2fF/μ^2
b) Determine t_{HL} and t_{LH} for the inverters in Problem 5 the inverter drives an identical structure
c) Comment on how the device sizing affects the propagation delay of an inverter.



Problem 7 Extra Credit Only

A 5-transistor memory cell is loaded with X_D when φ is high and holds the value of X_D when φ is low. Assume M_1, M_2, M_3 and M_4 all have W=1μ and L=2μ and the length of M_5 is 1μ. If a high Boolean signal is 5V and a low Boolean signal is 0V, determine the minimum value of W_5 needed to guarantee that the value of X_D can be written into the memory cell.



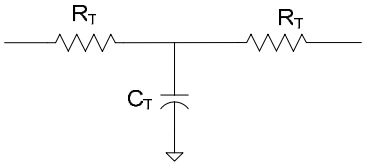
Problem 8

A static CMOS inverter with Wn=Wp=2u and Ln=Lp=1u designed in a 0.5u CMOS process is driving a 1pF load. Determine t_{HL} and t_{LH} for the output of this inverter.

Problem 9

A poly interconnect that is 2u wide and 50u long is used to connect a low impedance signal to a 500fF load. Assume the capacitance density of this poly layer is .5fF/$u^2$and the sheet resistance of the poly is 20 ohms/square.

a) If this interconnect is modeled by the series connection of 4 T-connected segments shown, determine the value of the resistors R_T and the capacitor C_T in each of these segments.



b) Determine the Elmore delay associated with this interconnect model

c) Compare the Elmore delay with that obtained with a Spice simulation

Problem 10 Problem 4.1 of Text (Assume $\mu_n/\mu_p=3$ and that the reference inverter has Wp=3Wn and Lp=Ln).

Problem 11 Problem 4.8 of Text
Problem 12 Problem 4.9 of Text