Laboratory 3: Layout and LVS (layout vs. Schematic)

Objective: The objective of this experiment is to learn to draw layout of a circuit. The concept of creating layouts that conform to a set of *design rules* is introduced. The produced layout will be checked against the schematic to ensure full equivalency.

Layout view

In our design environment, a layout view gives a representation of how the semiconductor circuit will look like once fabricated. Once the layout is complete, is found to be free of any design rules violations, and is electrically equivalent to the schematic, it can be sent to the foundry for fabrication.

We will create the layout of the inverter we created in the previous lab. Create a layout view of the **inverter** cell in **lablib** library. The virtuoso layout editor window will open. You will notice that a second window called *Layer Selection Window* was opened as well. It lists all the available layers in the process that is used, along with their corresponding color code. Since we attached the library to AMI06, our lambda is 0.3u.

In the layout editor window, notice how the mouse snaps to the closest coordinate unit. To check your grid settings, go to **Options→Display→Grid Controls**. It is suggested that the X & Y snap spacing be at 0.15. And the minor and major spacing be at 1 and 5 respectively. Based on the lecture notes, draw a layout of your inverter. Make sure you draw the transistorsizes according to the sizes you have in the schematic.

The shapes we are able to draw are all rectangular. For example, to draw a rectangular piece of *poly* that is $7\mu \times 0.6\mu$, first go to the LSW and select the *poly* layer (the vermillion one), then go to the layout window and select **Create→Rectangle**. Go to the middle of the window and left-click once. Now move the mouse all the while watching for the dX and dY on the bar above the menu: you should stop moving the mouse when you hit dX: ±7.00 and dY: ±0.60 or vice-versa, then left-click again to end the drawing. You can use the ruler to check your dimensions. If the screen becomes cluttered with rulers, go to **Window→Clear All Rulers**. Make sure you experiment with the buttons to the left as well as the menu to get comfortable moving, copying, stretching, cropping or rotating a rectangle; the options are endless.

To create a pin, go to **Create→Pin**. Make sure the pins are consistent with the schematic: names and I/O types. Check the **Display Pin Name** box. When you know where the pin goes, click on the **Pin Type** box. For example, a pin that goes on metal1 should have a pin type metal1. The pins do not go into fabrication: they are merely used to ensure that your layout matches your schematic design with respect to pin names.

Part 2 Checking for errors

When you think you have a finished layout, go to **Verify→DRC→OK**. What we are essentially doing is verifying our layout for design rule errors. For example, if the smallest width of a poly strip is 0.6um, and we drew it to be 0.3um, then the Design Rule Check will print out an error. The check will guarantee that the fabrication of the integrated circuit is at least feasible.

If your layout is flawless, you should see the following message in the CIW:
`Total errors found: 0`

If you'd like to debug your errors, you can go to **Verify→Markers→Explain**, and click on any of the white error markers on your layout. It is easy to guess what the white markers mean: for example, if you see that a rectangle has a white cross inside it, it means it is not probably shaped. If you see white markings in the area between two rectangles, it means that they are too close…etc

Part 1.2: Layout vs. Schematic (LVS) comparison:

When we are finished with the layout, we need to check it for consistence with the schematic it is supposed to represent. The comparison makes sure we have the exact number of devices, and also that they have the same I/O pins and device sizes.
There is one more step we need to perform before we can do the LVS, and that is the *extraction* of the layout. We will essentially go from layers of semiconductor material (layout) to an identification of the various components, their sizes and pins (extracted.) A more advanced extracted will also include the parasitic capacitance between any two layers as well as the resistance of any layer path. Go to **Verify→Extract→OK**. As with the DRC, we have the extraction rules stored in the *divaEXT.rul* file.

Usually the extraction step doesn't introduce any errors. You will notice that a new cell-view appeared in your Library Manager and that's the "extracted" view. You can open it and see how it looks. Press **Shift-F** for a more detailed view that shows where Diva has detected a capacitor, a resistor or a transistor.

In either the layout of the extracted view of your design, go to **Verify→LVS**. Make sure you are comparing the right schematic and extracted views by hitting **Browse**. Hit **Run** when you are ready to run the LVS. If you have everything checked and saved before you run the LVS, you will get the message:

`Job 'directory' that was started at 'time' has succeeded.`

This only means that the LVS ran properly, not that your design passed the test. If you don't save your schematic before running the LVS you will get a fail message, so make sure you always save your work. In order to know whether your design passes the LVS, go back to the LVS window and hit **Output**. Go over the file "si.out" that opens and study its different sections. This is the only text you will have for debugging. If your layout is acceptable and if you scroll down a bit you should see:

`The net-lists match.`

If they don't match, you need to alter your layout and re-do all the extraction and LVS steps again until they match.

How to <u>locate</u> a net on the extracted view:
Sometimes it is very hard to find a net in your extracted view. Probing the design makes finding nets a much easier job. Choose **Verify/ Probe**. In the Probing form, click on **Add Net**. Then go to

the CIW, and type “X” (X is the name of the net that you wish to locate) at the command prompt, including the double quotes, and press Enter. Back to the extracted cell-view window, you should see a mask layer being highlighted, which has the given net name. You can also left-click on a net and look at the CIW to know its name. The latter method is faster and more suitable for smaller designs, while the first one is better for larger designs.

♦ This document is available at http://class.ece.iastate.edu/ee434/labs/lab3.pdf