Lab 4: From Boolean Function to Silicon

Pre-lab (To be completed before start of week 2 of the lab)

1) For your inverter and the other gate you chose (2 or 3-input NAND or NOR), attach the following
   a. Transistor-level schematics
   b. Test bench (test setup) to verify the operation of the gates
   c. Simulation results demonstrating correct gate operation
   d. Layout without any DRC violations
   e. LVS report showing that net-lists matched

2) Attach the hand-drawn gate level implementation of the assigned Boolean function that uses only the allowed gates (2 or 3-input NAND or NOR, Inverter).

3) Attach proof that demonstrates the correctness of the gate level Boolean function of step 2. This can be done by hand by applying all 16 possible inputs and building a truth table for your circuit. Alternatively, you can use any other tool of your choice to build the truth table. Compare the truth table of your implementation with the truth table of the function assigned to you.

4) At the start of the lab, you will enter the top level schematic in Cadence and then test it by applying A, B, C, and D waveforms. What would those input stimuli be in order to exercise all combinations of the inputs? Draw a simple figure that shows the pulse width, period. etc., of each input waveform. What output waveform do you expect?

5) Write the names of the colleagues you are collaborating with and the gates you are exchanging:

Name of the colleague	Gate you will provide	Gate you will obtain