Performing post-layout simulations

Parasitic capacitances and resistances in the layout can strongly affect the performance of a design. To evaluate the effects of parasitics and to gain a higher degree of confidence that a layout will result in a chip that meets the specifications, it is important to run post-layout simulations. The performance of a circuit predicted with parasitics accounted for will always be worse, although closer to reality, than a schematic that does not include estimated parasitics.

The procedure of running post-layout simulations is very similar to simulating a Schematic. The steps to prepare a design for post-layout simulations are listed below.

1. Extracting the parasitics

To include the actual parasitic capacitances of a layout, we need to extract them. This is achieved during the extraction phase of verification. In our design flow so far, we extracted a layout using the default options and then performed LVS. To extract a layout with parasitic capacitors (our design environment currently does not support extracting parasitic resistors), click on **Verify**→**Extract** in the layout window (after correcting *all* DRC violations). In the window that comes up, click on the "Switches" button. Another form, shown below, will pop-up with a few optional switches. The explanation of all the switches can be found at

http://www.cadence.ncsu.edu/doc/cdsmgr/diva_verification.html#extraction.

S EXTRACTOR		×	X Set Switches(Ctrl+mouse for multiple)	×
OK Cancel Defaul	ts Apply	Help	OK Cancel	Help
Extract Method Join Nets With Same Nam Switch Names Run-Specific Command Ei	√ macro cell √ full hier √ incremental hier Echo Commands I Set Switches		Extract_parasitic_caps Keep_labels_in_extracted_view Layer_convert_[np]active_to_active Layer_convert_active_to_[np]active Layer_create_nselect_around_nactive Layer_create_pselect_around_pactive	
Inclusion Limit View Names Extrac	ed extracted Excell excell		Use_old_moscap_extraction	
Rules File	divaEXT. rulį			
Rules Library	U_TechLib_ami06			
	local remote Machine	_		

For our purposes, select the "Extract_parasitic_caps" switch and click OK on both forms. You can open the extracted view and look at the various parasitic capacitors in your layout.

2. Creating analog_extracted view

To simulate the complete design, we will simulate a cell view called the analog_extracted view. Once your design has passed LVS, click on the "Build Analog" button at the bottom right of the LVS form, as shown in the figure below.

			Help 3	
Run Directory	LVŠ		Browse	
Create Netlist	schematic	extracted		
Library	lablib	lablib		
Cell	OpampFromTA	OpampFromTA4XL		
View	schematic	extracted		
	Browse Sel by Cursor	Browse	Sel by Cursor	
Rules File	divaLVS.rulį		Browse	
Rules Library	📕 NCSU_TechLib_ami06			
VS Options	Rewiring	Device Fi	xing	
	Create Cross Reference	e 📕 Terminals	Oreste	
orrespondenc	e File lvs_corr_file		Greate	
Correspondence Switch Names	Filelvs_corr_file			
Correspondence Switch Names Priority (File _ lvs_corr_file			

A new cell view called analog_extracted will be created for the cell.

3. Simulating the analog_extracted view

Open the schematic window that contains the top level symbol of your design and the test stimuli. Start the ADE as if you wanted to test the functionality of your complete design. Once ADE has started, click on **Setup** \rightarrow **Environment...** In the form, add analog_extracted as the first entry in the Switch View list. Run simulations as before and the simulator will use analog_extracted view for every block, if available, before resorting to the Schematic view. Consequently, the simulation results will include the effects of the parasitic capacitors we extracted earlier. To verify that you are simulating the circuit with parasitics, view the netlist from ADE and see if you can spot the parasitic capacitors in the netlist.

Your chip will be sent for fabrication only if you provide proof of functionality from post-layout simulations.