EE 434
Lecture 10

Resistors and Capacitors

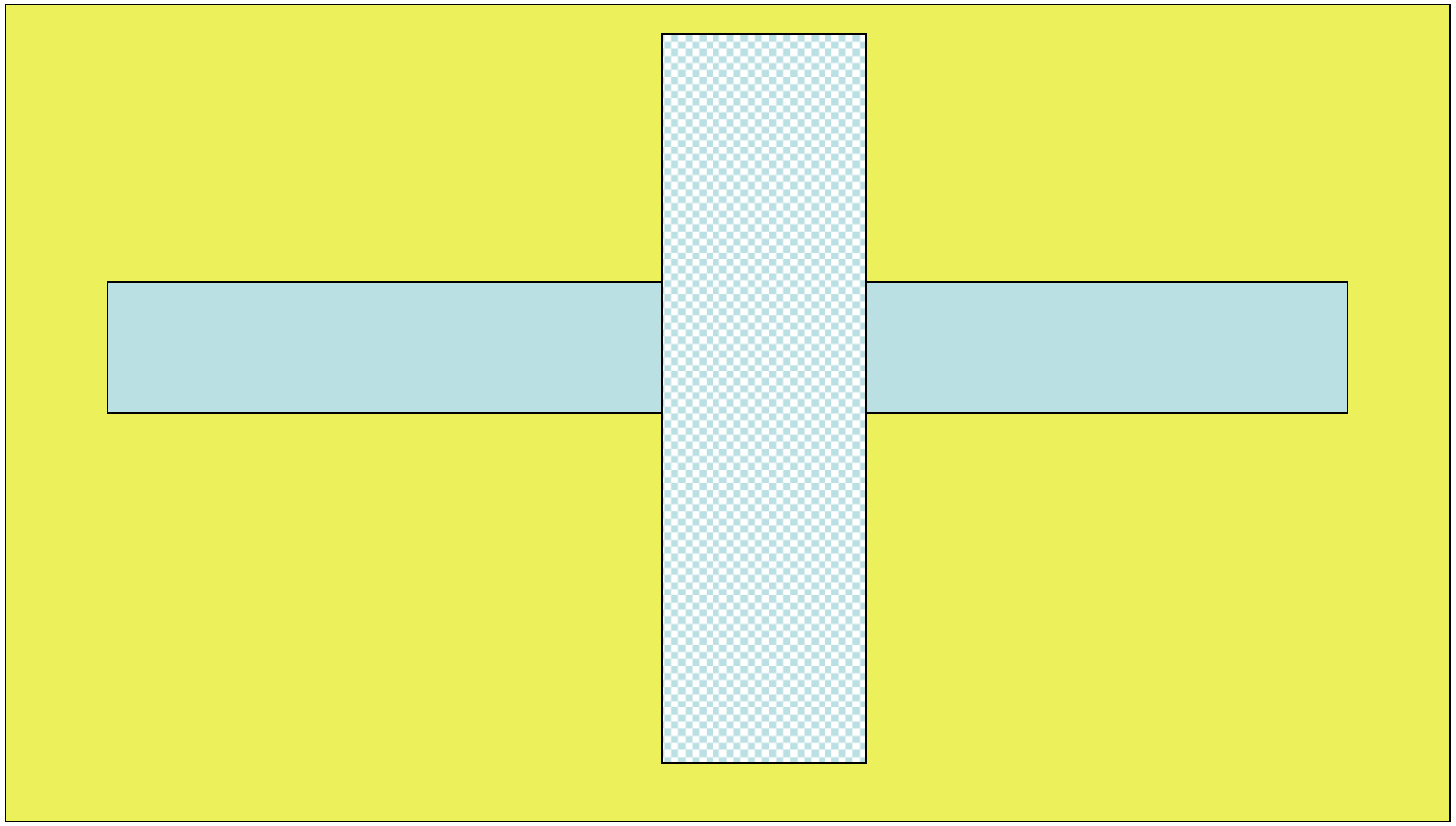
Planarization

Backend Processing Steps

Basic Semiconductor Processes

Devices in Semiconductor Processes

Capacitance in Interconnects



$C=C_DA$

C_D is the capacitance density and A is the area of the overlap

Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quility layers in subsequent processing steps
  - Mechanically planarized

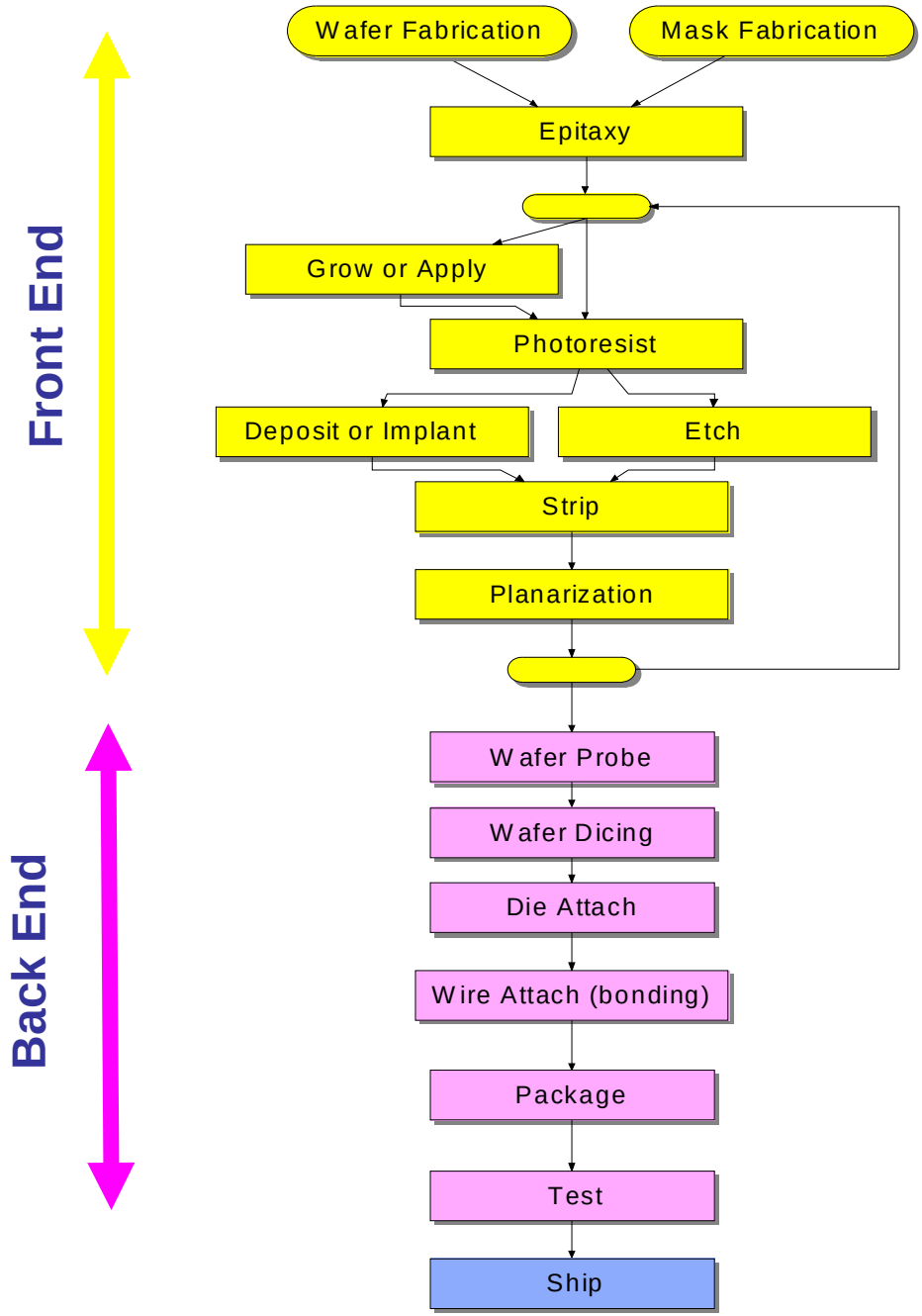
Basic Devices

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (in some processes)
    - npn
    - pnp
- Niche Devices
  - Photodetectors
  - MESFET
  - Schottky Diode (not Shockley)
  - MEM Devices
  - ….

Primary Consideration in This Course

Limited Consideration in This Course

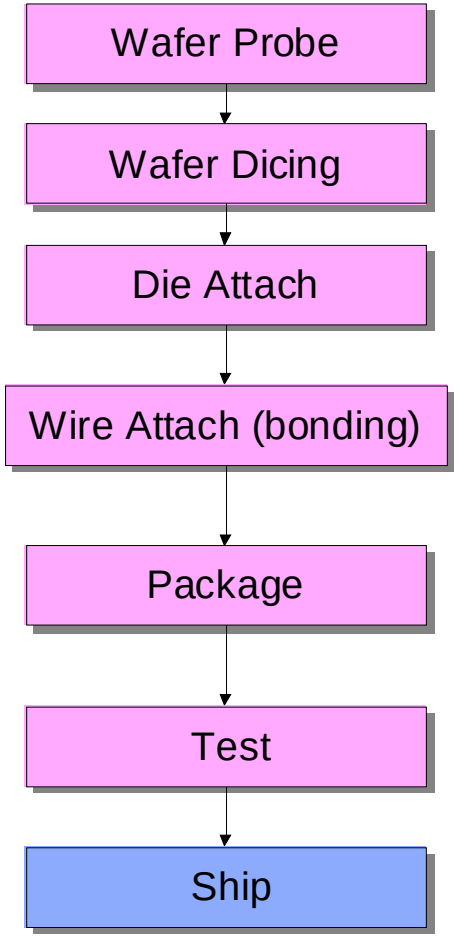
Generic Process Flow



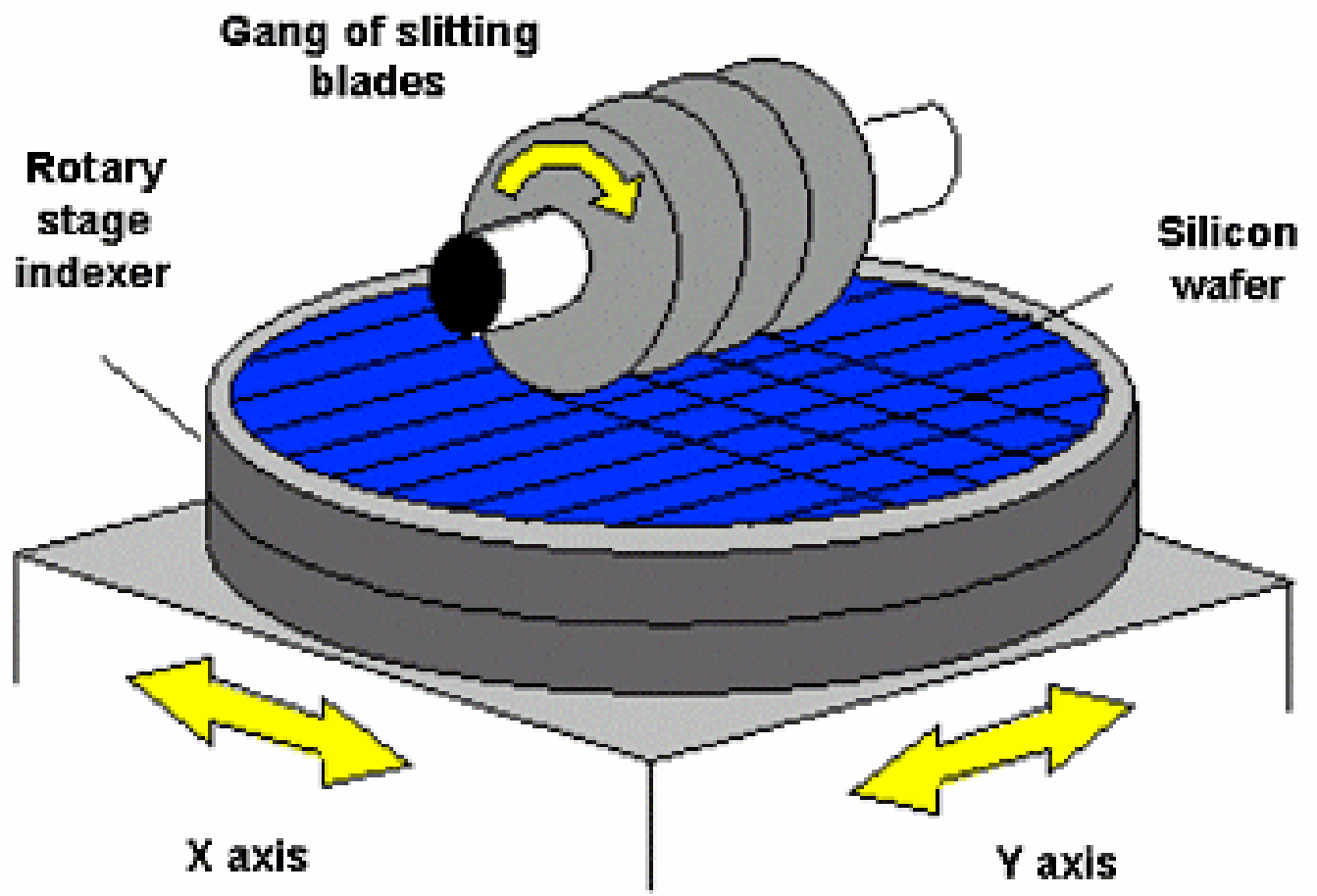
Front-End Process Flow

- Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary

Back-End Process Flow



Wafer Dicing



www.renishaw.com

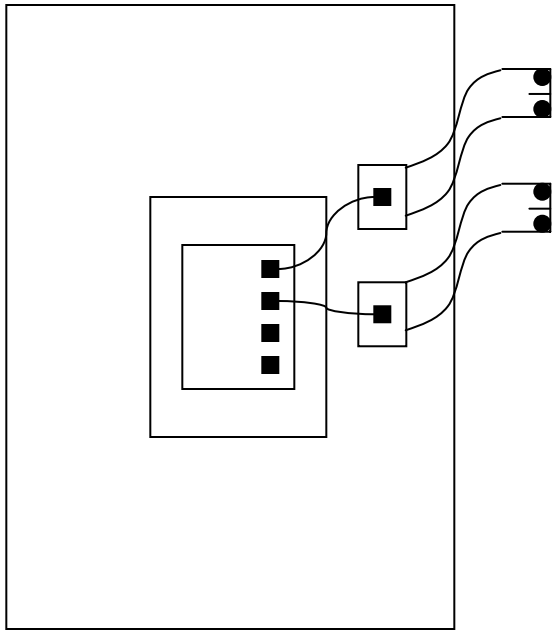
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy

Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding

Wire Bonding



Wire – gold or aluminum
25 μ in diameter

Wire Bonding

Excellent Annimation showing process at :

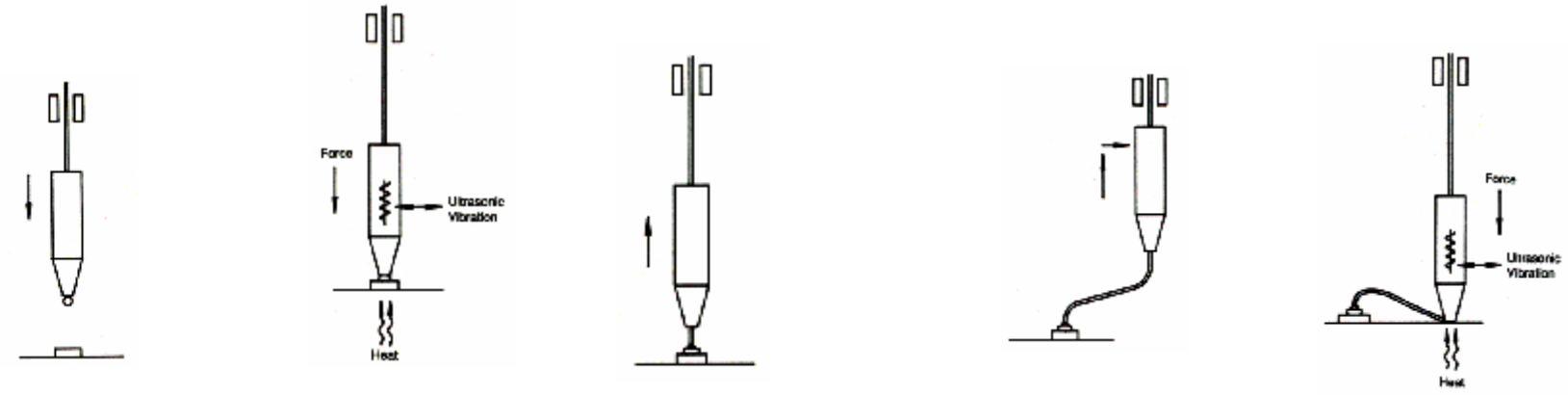
http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf

Wire Bonding

Ball Bond

Wedge Bond

Ball Bonding Steps



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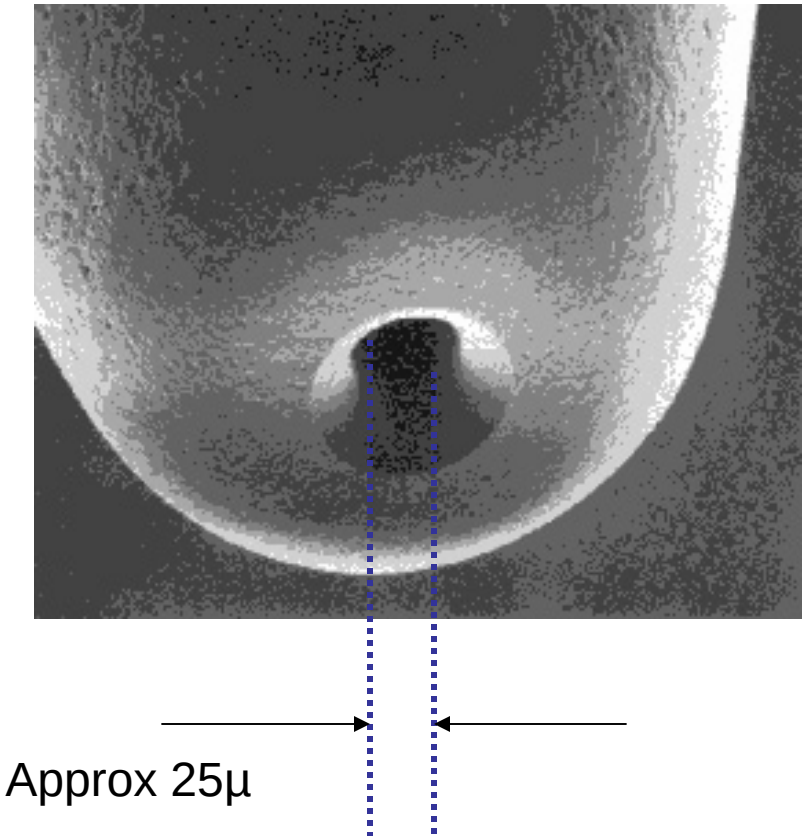
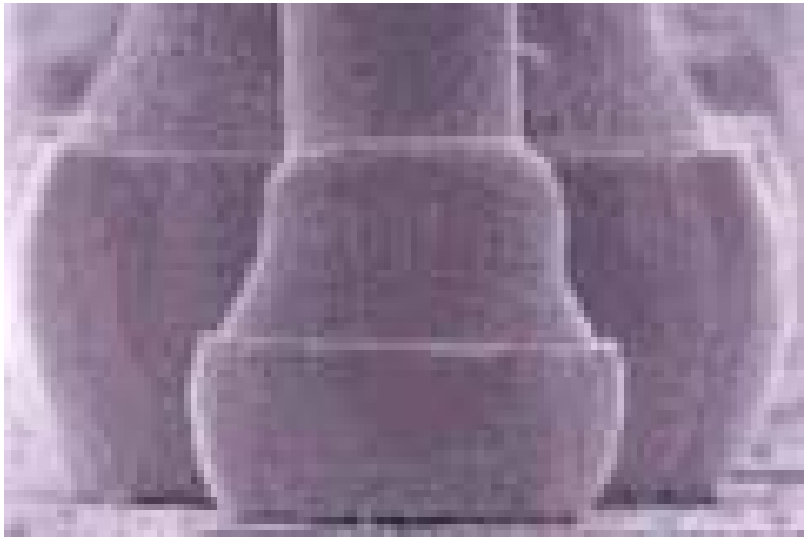
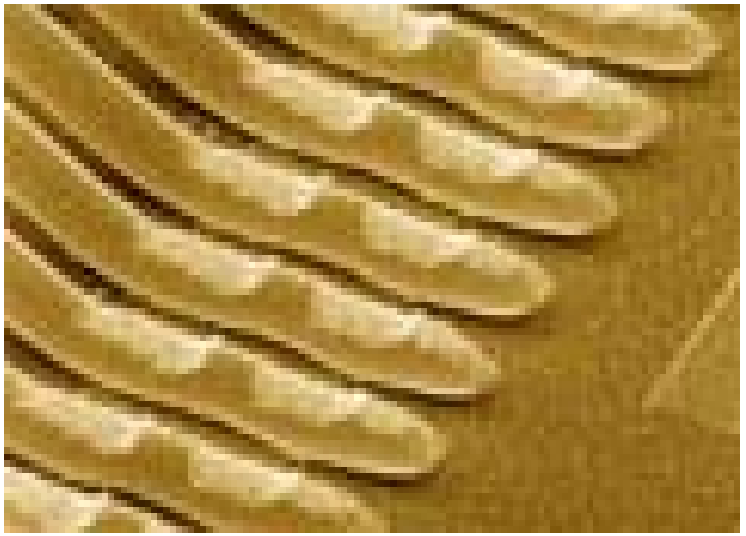
Ball Bonding Tip



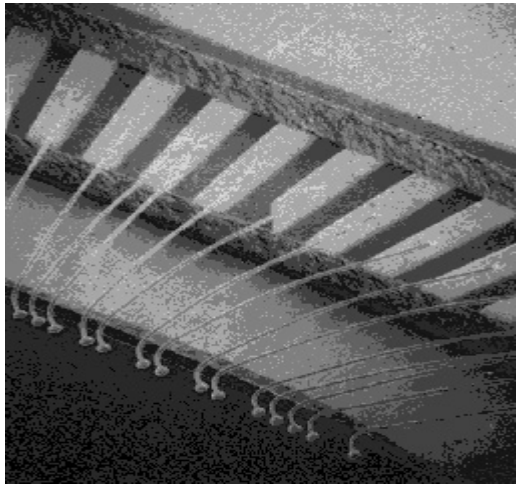
Wire Bonding



Ball Bond

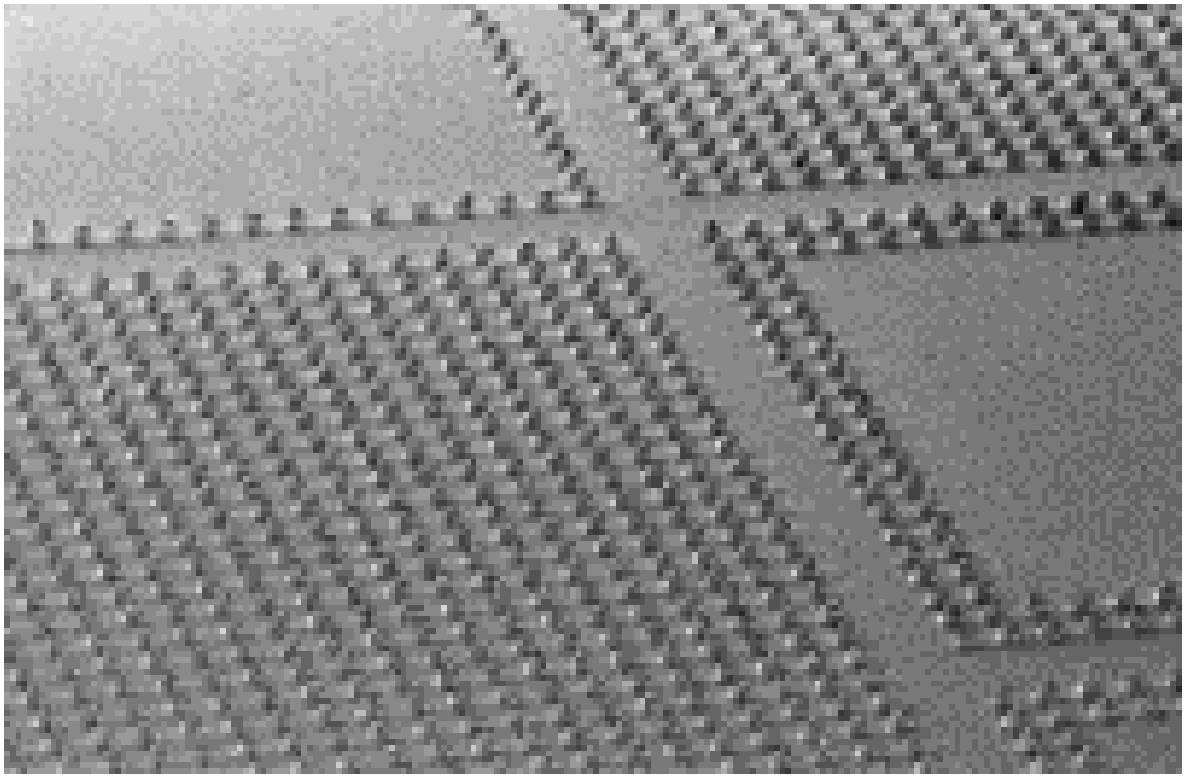


Termination Bond



Ball Bond Photograph

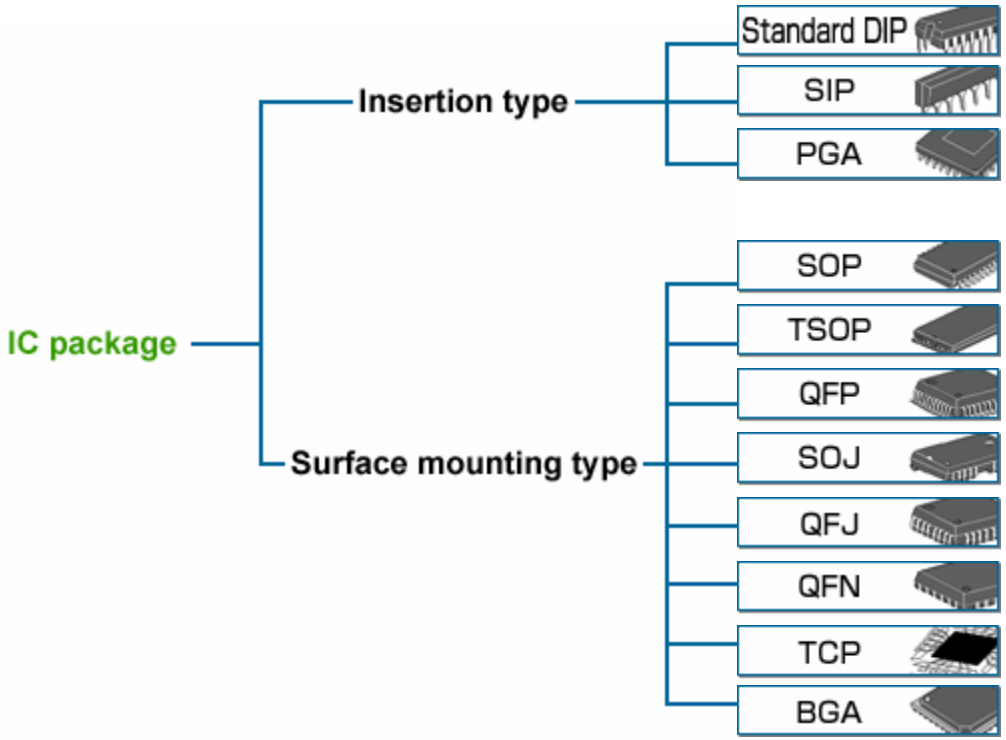
Bump Bonding



Packaging

1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models

Packaging



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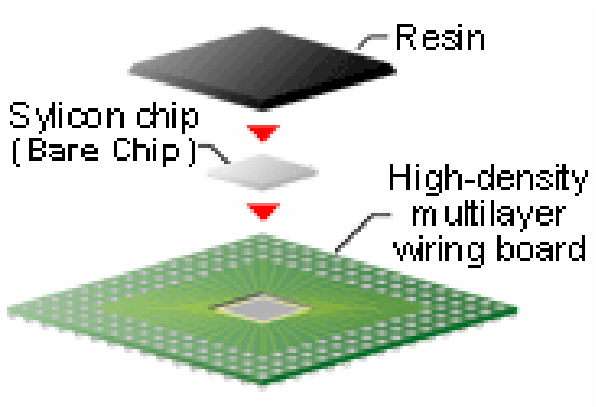
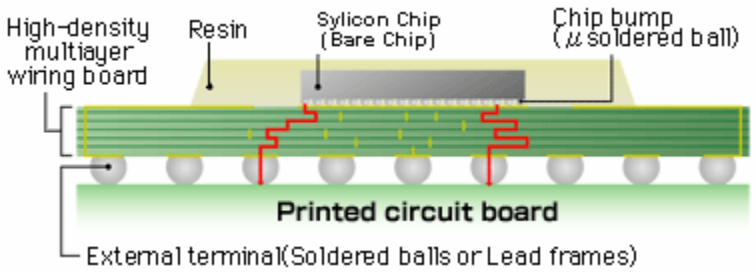
Packaging





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Basic Semiconductor Processes

MOS (Metal Oxide Semiconductor)

1.	NMOS	n-ch
2.	PMOS	p-ch
3.	CMOS	n-ch & p-ch
–	Basic Device:	MOSFET
–	Niche Device:	MESFET
–	Other Devices:	Diode BJT Resistors Capacitors Schottky Diode

Basic Semiconductor Processes

Bipolar

1. T^2L
2. ECL
3. I^2L
4. Linear ICs
   - Basic Device: BJT (Bipolar Junction Transistor)
   - Niche Devices: HBJT (Heterojunction Bipolar Transistor)
     HBT
   - Other Devices: Diode
     Resistor
     Capacitor
     Schottky Diode
     JFET (Junction Field Effect Transistor)

Basic Semiconductor Processes

Other Processes

- Thin and Thick Film Processes
  - Basic Device: Resistor
- BiMOS or BiCMOS
  - Combines both MOS & Bipolar Processes
  - Basic Devices: MOSFET & BJT
- SiGe
  - BJT with HBT implementation
- SiGe / MOS
  - Combines HBT & MOSFET technology
- SOI / SOS (Silicon on Insulator / Silicon on Sapphire)
- Twin-Well & Twin Tub CMOS
  - Very similar to basic CMOS but more optimal transistor char.