# EE 434
# Lecture 12

Process Flow (wrap up)

Device Modeling in Semiconductor Processes

# Quiz 6

How have process engineers configured a process to assure that the thickness of the gate oxide for the p-channel devices is nominally the same as that for the n-channel devices?

# And the number is ....

1

8

3

5

4

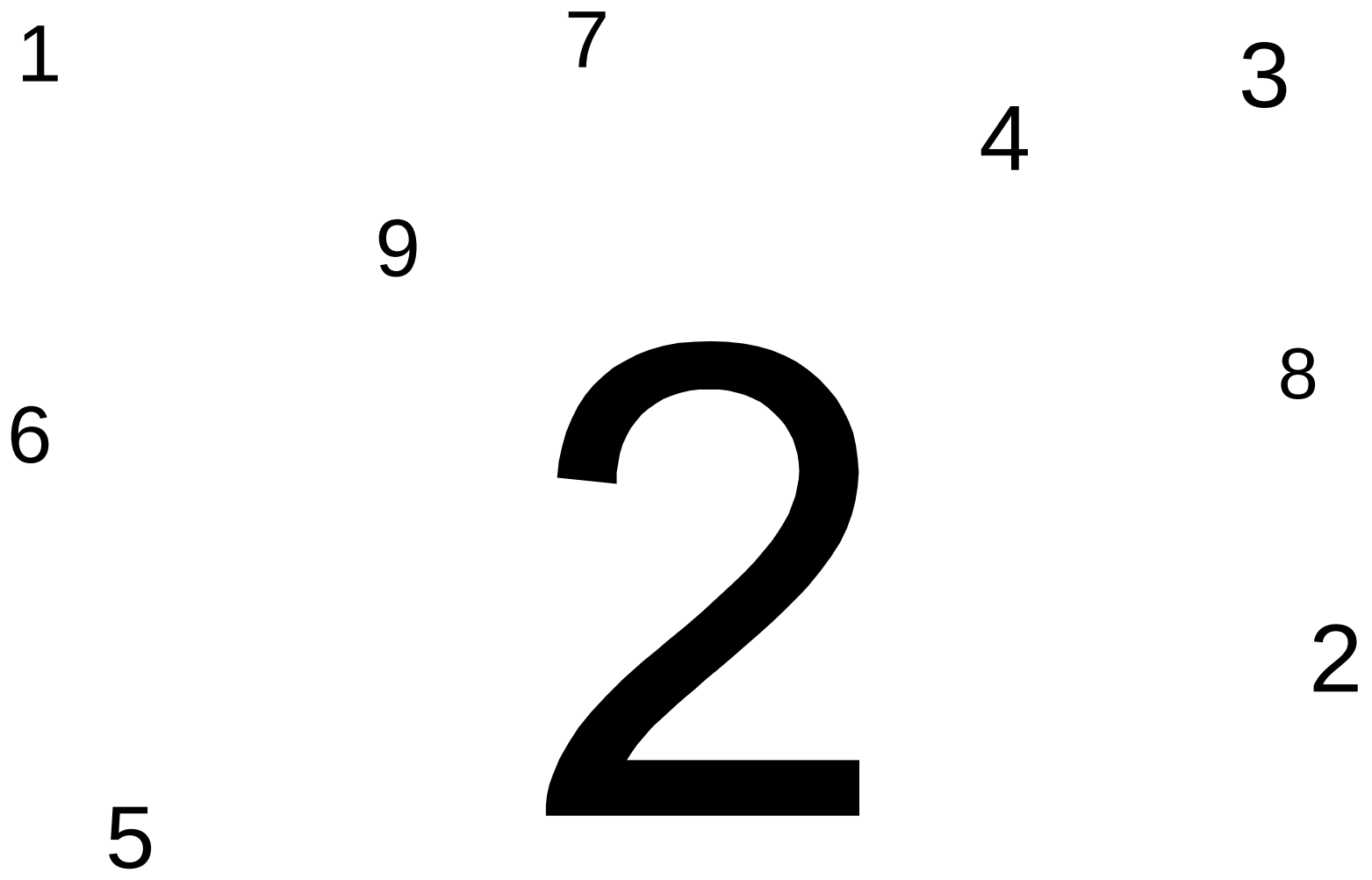
6

9

7

2

# And the number is ....



# Quiz 6

How have process engineers configured a process to assure that the thickness of the gate oxide for the p-channel devices is nominally the same as that for the n-channel devices?

Solution:

The same polysilicon layer is used to form the gates of both the n-channel and the p-channel transistors

$SiO_2$ is stripped and then regrown to assure uniformity of thin oxide across the whole wafer.

# Process Flow

## Processing Steps Have Been Discussed

Wafer Prep, Photolithography, Deposition, Etching, Diffusion, ...

## Combining these Processing Steps to Make Useful Integrated Circuits constitutes a Process Flow

Each Process has a unique process flow

Process flow constitutes very valuable IP

# APPENDIX 2B
# PROCESS CHARACTERIZATION OF A GENERIC CMOS PROCESS

**TABLE 2B.1**
**Process scenario of major process steps in typical p-well CMOS process[a]**

| | | |
|---|---|---|
| 1. | Clean wafer | |
| 2. | GROW THIN OXIDE | |
| 3. | Apply photoresist | |
| 4. | PATTERN P-WELL | (MASK #1) |
| 5. | Develop photoresist | |
| 6. | Deposit and diffuse p-type impurities | |
| 7. | Strip photoresist | |
| 8. | Strip thin oxide | |
| 9. | Grow thin oxide | |
| 10. | Apply layer of $Si_3N_4$ | |
| 11. | Apply photoresist | |
| 12. | PATTERN $Si_3N_4$ (active area definition) | (MASK #2) |
| 13. | Develop photoresist | |
| 14. | Etch $Si_3N_4$ | |
| 15. | Strip photoresist | |
| | *Optional field threshold voltage adjust* | |
| | A.1 Apply photoresist | |
| | A.2 PATTERN ANTIMOAT IN SUBSTRATE | (MASK #A1) |
| | A.3 Develop photoresist | |
| | A.4 FIELD IMPLANT (n-type) | |
| | A.5 Strip photoresist | |
| 16. | GROW FIELD OXIDE | |
| 17. | Strip $Si_3N_4$ | |
| 18. | Strip thin oxide | |
| 19. | GROW GATE OXIDE | |
| 20. | POLYSILICON DEPOSITION (POLY I) | |
| 21. | Apply photoresist | |
| 22. | PATTERN POLYSILICON | (MASK #3) |
| 23. | Develop photoresist | |
| 24. | ETCH POLYSILICON | |
| 25. | Strip photoresist | |
| | *Optional steps for double polysilicon process* | |
| | B.1 Strip thin oxide | |
| | B.2 GROW THIN OXIDE | |
| | B.3 POLYSILICON DEPOSITION (POLY II) | |
| | B.4 Apply photoresist | |
| | B.5 PATTERN POLYSILICON | (MASK #B1) |
| | B.6 Develop photoresist | |
| | B.7 ETCH POLYSILICON | |
| | B.8 Strip photoresist | |
| | B.9 Strip thin oxide | |

**TABLE 2B.1**
*(Continued)*

| | | |
|---|---|---|
| 26. | Apply photoresist | |
| 27. | PATTERN P-CHANNEL DRAINS AND SOURCES AND $P^+$ GUARD RINGS (p-well ohmic contacts) | (MASK #4) |
| 28. | Develop photoresist | |
| 29. | $p^+$ IMPLANT | |
| 30. | Strip photoresist | |
| 31. | Apply photoresist | |
| 32. | PATTERN N-CHANNEL DRAINS AND SOURCES AND $N^+$ GUARD RINGS (top ohmic contact to substrate) | (MASK #5) |
| 33. | Develop photoresist | |
| 34. | $n^+$ IMPLANT | |
| 35. | Strip photoresist | |
| 36. | Strip thin oxide | |
| 37. | Grow oxide | |
| 38. | Apply photoresist | |
| 39. | PATTERN CONTACT OPENINGS | (MASK #6) |
| 40. | Develop photoresist | |
| 41. | Etch oxide | |
| 42. | Strip photoresist | |
| 43. | APPLY METAL | |
| 44. | Apply photoresist | |
| 45. | PATTERN METAL | (MASK #7) |
| 46. | Develop photoresist | |
| 47. | Etch metal | |
| 48. | Strip photoresist | |
| | *Optional steps for double metal process* | |
| | C.1 Strip thin oxide | |
| | C.2 DEPOSIT INTERMETAL OXIDE | |
| | C.3 Apply photoresist | |
| | C.4 PATTERN VIAS | (MASK #C1) |
| | C.5 Develop photoresist | |
| | C.6 Etch oxide | |
| | C.7 Strip photoresist | |
| | C.8 APPLY METAL (Metal 2) | |
| | C.9 Apply photoresist | |
| | C.10 PATTERN METAL | (MASK #C2) |
| | C.11 Develop photoresist | |
| | C.12 Etch metal | |
| | C.13 Strip photoresist | |
| 49. | APPLY PASSIVATION | |
| 50. | Apply photoresist | |
| 51. | PATTERN PAD OPENINGS | (MASK #8) |
| 52. | Develop photoresist | |
| 53. | Etch passivation | |
| 54. | Strip photoresist | |
| 55. | ASSEMBLE, PACKAGE AND TEST | |

[a]Major functional steps shown in capital letters.

TABLE 2B.2
**Design rules for a typical p-well CMOS process (See Table 2B.3 in color plates for graphical interpretation)**

| | | Dimensions | |
|---|---|---|---|
| | | **Microns** | **Scalable** |
| 1. | p-well (CIF Brown, Mask #1[a]) | | |
| 1.1 | Width | 5 | 4λ |
| 1.2 | Spacing (different potential) | 15 | 10λ |
| 1.3 | Spacing (same potential) | 9 | 6λ |
| 2. | Active (CIF Green, Mask #2) | | |
| 2.1 | Width | 4 | 2λ |
| 2.2 | Spacing | 4 | 2λ |
| 2.3 | $p^+$ active in n-subs to p-well edge | 8 | 6λ |
| 2.4 | $n^+$ active in n-subs to p-well edge | 7 | 5λ |
| 2.5 | $n^+$ active in p-well to p-well edge | 4 | 2λ |
| 2.6 | $p^+$ active in p-well to p-well edge | 1 | λ |
| 3. | Poly (POLY I) (CIF Red, Mask #3) | | |
| 3.1 | Width | 3 | 2λ |
| 3.2 | Spacing | 3 | 2λ |
| 3.3 | Field poly to active | 2 | λ |
| 3.4 | Poly overlap of active | 3 | 2λ |
| 3.5 | Active overlap of poly | 4 | 2λ |
| 4. | $p^+$ select (CIF Orange, Mask #4) | | |
| 4.1 | Overlap of active | 2 | λ |
| 4.2 | Space to $n^+$ active | 2 | λ |
| 4.3 | Overlap of channel[b] | 3.5 | 2λ |
| 4.4 | Space to channel[b] | 3.5 | 2λ |
| 4.5 | Space to $p^+$ select | 3 | 2λ |
| 4.6 | Width | 3 | 2λ |
| 5. | Contact[c] (CIF Purple, Mask #6) | | |
| 5.1 | Square contact, exactly | 3 × 3 | 2λ × 2λ |
| 5.2 | Rectangular contact, exactly | 3 × 8 | 2λ × 6λ |
| 5.3 | Space to different contact | 3 | 2λ |
| 5.4 | Poly overlap of contact | 2 | λ |
| 5.5 | Poly overlap in direction of metal 1 | 2.5 | 2λ |
| 5.6 | Space to channel | 3 | 2λ |
| 5.7 | Metal 1 overlap of contact | 2 | λ |
| 5.8 | Active overlap of contact | 2 | λ |
| 5.9 | $p^+$ select overlap of contact | 3 | 2λ |
| 5.10 | Subs./well shorting contact, exactly | 3 × 8 | 2λ × 6λ |
| 6. | Metal 1[d] (CIF Blue, Mask #7) | | |
| 6.1 | Width | 3 | 2λ |
| 6.2 | Spacing | 4 | 3λ |
| 6.3 | Maximum current density | 0.8 mA/μ | 0.8 mA/μ |

**TABLE 2B.2**
*(Continued)*

| | | Dimensions | |
|---|---|---|---|
| | | **Microns** | **Scalable** |
| 7. | Via [e](CIF Purple Hatched, Mask #C1) | | |
| 7.1 | Size, exactly | 3 × 3 | 2λ × 2λ |
| 7.2 | Separation | 3 | 2λ |
| 7.3 | Space to poly edge | 4 | 2λ |
| 7.4 | Space to contact | 3 | 2λ |
| 7.5 | Overlap by metal 1 | 2 | λ |
| 7.6 | Overlap by metal 2 | 2 | λ |
| 7.7 | Space to active edge | 3 | 2λ |
| 8. | Metal 2 (CIF Orange Hatched, Mask #C2) | | |
| 8.1 | Width | 5 | 3λ |
| 8.2 | Spacing | 5 | 3λ |
| 8.3 | Bonding pad size | 100 × 100 | 100 μ × 100 μ |
| 8.4 | Probe pad size | 75 × 75 | 75 μ × 75 μ |
| 8.5 | Bonding pad separation | 50 | 50 μ |
| 8.6 | Bonding to probe pad | 30 | 30 μ |
| 8.7 | Probe pad separation | 30 | 30 μ |
| 8.8 | Pad to circuitry | 40 | 40 μ |
| 8.9 | Maximum current density | 0.8 mA/μ | 0.8 mA/μ |
| 9. | Passivation[f] (CIF Purple Dashed, Mask #8) | | |
| 9.1 | Bonding pad opening | 90 × 90 | 90 μ × 90 μ |
| 9.2 | Probe pad opening | 65 × 65 | 65 μ × 65 μ |
| 10. | Metal 2 crossing coincident metal 1 and poly[g] | | |
| 10.1 | Metal 1 to poly edge spacing when crossing metal 2 | 2 | λ |
| 10.2 | Rule domain | 2 | λ |
| 11. | Electrode (POLY II)[h] (CIF Purple Hatched, Mask #A1) | | |
| 11.1 | Width | 3 | 2λ |
| 11.2 | Spacing | 3 | 2λ |
| 11.3 | POLY I overlap of POLY II | 2 | λ |
| 11.4 | Space to contact | 3 | 2λ |

[a]Mask numbers are relative to the process scenario of Table 2B.1. CIF format discussed in footnote of Table 2A.2.
[b]Add 2.5 microns for a source/drain width of 3μ for worst-case mask misalignment.
[c]No contact to poly inside active.
[d]For single metal process, pads are made with metal 1 following design rules 8.3–8.8.
[e]Via must be on a flat surface; metal 1 must be under a via.
[f]There must be metal 2 under the pad openings in a double-metal process.
[g]Objective: Avoidance of too large a step for metal 2.
[h]POLY I must always be under POLY II.

**TABLE 2B.3**
**Graphical interpretation of CMOS design rules.**

*(See color plate 6 in insert section)*

**TABLE 2B.4**
**Process parameters for a typical[a] p-well CMOS process**

| | Typical | Tolerance[b] | Units |
|---|---|---|---|
| **Square law model parameters** | | | |
| $V_{T0}$ (threshold voltage) | | | |
| n-channel ($V_{TN0}$) | 0.75 | ± 0.25 | V |
| p-channel ($V_{TP0}$) | −0.75 | ± 0.25 | V |
| $K'$(conduction factor) | | | |
| n-channel | 24 | ± 6 | $\mu A/V^2$ |
| p-channel | 8 | ± 1.5 | $\mu A/V^2$ |
| $\gamma$(body effect) | | | |
| n-channel | 0.8 | ± 0.4 | $V^{1/2}$ |
| p-channel | 0.4 | ± 0.2 | $V^{1/2}$ |
| $\lambda$(channel length modulation) | | | |
| n-channel | 0.01 | ± 50% | $V^{-1}$ |
| p-channel | 0.02 | ± 50% | $V^{-1}$ |
| $\phi$(surface potential) | | | |
| n- and p-channel | 0.6 | ± 0.1 | V |
| **Process parameters** | | | |
| $\mu$ (channel mobility) | | | |
| n-channel | 710 | | $cm^2/(V \cdot s)$ |
| p-channel | 230 | | $cm^2/(V \cdot s)$ |
| **Doping[c]** | | | |
| $n^+$ active | 5 | ±4 | $10^{18}/cm^3$ |
| $p^+$ active | 5 | ±4 | $10^{17}/cm^3$ |
| p-well | 5 | ±2 | $10^{16}/cm^3$ |
| n-substrate | 1 | ±0.1 | $10^{16}/cm^3$ |
| **Physical feature sizes** | | | |
| $T_{OX}$ (gate oxide thickness) | 500 | ± 100 | Å |
| Total lateral diffusion | | | |
| n-channel | 0.45 | ± 0.15 | $\mu$ |
| p-channel | 0.6 | ± 0.3 | $\mu$ |
| Diffusion depth | | | |
| $n^+$ diffusion | 0.45 | ± 0.15 | $\mu$ |
| $p^+$ diffusion | 0.6 | ± 0.3 | $\mu$ |
| p-well | 3.0 | ± 30% | $\mu$ |
| **Insulating layer separation** | | | |
| POLY I to POLY II | 800 | ± 100 | Å |
| Metal 1 to Substrate | 1.55 | ± 0.15 | $\mu$ |
| Metal 1 to Diffusion | 0.925 | ± 0.25 | $\mu$ |
| POLY I to Substrate (POLY I on field oxide) | 0.75 | ± 0.1 | $\mu$ |
| Metal 1 to POLY I | 0.87 | ± 0.7 | $\mu$ |
| Metal 2 to Substrate | 2.7 | ± 0.25 | $\mu$ |
| Metal 2 to Metal I | 1.2 | ± 0.1 | $\mu$ |
| Metal 2 to POLY I | 2.0 | ± 0.07 | $\mu$ |

Note: $K' = \mu C_{ox}$ $24E-6 \neq (710)(69) \simeq 49.7E-6$

**TABLE 2B.4**
*(Continued)*

| | Typical | Tolerance[b] | Units |
|---|---|---|---|
| **Capacitances[d]** | | | |
| $C_{OX}$ (gate oxide capacitance, n- and p-channel) | 0.7 | ±0.1 | fF/$\mu^2$ |
| POLY I to substrate, poly in field | 0.045 | ±0.01 | fF/$\mu^2$ |
| POLY II to substrate, poly in field | 0.045 | ±0.01 | fF/$\mu^2$ |
| Metal 1 to substrate, metal in field | 0.025 | ±0.005 | fF/$\mu^2$ |
| Metal 2 to substrate, metal in field | 0.014 | ±0.002 | fF/$\mu^2$ |
| POLY I to POLY II | 0.44 | ±0.05 | fF/$\mu^2$ |
| POLY I to Metal 1 | 0.04 | ±0.01 | fF/$\mu^2$ |
| POLY I to Metal 2 | 0.039 | ±0.003 | fF/$\mu^2$ |
| Metal 1 to Metal 2 | 0.035 | ±0.01 | fF/$\mu^2$ |
| Metal 1 to diffusion | 0.04 | ±0.01 | fF/$\mu^2$ |
| Metal 2 to diffusion | 0.02 | ±0.005 | fF/$\mu^2$ |
| $n^+$ diffusion to p-well (junction, bottom) | 0.33 | ±0.17 | fF/$\mu^2$ |
| $n^+$ diffusion sidewall (junction, sidewall) | 2.6 | ±0.6 | fF/$\mu$ |
| $p^+$ diffusion to substrate (junction, bottom) | 0.38 | ±0.12 | fF/$\mu^2$ |
| $p^+$ diffusion sidewall (junction, sidewall) | 3.5 | ±2.0 | fF/$\mu$ |
| p-well to substrate (junction, bottom) | 0.2 | ±0.1 | fF/$\mu^2$ |
| p-well sidewall (junction, sidewall) | 1.6 | ±1.0 | fF/$\mu$ |
| **Resistances** | | | |
| Substrate | 25 | ±20% | Ω-cm |
| p-well | 5000 | ±2500 | Ω/□ |
| $n^+$ diffusion | 35 | ±25 | Ω/□ |
| $p^+$ diffusion | 80 | ±55 | Ω/□ |
| Metal | 0.003 | ±25% | Ω/□ |
| Poly | 25 | ±25% | Ω/□ |
| Metal 1–Metal 2 via (3 $\mu$ × 3 $\mu$ contact) | <0.1 | | Ω |
| Metal 1 contact to POLY I (3 $\mu$ × 3 $\mu$ contact) | <10 | | Ω |
| Metal 1 contact to $n^+$ or $p^+$ diffusion (3 $\mu$ × 3 $\mu$ contact) | <5 | | Ω |
| **Breakdown voltages, leakage currents, migration currents and operating conditions** | | | |
| Punchthrough voltages (Gate oxide, POLY I to POLY II) | >10 | | V |
| Diffusion reverse breakdown voltage | >10 | | V |
| p-well to substrate reverse breakdown voltage | >20 | | V |
| Metal 1 in field threshold voltage | >10 | | V |
| Metal 2 in field threshold voltage | >10 | | V |
| Poly-field threshold voltage | >10 | | V |
| Maximum operating voltage | 7.0 | | V |
| $n^+$ diffusion to p-well leakage current | 0.25 | | fA/$\mu^2$ |
| $p^+$ diffusion to substrate leakage current | 0.25 | | fA/$\mu^2$ |
| p-well leakage current | 0.25 | | fA/$\mu^2$ |
| Maximum metal current density | 0.8 | | mA/$\mu$ width |
| Maximum device operating temperature | 200 | | °C |

[a] Parameters based upon a $3\mu$ ($\lambda = 1.5\mu$) CMOS process.

[b] The tolerance is in terms of the absolute value of the parameter relative to processing variations from run to run. Matching characteristics on a die are much better. For example, chip-level matching of $V_{T0}$ is in the 1 $mV$ to 20 $mV$ range, and K′ matching is in the 0.5% to 5% range.[18–22]

[c] Impurity concentration varies with depth.

[d] Junction capacitances at zero bias.

**TABLE 2B.5**
**SPICE MOSFET model parameters of a typical p-well CMOS process (MOSIS[a])**

| Parameter (Level 2 model) | n-channel | p-channel | Units |
|---|---|---|---|
| VTO | 0.827 | −0.895 | V |
| KP | 32.87 | 15.26 | $\mu A/V^2$ |
| GAMMA | 1.36 | 0.879 | $V^{1/2}$ |
| PHI | 0.6 | 0.6 | V |
| LAMBDA | 1.605E−2 | 4.709E−2 | $V^{-1}$ |
| CGSO | 5.2E−4 | 4.0E−4 | fF/$\mu$ width |
| CGDO | 5.2E−4 | 4.0E−4 | fF/$\mu$ width |
| RSH | 25 | 95 | $\Omega/\square$ |
| CJ | 3.2E−4 | 2.0E−4 | p/fF/$\mu^2$ |
| MJ | 0.5 | 0.5 | |
| CJSW | 9.0E−4 | 4.5E−4 | p/fF/$\mu$ perimeter |
| MJSW | 0.33 | 0.33 | |
| TOX | 500 | 500 | Å |
| NSUB | 1.0E16 | 1.12E14 | $1/cm^3$ |
| NSS | 0 | 0 | $1/cm^2$ |
| NFS | 1.235E12 | 8.79E11 | $1/cm^2$ |
| TPG | 1 | −1 | |
| XJ | 0.4 | 0.4 | $\mu$ |
| LD | 0.28 | 0.28 | $\mu$ |
| UO | 200 | 100 | $cm^2/(V \cdot s)$ |
| UCRIT | 9.99E5 | 1.64E4 | V/cm |
| UEXP | 1.001E−3 | 0.1534 | |
| VMAX | 1.0E5 | 1.0E5 | m/s |
| NEFF | 1.001E−2 | 1.001E−2 | |
| DELTA | 1.2405 | 1.938 | |

verify units before final corrections

[a] The SPICE parameters were obtained by assuming them to be empirical parameters and then fitting measured device characteristics to the mathematical equations which comprise the model by using a numerical optimization algorithm. This approach gives good fit to the model but causes a deviation from the typical parameters of Table 2A.4 and results in parameter relationships which may not be self-consistent with some of the fundamental relationships developed in Chapters 3 and 4.

# Basic Devices

- Devices in Standard Processes
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (in some processes)
    - npn
    - pnp
- Niche Devices
  - Photodetectors
  - MESFET
  - Schottky Diode (not Shockley)
  - MEM Devices
  - ….

**Primary Consideration in This Course**

**Limited Consideration in This Course**

# Basic Devices and Device Models

- Resistor
- Capacitor
- MOSFET
- Diode
- BJT

# Basic Devices and Device Models

- Resistor
- Capacitor
- MOSFET
- Diode
- BJT

- Resistors and Capacitors were discussed previously in the context of interconnects
- Were generally considered parasitics in earlier discussions
- Will now be considered as desired components
- Models obviously will be very similar or identical

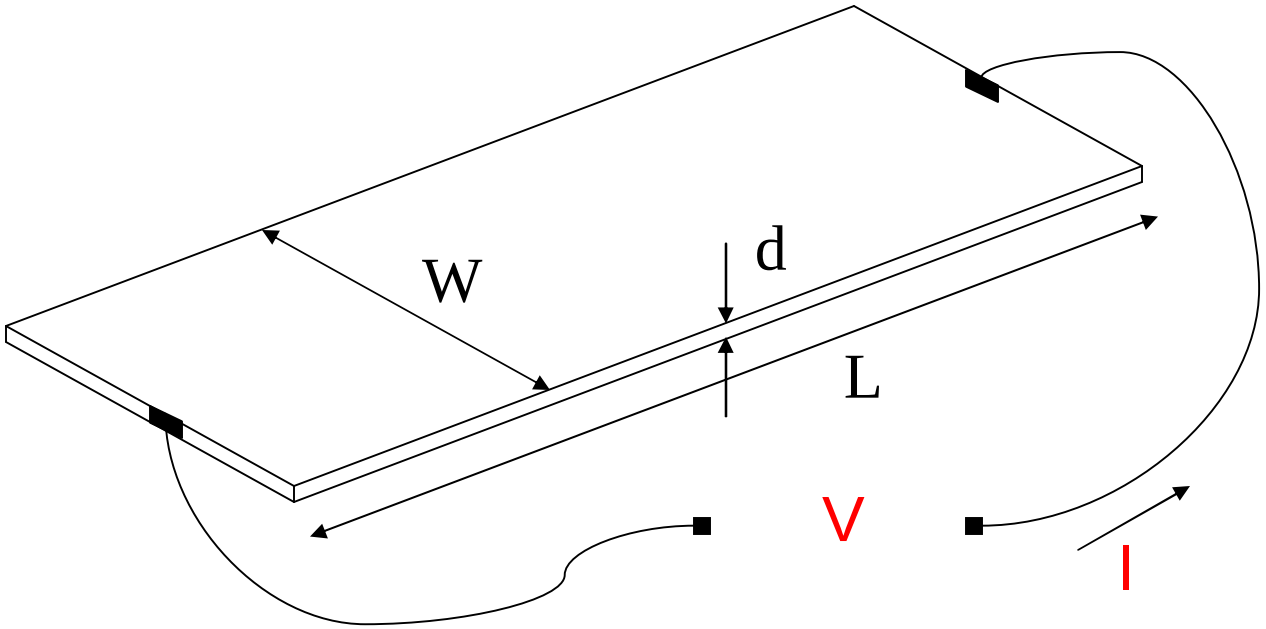
# Basic Devices and Device Models

- Resistor
- Capacitor
- MOSFET
- Diode
- BJT

# Resistors

- Generally thin-film devices
- Almost any thin-film layer can be used as a resistor
  - Diffused resistors
  - Poly Resistors
  - Metal Resistors
  - “Thin-film” adders (SiCr or NiCr)
- Subject to process variations, gradient effects and local random variations
- Often temperature and voltage dependent
  - Ambient temperature
  - Local Heating
- Nonlinearities often a cause of distortion when used in circuits
- Trimming possible resistors
  - Laser,links,switches

# Resistor Model

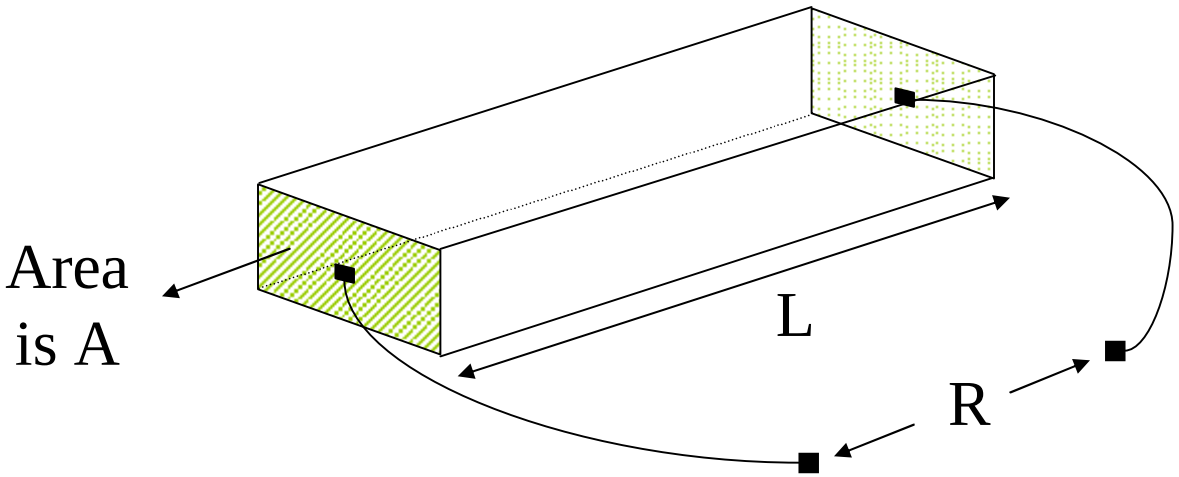



Model:

$$R = \frac{V}{I}$$

# Resistivity

- Volumetric measure of conduction capability of a material

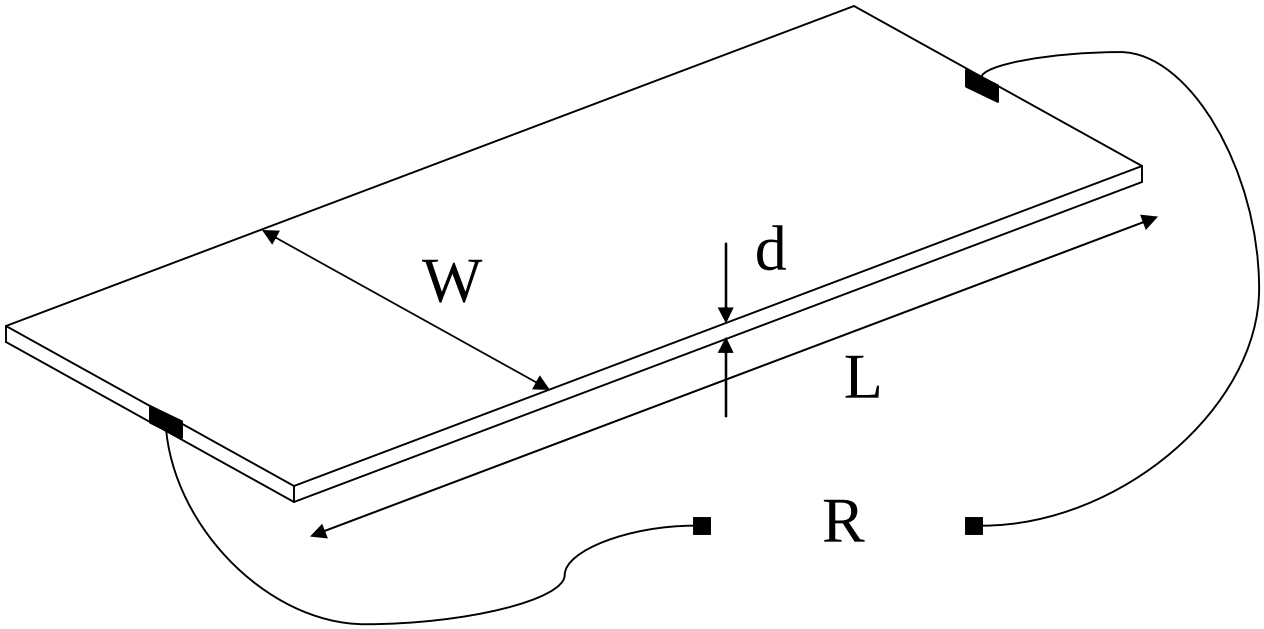



$$r = \frac{AR}{L}$$

units : ohm cm

for homogeneous material,
$\rho \perp A, R, L$

# Sheet Resistance




$$R_{\square} = \frac{RW}{L} \quad (\text{ for } d << w,\ d << L\ ) \qquad \text{units : ohms / } \square$$

for homogeneous materials, $R_{\square}$ is independent of W, L, R

# Relationship between ρ and $R_{\square}$

$$R_{\square} = \frac{RW}{L}$$

$$r = \frac{AR}{L}$$

$$\Longrightarrow \quad r = \frac{A}{W} R_{\square}$$

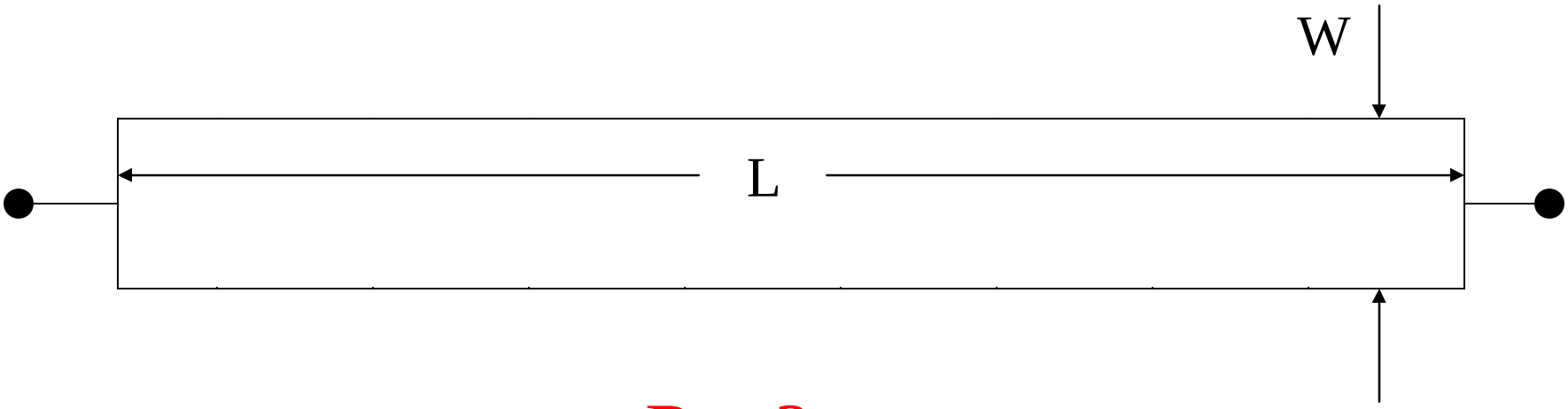
$$A = W \times d$$

$$r = \frac{A}{W} R_{\square} = \frac{W\,d}{W} R_{\square} = d \times R_{\square}$$

Number of squares, $N_S$, often used instead of L / W in determining resistance of film resistors

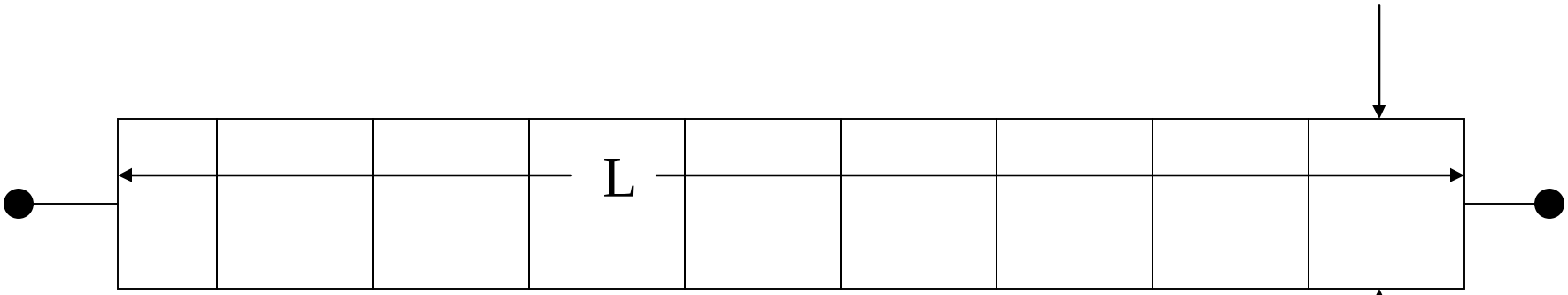
$$R = R_{\square} N_S$$

# Example 1



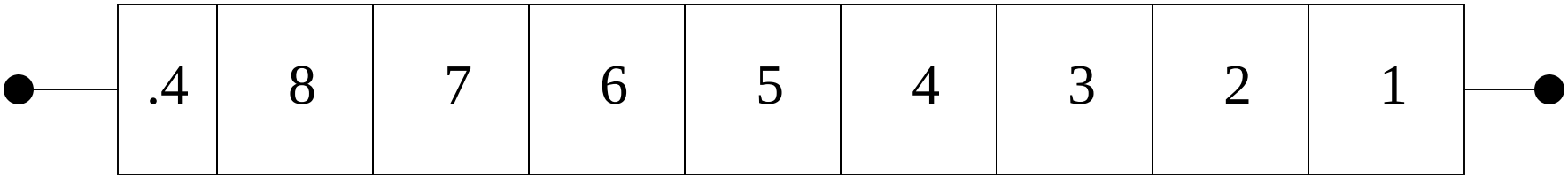

R = ?

# Example 1



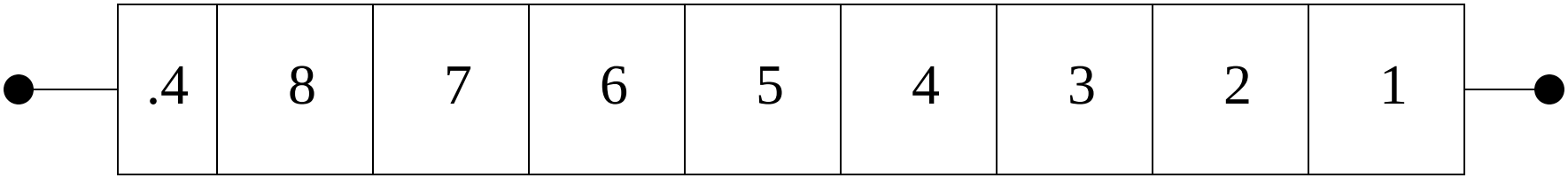

$$\frac{\mathbf{L}}{\mathbf{W}} = \mathbf{N_S}$$

# Example 1




R = ?

# Example 1

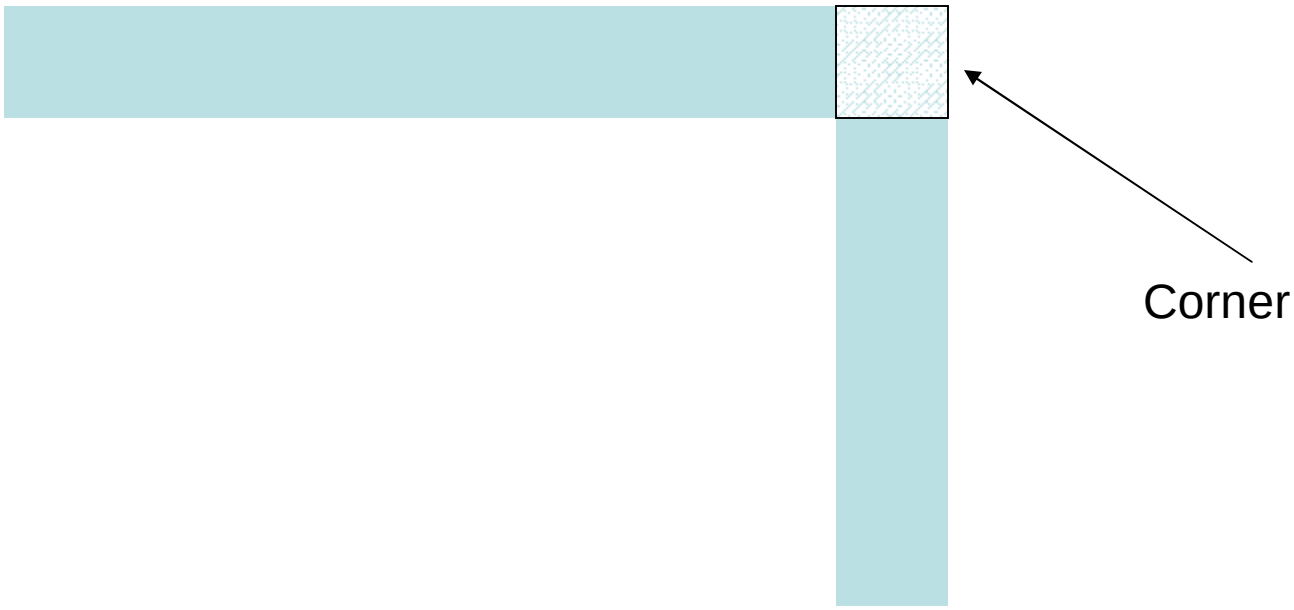



$R = ?$

$N_S = 8.4$

**$R = R_{\square}$ (8.4)**

# Corners in Film Resistors

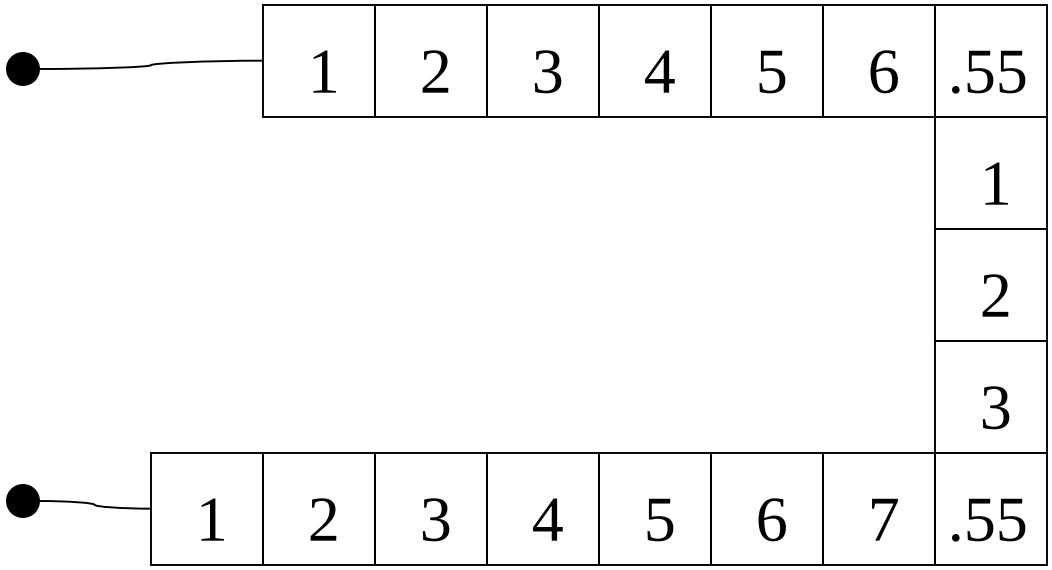



Rule of Thumb: .55 squares for each corner

# Example 2

Determine R if $R_{\square} = 100\ \Omega / \square$

# Example 2




$N_S$=17.1

R = (17.1) $R_{\square}$

R = 1710 Ω

# Resistivity of Materials used in Semiconductor Processing

- Cu: 1.7*E*-6 Ωcm
- Al: 2.7*E*-4 Ωcm
- Gold: 2.4*E*-6 Ωcm
- Platinum: 3.0*E*-6 Ωcm
- n-Si: .25 to 5 Ωcm
- intrinsic Si: 2.5*E5* Ωcm
- $SiO_2$: *E*14 Ωcm

# Temperature Coefficients

Used for indicating temperature sensitivity of resistors & capacitors

**For a resistor:**

$$TCR = \left( \frac{1}{R} \frac{dR}{dT} \right)_{\text{op. temp}}^{10^6} \qquad \text{ppm}/^\circ\text{C}$$

This diff eqn can easily be solved if TCR is a constant

$$R(T_2) = R(T_1) e^{\frac{T_2 - T_1}{10^6} TCR}$$

$$\boxed{R(T_2) \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right]}$$

Identical Expressions for Capacitors

# Voltage Coefficients

Used for indicating voltage sensitivity of resistors & capacitors

**For a resistor:**

$$\mathbf{VCR} = \left( \frac{1}{R} \frac{dR}{dV} \right)_{\text{ref voltage}}^{10^6} \qquad \mathbf{ppm/V}$$

This diff eqn can easily be solved if VCR is a constant

$$R(V_2) = R(V_1)\, e^{\frac{V_2 - V_1}{10^6} VCR}$$

$$\boxed{R(V_2) \approx R(V_1)\left[1 + (V_2 - V_1)\frac{VCR}{10^6}\right]}$$

Identical Expressions for Capacitors

# Temperature and Voltage Coefficients

- Temperature and voltage coefficients often quite large for diffused resistors
- Temperature and voltage coefficients often quite small for poly and metal resistors

# Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

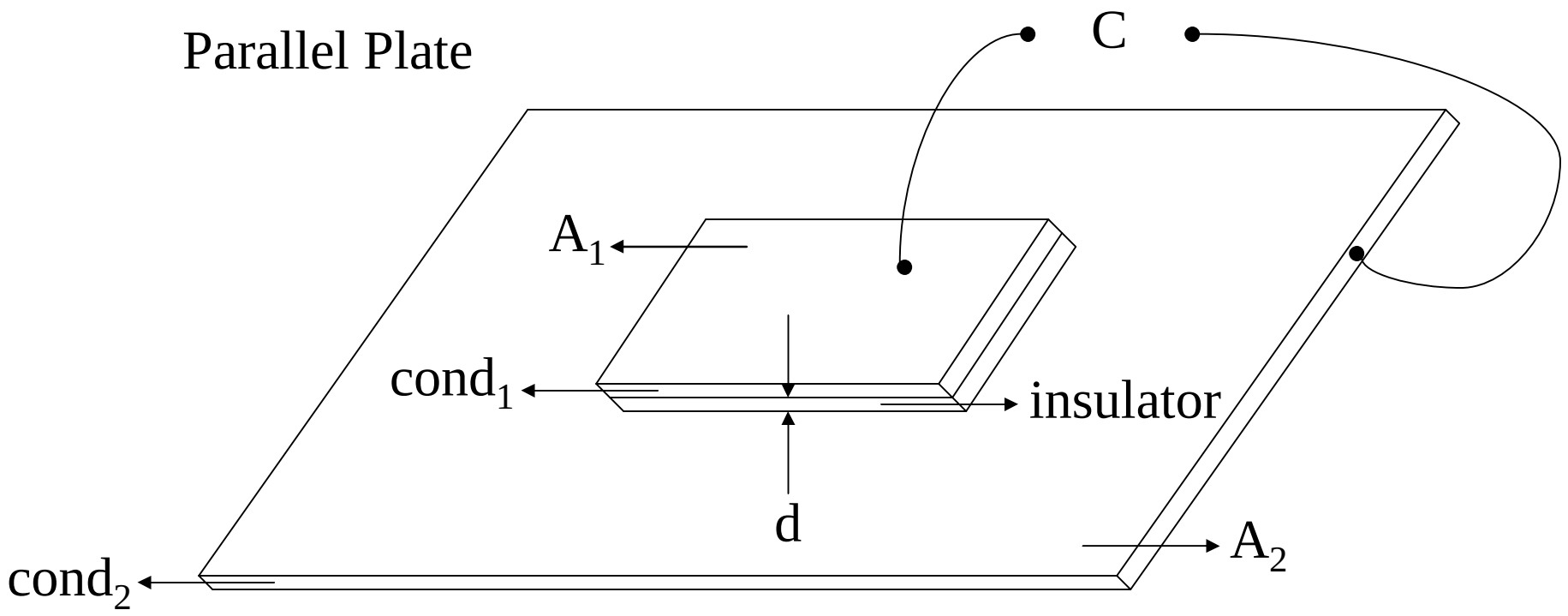
www.mosis.org

# Basic Devices and Device Models

- Resistor
- Capacitor
- MOSFET
- Diode
- BJT

# Capacitance

Parallel Plate




$$C = \frac{\in A}{d}$$

A = area of intersection of $A_1$ & $A_2$

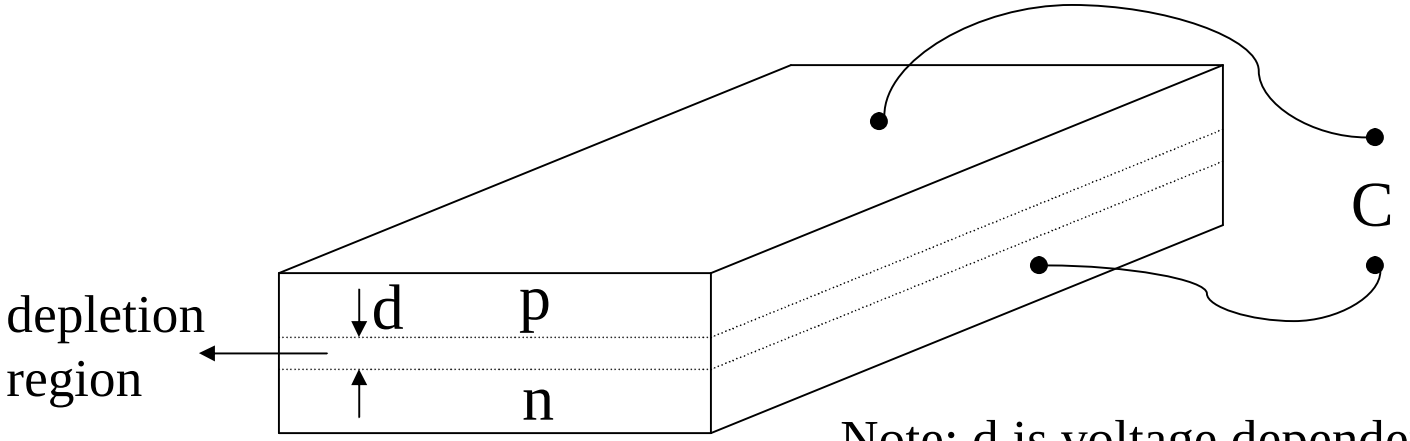
# Capacitance

Parallel Plate

$$\text{If } C_d = \frac{\text{Cap}}{\text{unit area}} \qquad C = C_d A \qquad \text{where } C_d = \frac{\in}{d}$$

# Capacitance

Junction Capacitor




$$C = \frac{\in A}{d}$$

Note: d is voltage dependent
-capacitance is voltage dependent
-usually parasitic caps
-varicaps or varactor diodes exploit voltage dep. of C