EE 434
Lecture 27

High Frequency Device Models

- Voltage Effects on MOS Devices
- BJT Models

Review from Last Time

Types of Capacitors

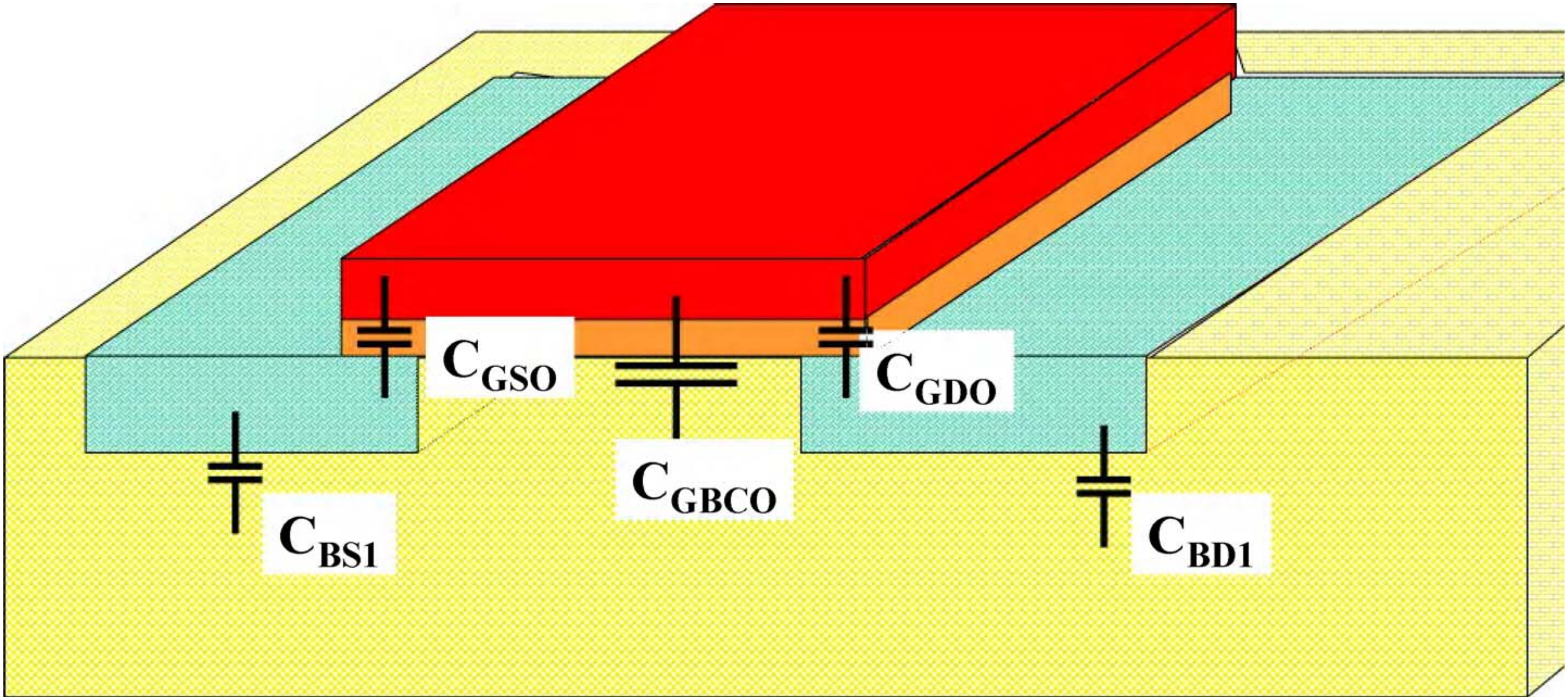
1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent
   a. Fixed Geometry
   b. Junction

Review from Last Time

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff



Overlap Capacitors: C_{GDO}, C_{GSO}

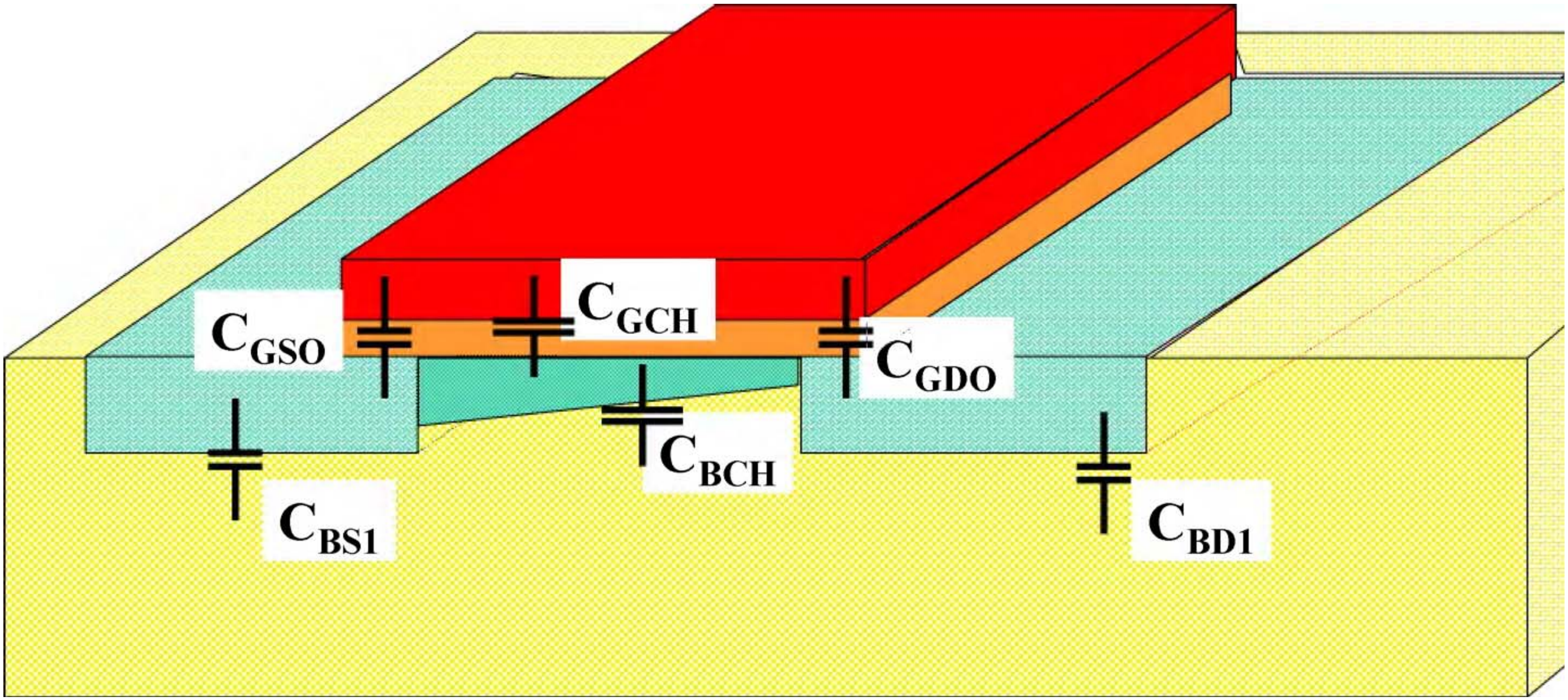
Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

Review from Last Time

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



Overlap Capacitors: C_{GDO}, C_{GSO}

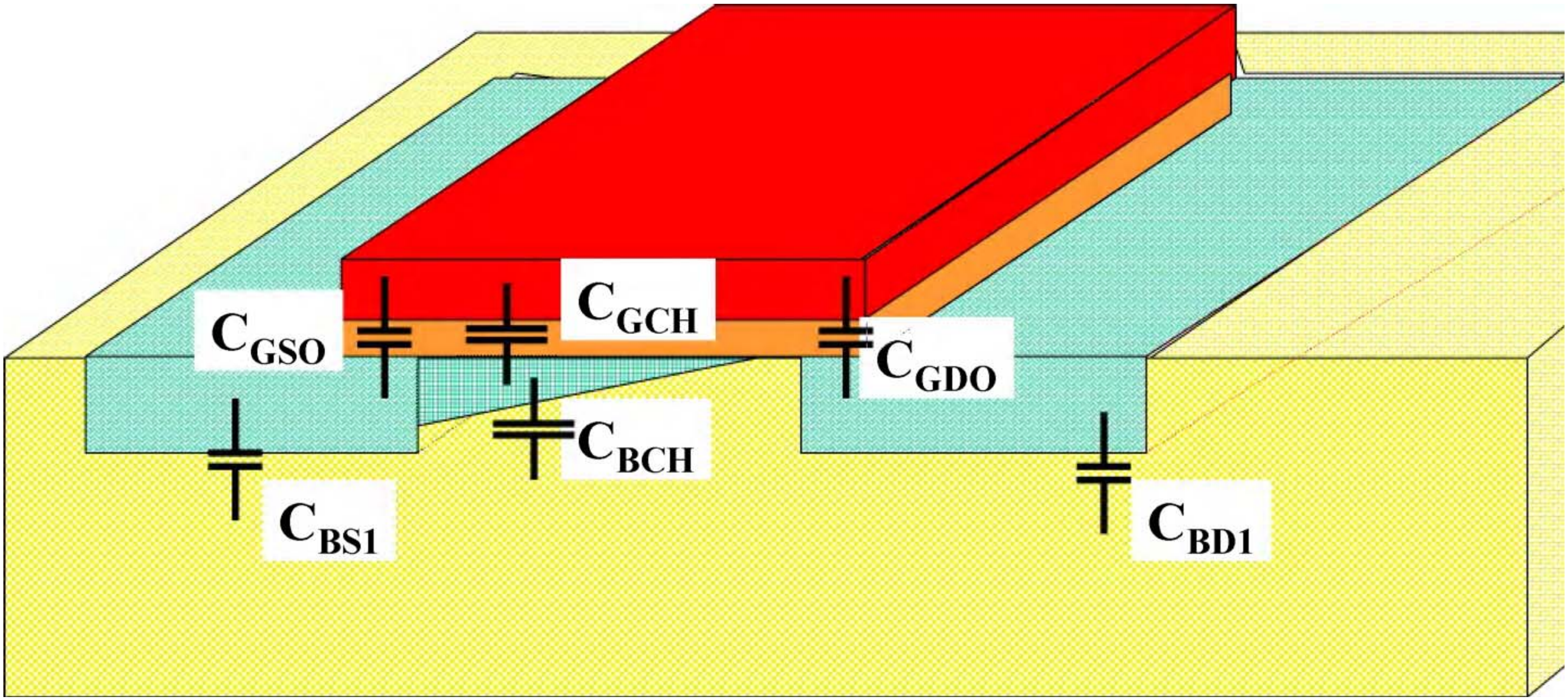
Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH} , C_{BCH}

Review from Last Time

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation



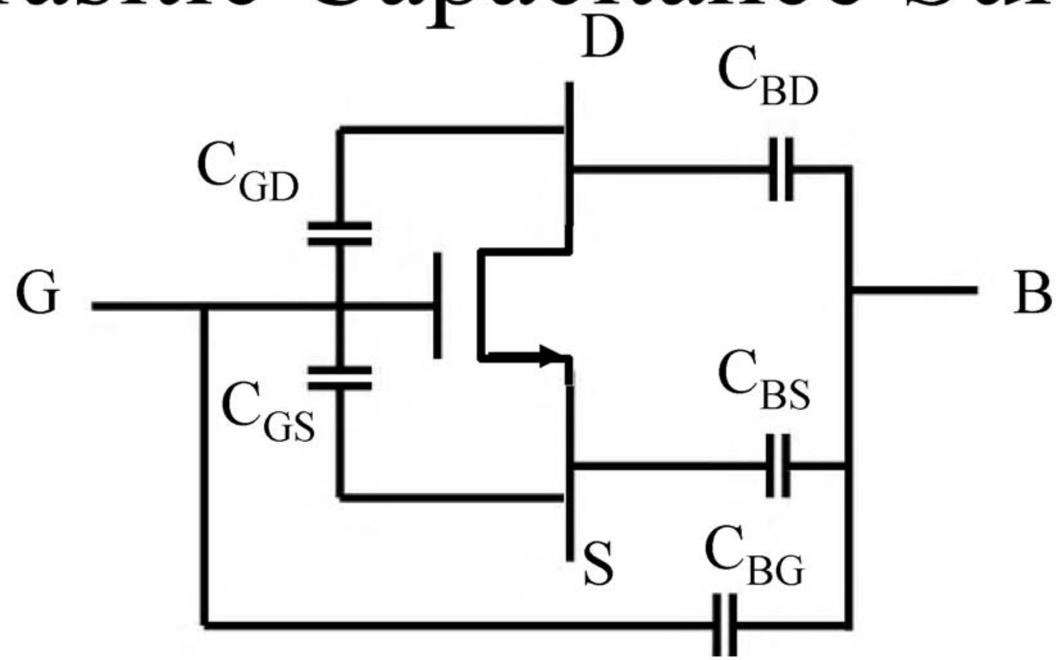
Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Saturation Capacitors: C_{GCH} , C_{BCH}

Review from Last Time

Parasitic Capacitance Summary



• { W/L }

• { W, L }

2 D.O.F. for high f circuits

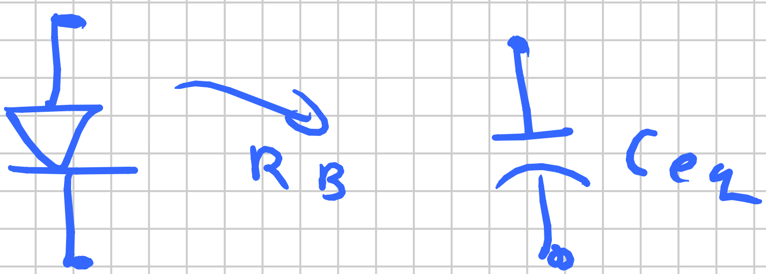
	Cutoff	Ohmic	Saturation
C_{GS}	$C_{OX}WL_D$	$C_{OX}WL_D + 0.5C_{OX}WL$	$C_{OX}WL_D+(2/3)C_{OX}WL$
C_{GD}	$C_{OX}WL_D$	$C_{OX}WL_D + 0.5C_{OX}WL$	$C_{OX}WL_D$
C_{BG}	$C_{OX}WL$ (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

- Why do high freq model errors in the parasitic capacitances not cause major concerns for trusting simulators?
  - These errors are of some concern
  - Most good designs will not have key performance char. that are strongly dependent upon exact models of parasitic capacitors

Voltage Dependence of Parasitic Capacitances

1) Voltage across p-n junctions

2) Voltage across G - Channel in Cutoff



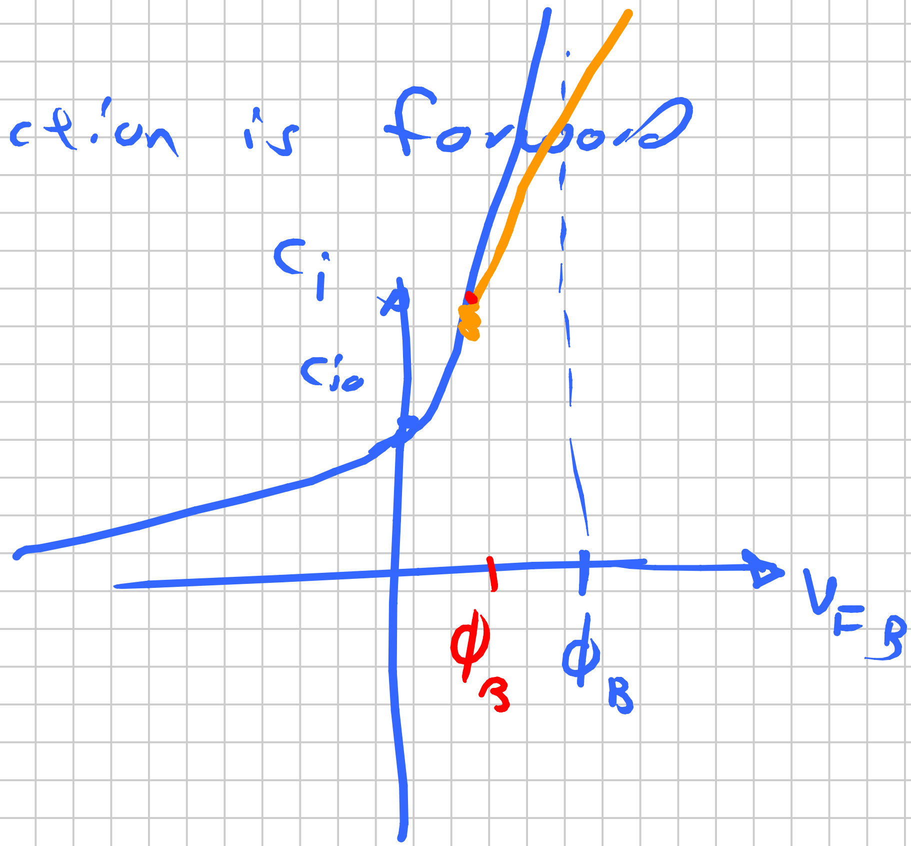
$$+ \frac{C_{js} P}{\left(1 - \frac{V_{FB}}{\phi_B}\right)^{n_2}}$$

$$C_j = \frac{C_{j0} A}{\left(1 - \frac{V_{FB}}{\phi_B}\right)^{n_1}}$$

$$V_{FB} < \frac{\phi_B}{2}$$

$$\phi_B \simeq .6V$$

• what happens if junction is forward biased ?



$$C_j = \frac{C_{jo} A}{\left(1 - \frac{V_{FB}}{\phi_B}\right)^n}$$

$V_{FB} < \frac{\phi_B}{2}$

Assume C_j is linear with V_{FB} for $V_{FB} > \phi_B$ and continuous, and differentiable at $V_{FB} = \phi_B$

To model C_i for $V_{FB} > \frac{\phi_B}{2}$

$$\left.\frac{\partial C_i}{\partial V_{FB}}\right|_{V_{FB}=\frac{\phi_B}{2}} = m$$

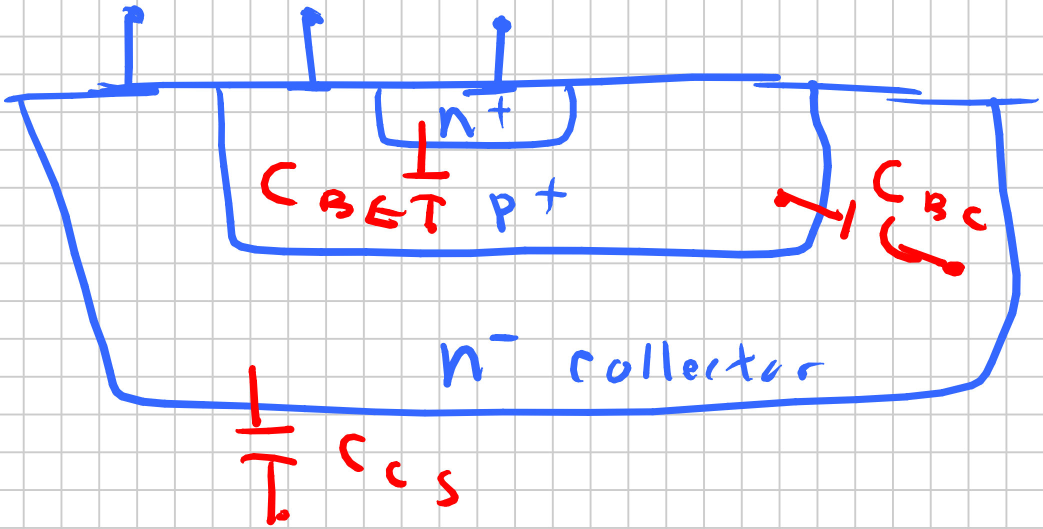
for $V_{FB} > \frac{\phi_B}{2}$

$$C_i = m V_{FB} + h$$

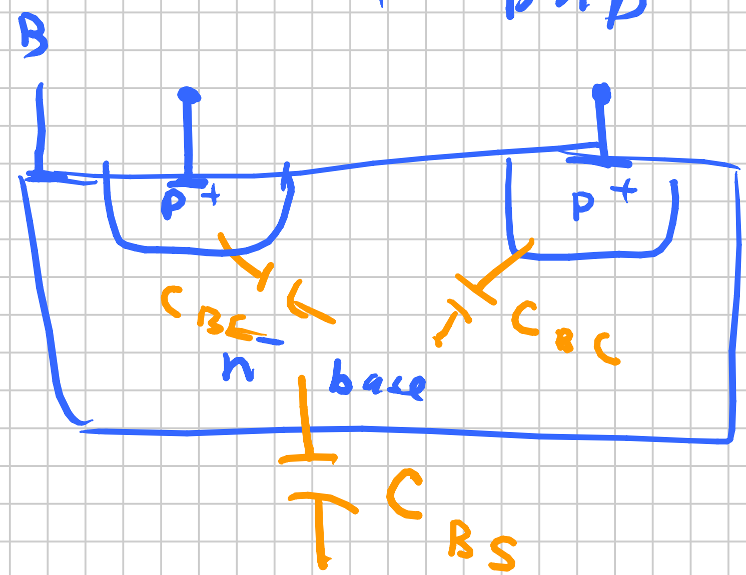
$$C_{i\,\frac{\phi_B}{2}} = m\frac{\phi_B}{2} + h \Rightarrow h = C_{i\,\frac{\phi_B}{2}} - m\frac{\phi_B}{2}$$

High F Bipolar Model

Vertical (npn)



Lateral pnp



For vertical transistor

$$\{ C_{BE}, C_{BC}, C_{CS} \}$$

$$C_i = \begin{cases} \dfrac{C_{io} A}{\left(1 - \dfrac{V_{FB}}{\phi_B}\right)^n} & V_{FB} < \dfrac{\phi_B}{2} \\ 2^n C_{io} A \left[\dfrac{2n V_{FB}}{\phi_B} + (1-n) \right] & V_{FB} > \dfrac{\phi_B}{2} \end{cases}$$

	Vertical	Lateral
C_{BE}	$C_{BE}' + C_{AC}$	$C_{BE}' + C_{AC}$
C_{BC}	C_{BC}	C_{BC}
C_{BS}	0	C_{BS}
C_{CS}	C_{CS}	0
C_{ES}	0	0

C_{BE}' ~ Forward Biased p-n eqn.

For BJT, carrier charge accumulation in base region adds to C_{BE}

$$C_{AC} = \frac{\tau_F I_{CQ}}{kT/q}$$

τ_F = Forward Base Transit Time

$$C_{AC} = \tau_F g_m$$

- Models of BJT for computer simulation

Models for Computer Simulation