EE 434
Lecture 27

High Frequency Device Models

- Voltage Effects on MOS Devices
- BJT Models
Types of Capacitors

1. Fixed Capacitors
   a. Fixed Geometry
   b. Junction

2. Operating Region Dependent
   a. Fixed Geometry
   b. Junction
Review from Last Time
Parasitic Capacitors in MOSFET
Operation Region Dependent -- Cutoff

Overlap Capacitors: $C_{GDO}, C_{GSO}$
Junction Capacitors: $C_{BS1}, C_{BD1}$
Cutoff Capacitor: $C_{GBCO}$
Review from Last Time

Parasitic Capacitors in MOSFET
Operation Region Dependent -- Ohmic

Overlap Capacitors: $C_{GDO}, C_{GSO}$
Junction Capacitors: $C_{BS1}, C_{BD1}$
Ohmic Capacitor: $C_{GCH}, C_{BCH}$
Review from Last Time

Parasitic Capacitors in MOSFET
Operation Region Dependent -- Saturation

Overlap Capacitors: $C_{GDO}$, $C_{GSO}$
Junction Capacitors: $C_{BS1}$, $C_{BD1}$
Saturation Capacitors: $C_{GCH}$, $C_{BCH}$
Review from Last Time
Parasitic Capacitance Summary

- \[ \frac{w}{L} \]
- \[ \sum w, L \]

2 D.O.F. for high f circuits

<table>
<thead>
<tr>
<th></th>
<th>Cutoff</th>
<th>Ohmic</th>
<th>Saturation</th>
</tr>
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<tbody>
<tr>
<td>C_{GS}</td>
<td>CoxWL_D</td>
<td>CoxWL_D + 0.5C_{Ox}WL</td>
<td>CoxWL_D + (2/3)C_{Ox}WL</td>
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</tr>
<tr>
<td>C_{BG}</td>
<td>CoxWL (or less)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>C_{BS}</td>
<td>( C_{BOT}A_s + C_{SW}P_s )</td>
<td>( C_{BOT}A_s + C_{SW}P_s + 0.5WL C_{BOTCH} )</td>
<td>( C_{BOT}A_s + C_{SW}P_s + (2/3)WL C_{BOTCH} )</td>
</tr>
<tr>
<td>C_{BD}</td>
<td>( C_{BOT}A_d + C_{SW}P_d )</td>
<td>( C_{BOT}A_d + C_{SW}P_d + 0.5WL C_{BOTCH} )</td>
<td>( C_{BOT}A_d + C_{SW}P_d )</td>
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Why do high frequency model errors in the parasitic capacitances not cause major concerns for trusting simulators?

- These errors are of some concern

- Most good designs will not have key performance characteristics that are strongly dependent upon exact models or parasitic capacitances
Voltage Dependence of Parasitic Capacitances

1) Voltage across p-n junctions

2) Voltage across G-channel in cutoff

\[ R_B = \frac{1}{C_{eq} + \frac{C_{js} P}{(1 - \frac{V_{FB}}{\phi_B})^n}} \]

\[ C_{js} = \frac{C_{j0} A}{(1 - \frac{V_{FB}}{\phi_B})^n} \]

\[ V_{FB} < \frac{\phi_B}{2} \]

\[ \phi_B = 0.6 \text{V} \]
What happens if function is for good biased?

\[ C_i = C_{i_0} \frac{A}{\left(1 - \frac{V_{FB}}{\phi_B}\right)^n} \]

\[ V_{FB} < \frac{\phi_B}{2} \]

Assume \( C_i \) is linear with \( V_{FB} \) for \( V_{FB} > \phi_B \) and continuous at \( V_{FB} = \phi_B \) and differentiable.
To model $C_i$ for $\phi < V_{FB} > \phi_{B}$

\[ \frac{\partial C_i}{\partial V_{FB}} |_{V_{FB} = \phi_{B}} = m \]

\[ V_{FB} = \phi_{B} \]

For $V_{FB} > \frac{d_{B}}{2}$

\[ C_i = m V_{FB} + h \]

\[ C_i \phi_{B} = m \phi_{B} + h = 0 \]

\[ h = C_i \phi_{B} - m \phi_{B} \]
High F Bipolar Model

Vertical (nnpn)

For vertical transistor:
\[ \{ C_B E, C_{BE}, C_{CE}, C_{CS} \} \]
\[ C_i = \begin{cases} 
\frac{C_{10} A}{\left(1 - \frac{V_{F_B}}{\phi_B}\right)^n} & \text{if } V_{F_B} < \frac{\phi_B}{2} \\
2 C_{10} A \left[ \frac{2^n V_{F_B}}{\phi_B} + (1-n) \right] & \text{if } V_{F_B} > \frac{\phi_B}{2} 
\end{cases} \]
Vertical

$C_{BBE} \quad C_{BC} + C_{AC}$

Lateral

$C_{BEC} + C_{AC}$

$C_{BC}$

$C_{BE} \quad C_{BS}$

$C_{CS}$

For BJT, carrier charge accumulation in base region

$C_{AC} = \frac{E_{F} - E_{C}}{kT/q}$

$\tau = \frac{Forward \quad Back}{Transit \quad Time}$

$C_{AC} = L = 9 \mu m$
Models of BJT for computer simulation
Models for Computer Simulation

Simple dc Model

- Small Signal Model
  - Frequency-Dependent Small Signal Model
- Better Analytical dc Models
- Sophisticated Model for Computer Simulations
  - Better Models for Predicting Device Operation