EE 434

Lecture 35

Device Sizing

Propagation Delay in Logic Circuits
Propagation Delay in Static CMOS Family

If $u_nC_{OX} = 100 \mu A V^{-2}$, $C_{OX} = 4 fF \mu^{-2}$, $V_{Tn} = V_{DD}/5$, $V_{TP} = -V_{DD}/5$, $\mu_n/\mu_p = 3$, $L_1 = W_1 = L_{MIN}$, $L_2 = W_2 = L_{MIN}$, $L_{MIN} = 0.5 \mu$ and $V_{DD} = 5V$

$$R_{PD} = \frac{1}{10^{-4} \cdot 0.8V_{DD}} = 2.5K\Omega$$

$$R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8V_{DD}} = 7.5K\Omega$$

$$C_{IN} = 4 \cdot 10^{-15} \cdot 2L_{MIN}^2 = 2fF$$
Propagation Delay in Static CMOS Family

\[ R_{PD} = \frac{L_1}{\mu_n C_{OX} W_1 (V_{DD} - V_{Tn})} \]

\[ R_{PU} = \frac{L_2}{\mu_p C_{OX} W_2 (V_{DD} + V_{TP})} \]

\[ C_{IN} = C_{OX} (W_1 L_1 + W_2 L_2) \]

If \( u_n C_{OX} = 100 \mu A V^{-2}, C_{OX} = 4 \text{ fF} \mu^{-2}, V_{Tn} = V_{DD}/5, V_{TP} = -V_{DD}/5, \mu_n/\mu_p = 3, L_1 = W_1 = L_{MIN}, L_2 = W_2 = L_{MIN}, L_{MIN} = 0.5 \mu \text{ and } V_{DD} = 5V \]

\[ R_{PD} = \frac{1}{10^{-4} \cdot 0.8 V_{DD}} = 2.5 K \Omega \]

\[ R_{PU} = \frac{1}{10^{-4} \cdot \frac{1}{3} \cdot 0.8 V_{DD}} = 7.5 K \Omega \]

\[ C_{IN} = 4 \cdot 10^{-15} \cdot 2 L_{MIN}^2 = 2 \text{ fF} \]
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

What is the transition time $t_{HL}$?
Propagation Delay in Static CMOS Family

\[ t_{HL} = R \text{DD} C_L \]

\[ t_{CH} = R \text{PD} C_L \]
Propagation Delay in Static CMOS Family

For HL output transition, $C_L$ charged to $V_{DD}$

$t_{HL} \approx R_{PD} C_L$

$t_{LH} \approx R_{PU} C_L$
Propagation Delay in Static CMOS Family

\[ t_{HL} = (5.5 \mu s)(2\pi f) \approx 5 \mu s \]

\[ t_{ LH} = (7.5 \mu s)(2\pi f) \approx 15 \mu s \]

\[ T_{clkn} = t_{HL} + t_{ LH} = 20 \mu s \approx 50 \text{GHz} \]
Propagation Delay in Static CMOS Family
Device Sizing

- Since not ratio logic, $V_H$ and $V_L$ are independent of device sizes for this inverter

- With $L_1=L_2=L_{\text{min}}$, there are 2 degrees of freedom ($W_1$ and $W_2$)

Sizing Strategies

- Minimum Size
- Fixed $V_{\text{TRIP}}$
- Equal rise-fall times (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
Device Sizing

- Minimum Size
  - $W_1 = W_2 = W_{\text{MIN}}$
  - Also provides minimum input capacitance
  - $t_{\text{LH}}$ is longer than $t_{\text{HL}}$

\[ V_{\text{IN}} = \frac{(0.2V_{\text{DD}}) + (V_{\text{DD}} - 0.2V_{\text{DD}})\sqrt{\frac{1}{3}}}{1 + \sqrt{\frac{1}{3}}} = .42V_{\text{DD}} \]
Device Sizing

Equal Rise-Fall Times

\[ t_{LH} = \frac{R_{PU} C_O X}{R_{PD} C_O X} \]

Thus if \( t_{HL} = t_{LH} \), must have

\[ \frac{W_2}{W_1} = \frac{\mu_n}{\mu_p} \]

What about the second degree of freedom?

\[ V_{TRIP} = \frac{V_{DD}}{2} \]
Device Sizing

Equal Rise-Fall Times

\[ t_{LH} = \frac{R_{PU}}{R_{PD}} C_{OX} = \frac{\mu_p}{\mu_n} \]

Thus if \( t_{HL} = t_{LH} \), must have

\[ \frac{W_2}{W_1} = \frac{\mu_n}{\mu_p} \]

\[
V_{IN} = \frac{(V_{Tn}) + (V_{DD} + V_{tp})}{1 + \sqrt[2]{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{0.2V_{DD} + 0.8V_{DD}}{2} = \frac{V_{DD}}{2}
\]
Device Sizing

Fixed $V_{TRIP}$

Set $V_{TRIP} = V_{DD}/2$

\[
\frac{(.2V_{DD}) + (V_{DD} - .2V_{DD})\sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}} = \frac{V_{DD}}{2}
\]

Solving, obtain $W_2/W_1 = \mu_n/\mu_p$
Device Sizing

Sizing Strategies

- Minimum Size
- Fixed $V_{TRIP} = \frac{3}{8}V_{DD}$
- Equal rise-fall times (equal worst-case rise and fall times)
- Minimum power dissipation
- Minimum time required to drive a given load
- Minimum input capacitance
for min sized
\[ t_{HL} = k R_{pd} C_L = k t_{HL,ret} \quad \text{and} \quad t_{OH} = 3 k R_{pd} \]

\[ FI = 2 \cos \theta \tan \theta \frac{L_{oh}}{2} = \frac{C_{AE}}{2} \]

for equal work-coned nose & half

\[ W_n = (w_{min}) k \]
\[ W_p = 3 w_{min} \]

\[ E_{min} + I = 2 \cos \theta (w_{min} L_{oh} + 3 \cos \theta w_{min} h_{oh}) = (3+k)(\cos \theta w_{min} h_{oh}) \]
\[ = \frac{3+k}{k} C_{AE} \]

\[ u_0 \]
To Inverter with \( t_{\text{in}} + t_{\text{out}} \)

all devices as small as possible

\( W_0 = \text{water}, \ W_2 = 3 \ \text{water}, \ L_1 = L_2 = L_4 \)

called Ref. Inverter

\( t_{\text{in}} = \frac{3k+1}{4} \text{C.R.E.F.} \)

\( t_{\text{out}} = \frac{kR_{\text{pu}} C_L}{k} = R_{\text{pu}} C_L \)

\( R_{\text{pu}} = \frac{R_{\text{ld}}}{k} \)

\( R_{\text{pu}} = \frac{mn R_{\text{po}}}{m^2} = \frac{3k+1}{4} \text{C.R.E.F.} \)

\( L_2 = \text{inlet} \)}
Sizing multiple-input gates

\[ K \frac{M_y}{M_D} = 3 \]

- Minimum
- Equal wires full (worst case)

\[ t_{HL} = \begin{cases} \frac{R_{PD}}{C_L} & \text{for 1 input} \\ \frac{R_{PD}}{C_L} \frac{R_{PD}}{C_L} \frac{R_{PD}}{C_L} \cdots \frac{R_{PD}}{C_L} & \text{for 2 inputs} \\ \sqrt[4]{\frac{R_{PD}}{C_L}} \cdots \sqrt[4]{\frac{R_{PD}}{C_L}} & \text{for all } k \text{ inputs} \end{cases} \]

\[ L_1 = L_2 = L_{in} \]

\[ w_1 = w_2 = \text{min} \]

will turn on if all inputs are \( V_{dd} \)

prior to clock 1, 2, ..., \( k \) go high

at clock

\[ t_{HL} = k \frac{R_{PD}}{C_L} = 3k \frac{R_{PD}}{C_L} \]

Fan In on each input = \( C_{in}w_1l_1 + C_{in}w_2l_2 = 2C_{in}w_{min} \text{ min} \)