EE 434

Lecture 40

- Power Dissipation
- Other logic design styles

Review:

4 types of power dissipation

1) Static
2) Dynamic
3) Pipe
4) Leakage

Dynamic !

$$P = \Theta f_{CL} C_L V_{DD}^2$$

Example:

How much power required by last inverter driving a 32-bit bus off chip if $\Theta = .5$

Assume $V_{DD} = 5v$, $f_{CL} = 10G$, $C_L = 5pf$

$$P = \left(\frac{1}{2}\right) 10^{10} (5E-12)(5v)^2 32 = 20w$$

If $V_{DD} = 1v$

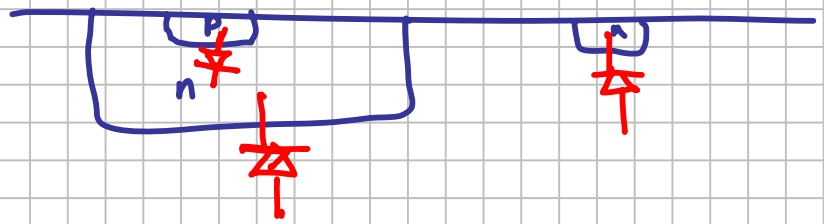
$P = 800mw$

Power required to drive off-chip loads fast is very high!

- maybe can use lower-level signaling - avoid going off chip
- adiabatic methods ?

Leakage Power

- diffusion leakage (reverse-biased pn junction)



$I_G = 0$

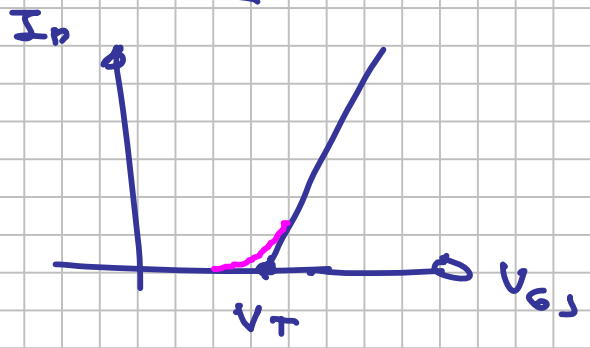
- Channel Leakage: subthreshold current in I_D when $V_{GS} << V_T$

$$I_D = \begin{cases} 0 \\ \vdots \end{cases}$$

$V_{GS} < V_T$

$V_{GS} > V_T$

- Gate Leakage V_{GS}



$$I_D = k e^{\frac{V_{GS} - V_T}{a}}$$

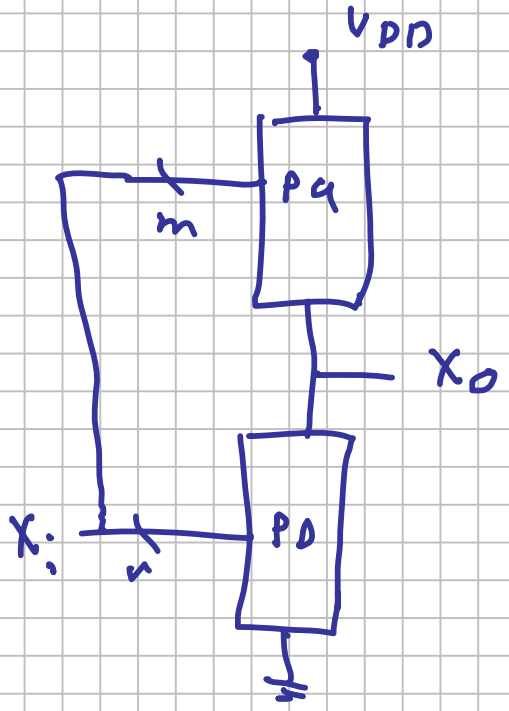
If $V_{GS} < V_T + 100\,mV$

operate in weak inversion / subthreshold

Other Types of Logic

- Complex Logic Gates
- Pass Transistor Logic
- Pseudo NMOS
- Dynamic Logic

Observation:

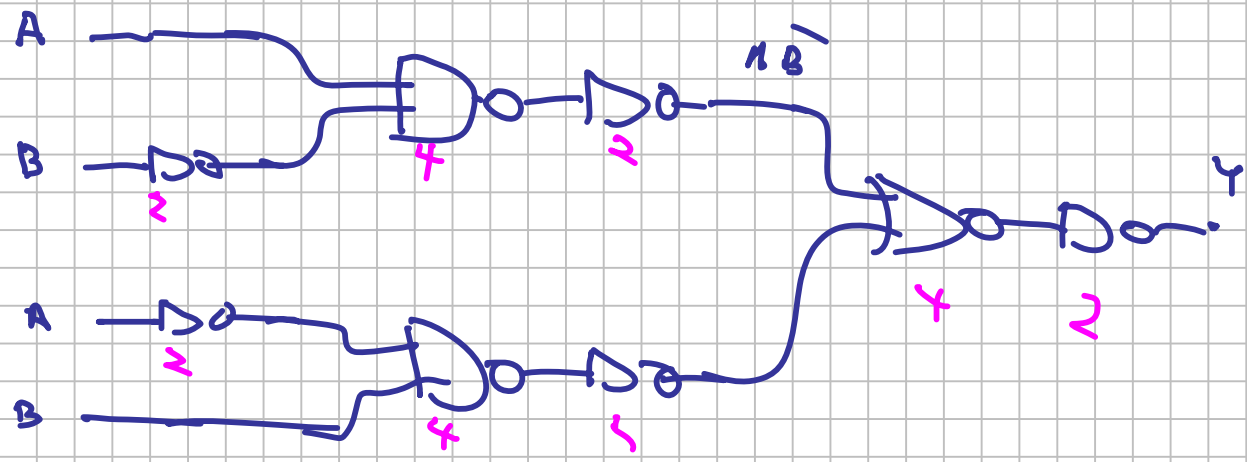


Only one of the {PU, PD} is ever conduct at same time!

(provides zero static power dissipation)

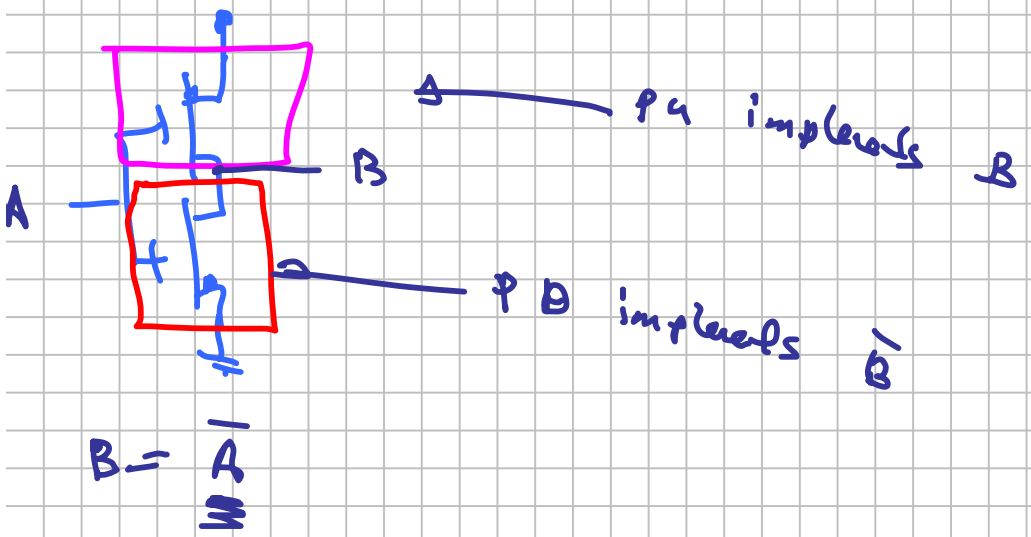
Ex: $Y = A \oplus B$

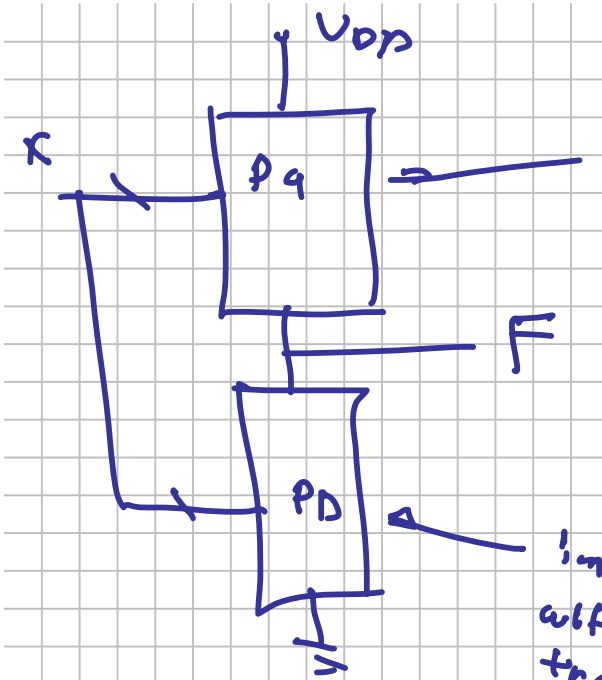
$= A\bar{B} + \bar{A}B$



5 levels of logic

22 transistors


A
B
PA implants B
PB implants B'
B = A'



$A \oplus B = \bar{A}B + A\bar{B}$

Ex:

$$F = A \oplus B = A\bar{B} + \bar{A}B$$

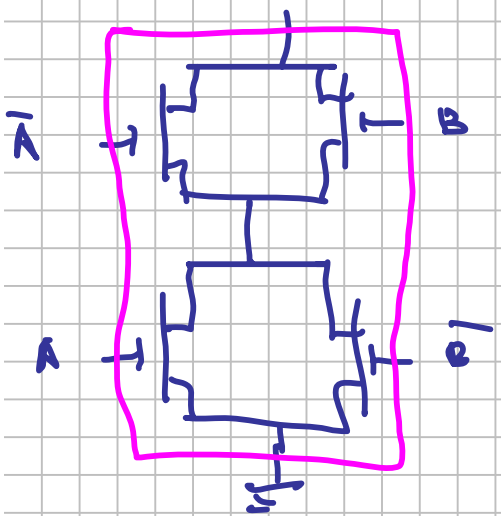
$$\bar{F} = \overline{A\bar{B} + \bar{A}B}$$

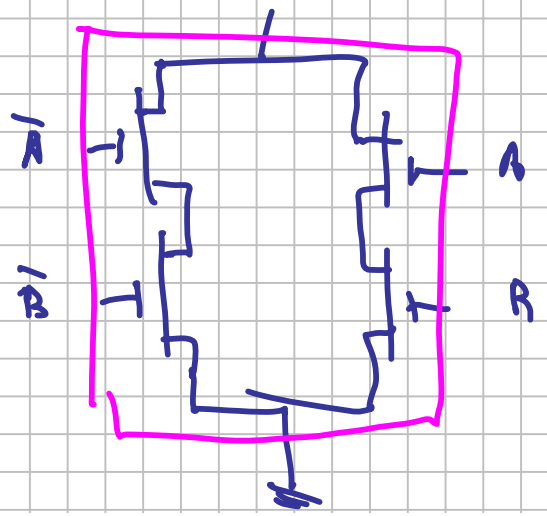
$$= \overline{A\bar{B}} \cdot \overline{\bar{A}B}$$

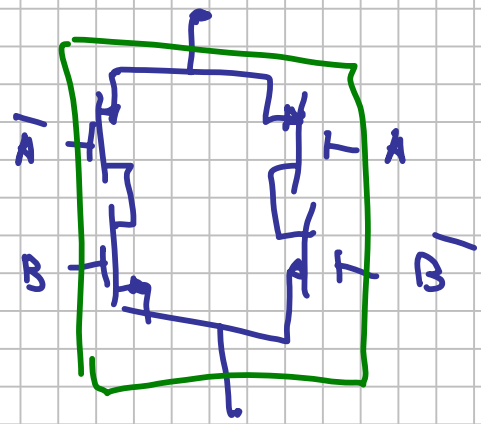
$$= (\bar{A} + B)\cdot(A + \bar{B})$$

$$= \bar{A}A + \bar{A}\bar{B} + BA + B\bar{B}$$

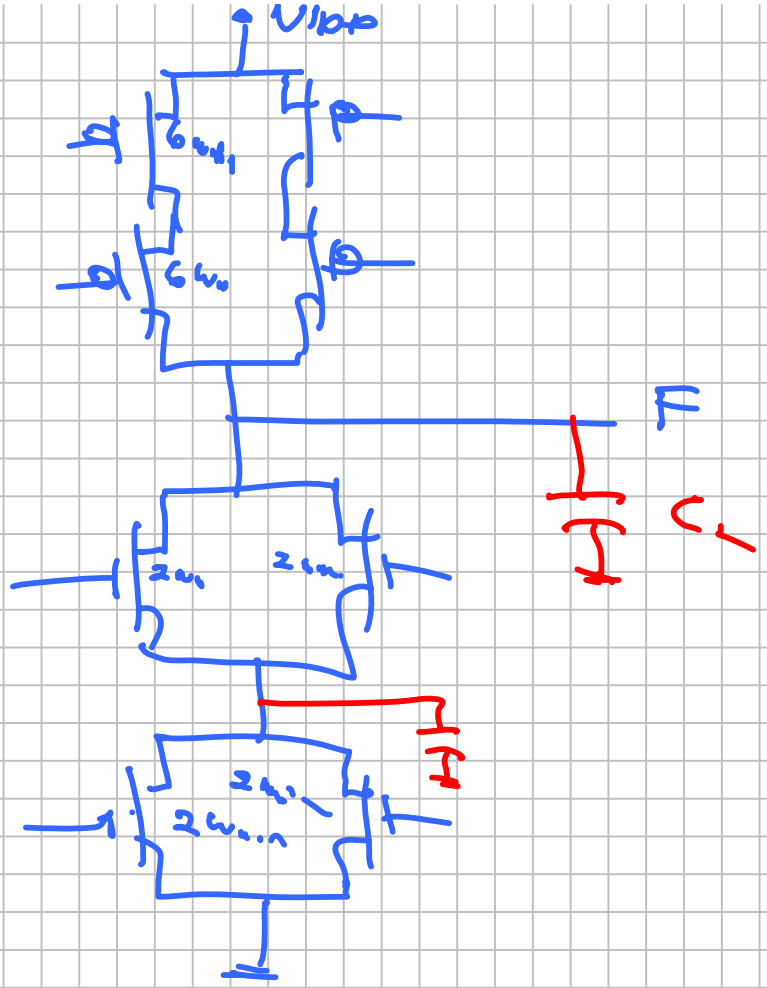
$$= \bar{A}\bar{B} + BA$$







transistors 12
2 levels of logic



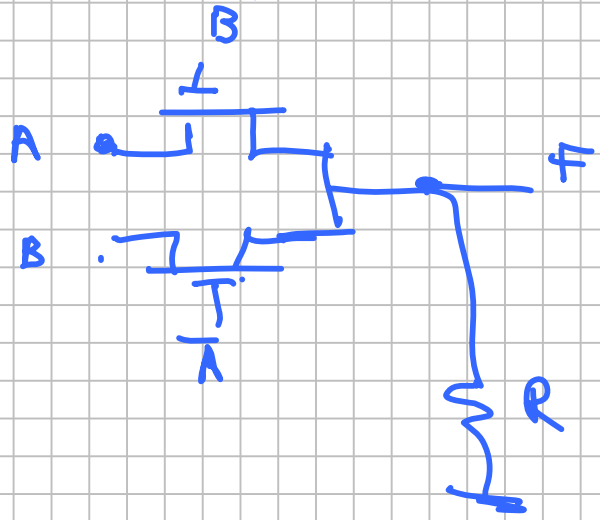
- sizing
- delay

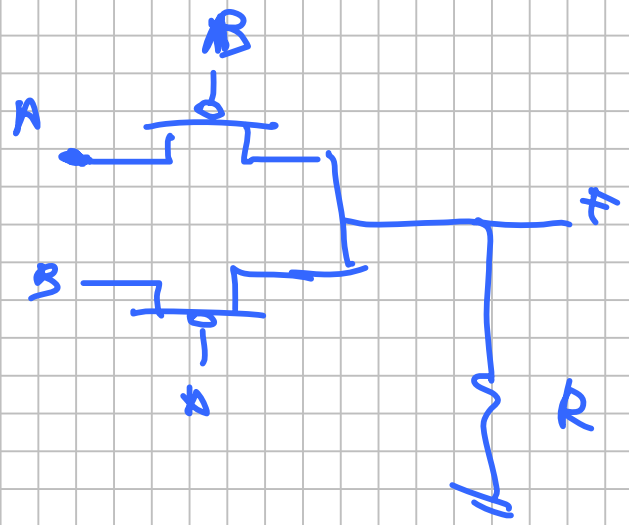
(Elmore delay mostly useful for pencil+paper

— were present in static CMOS gates as well, just not discussed

Pass Transistor Logic

$F = A\bar{B} + \bar{A}B$

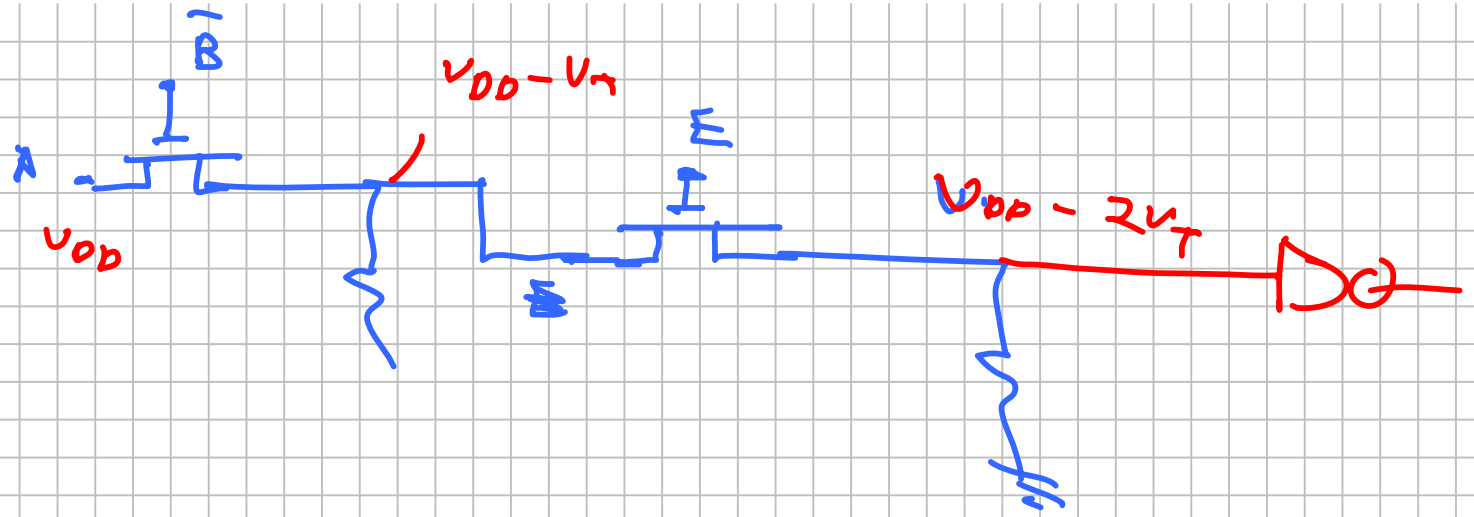




6 transistors:
1 resistor

2 transistors
1 resistor

- static power disc is not 0
- signal levels degrad
  (e.g. in first ckt, $V_{OH} < V_{DD} - V_T$



- signal degradation can occur
- can restore with static CMOS before too much degradation