

# EE 434

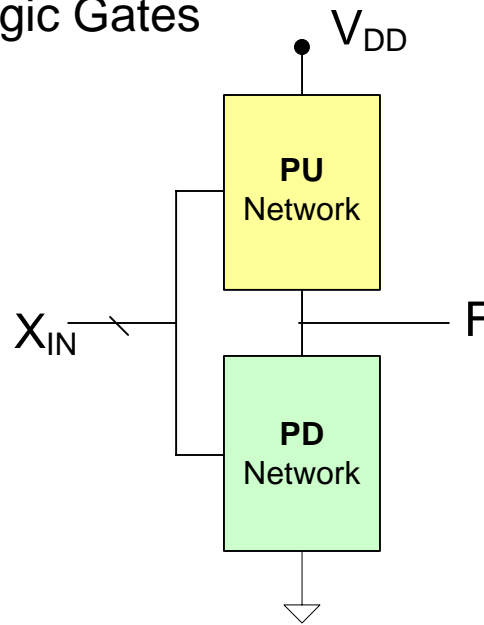
## Lecture 42

### Other Logic Styles

- Static CMOS Logic
- Complex Logic Gates
- Pass Transistor Logic
- Pseudo-NMOS
- Dynamic Logic

## Review from last time

### Complex Logic Gates



Implement  $\bar{F}$  in PD Network with n-channel devices

Implement  $F$  in PU Network with p-channel devices with complimented variables

Preserves rail-to-rail signal swing

No static power dissipation

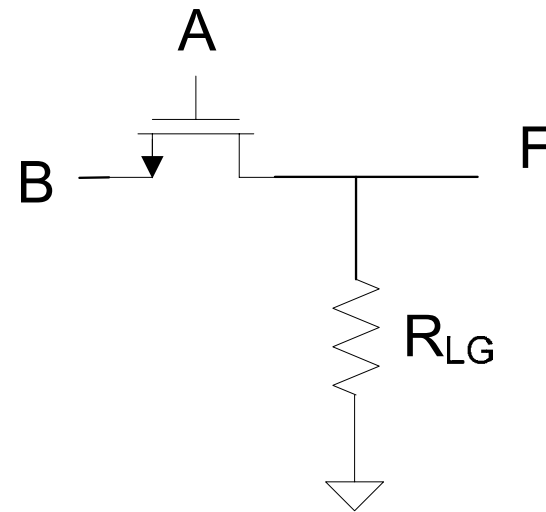
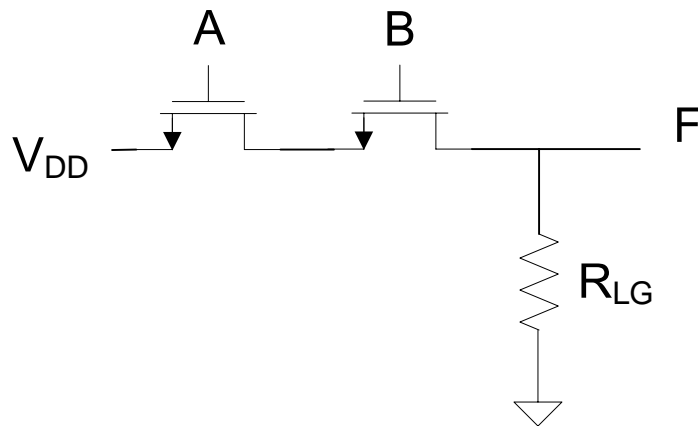
At most two levels of logic

Often significant reduction in device count and delay

## Review from last time

### Pass Transistor Logic

Example:



$$F=A \cdot B$$

Low device count implementation of non inverting function (can be dramatic)

Logic Swing not rail to rail

Static power dissipation not 0 when F high

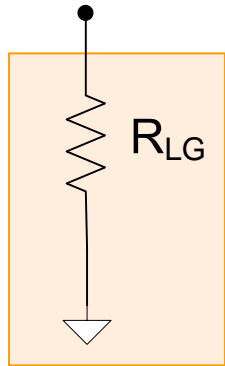
$R_{LG}$  may be unacceptably large

Slow  $t_{LH}$

Signal degradation can occur when multiple levels of logic are used

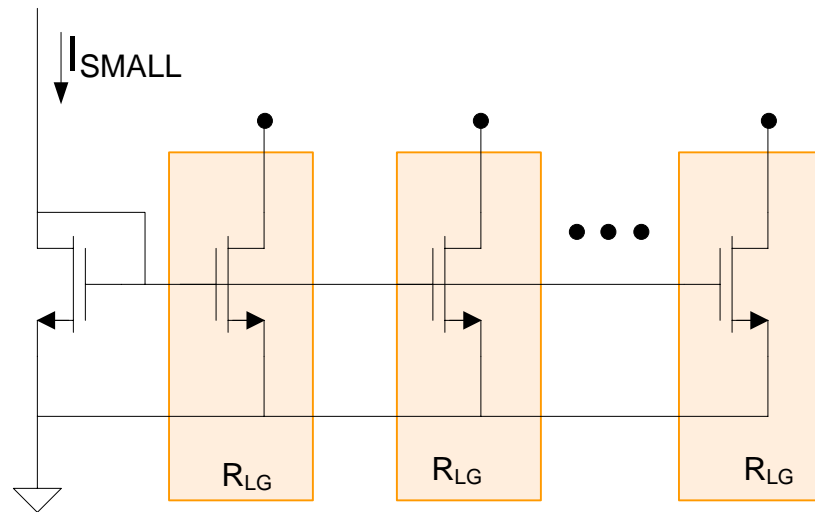
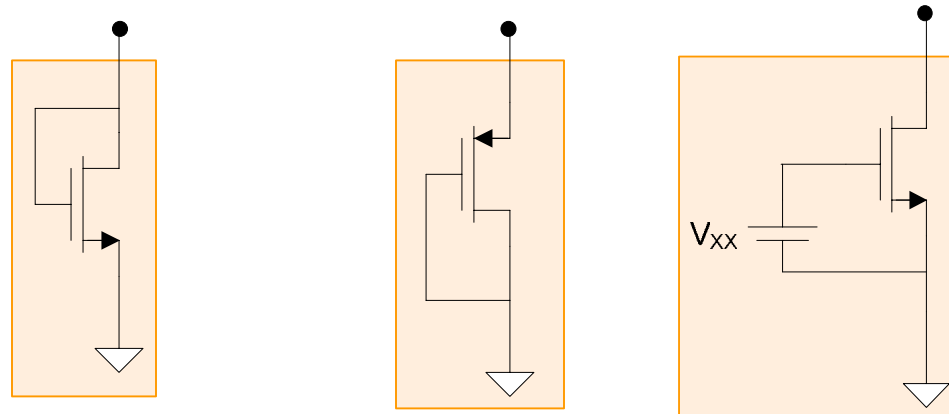
Review from last time

# Pass Transistor Logic



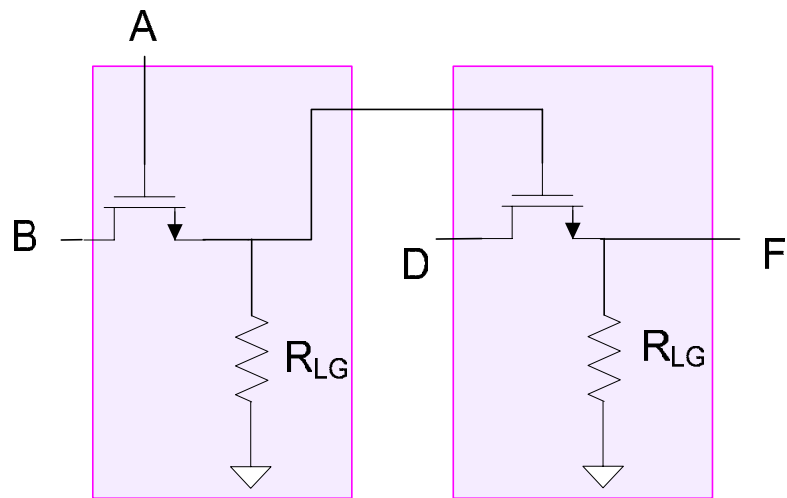
Physical Size of  $R_{LG}$  too large

Methods of implementing  $R_{LG}$

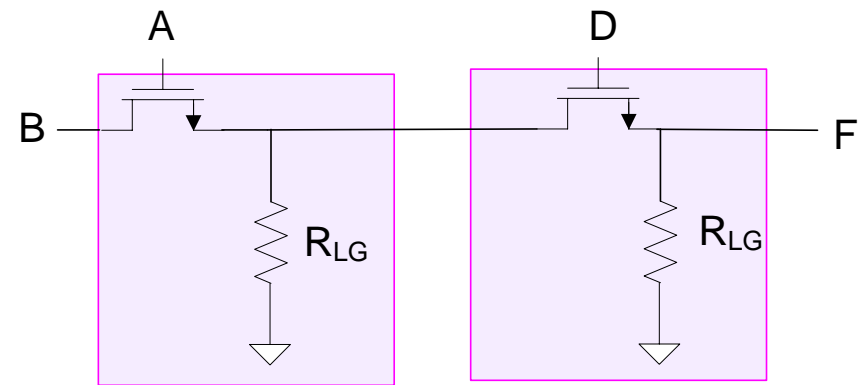


## Review from last time

### Pass Transistor Logic



Signal degradation



No signal degradation

Signal degradation may occur with PTL

- Can intermix n-channel and p-channel devices to reduce/eliminate the signal degradation problem
- Can add static CMOS buffers to restore signals provided too much signal degradation has not occurred

## Other Logic Styles

Static CMOS Logic

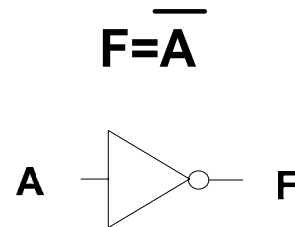
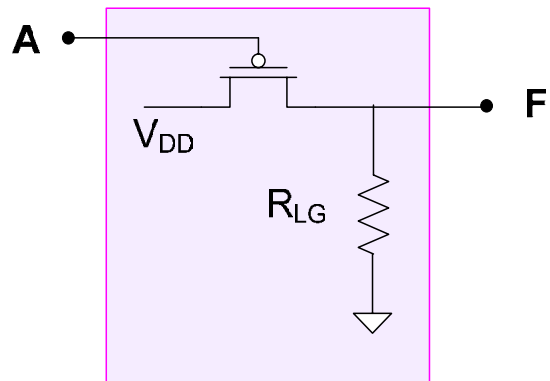
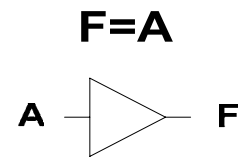
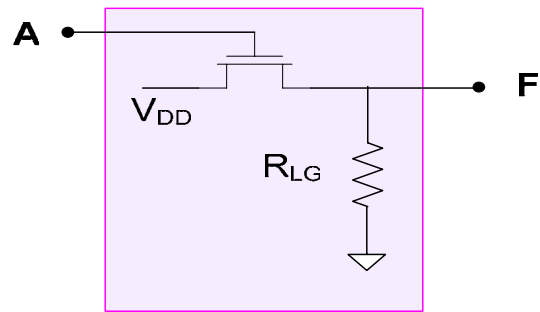
Complex Logic Gates

 Pass Transistor Logic

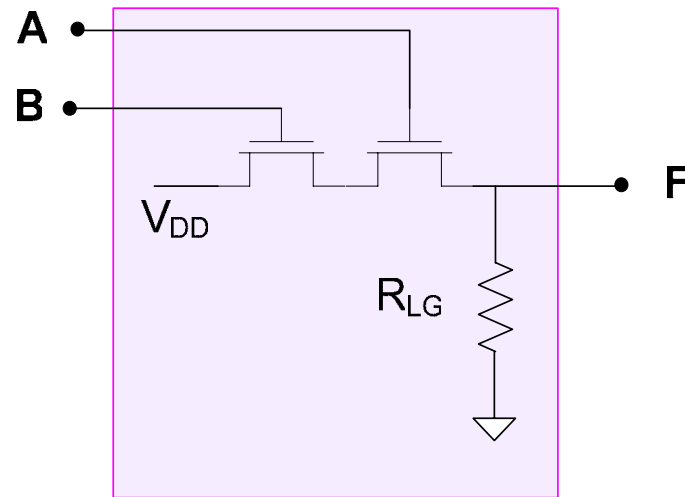
Pseudo-NMOS

Dynamic Logic

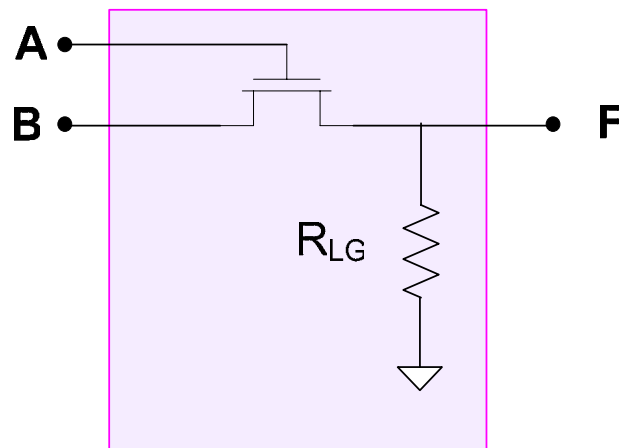
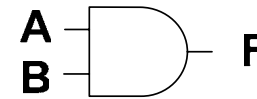
# Pass Transistor Logic Gates



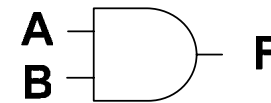
# Pass Transistor Logic Gates



$$F = A \cdot B$$

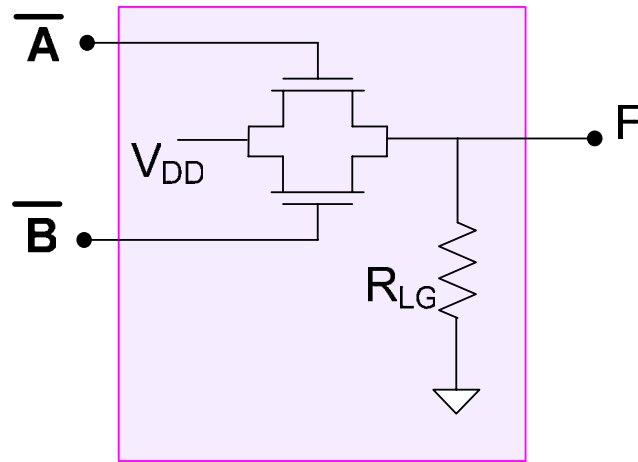


$$F = A \cdot B$$

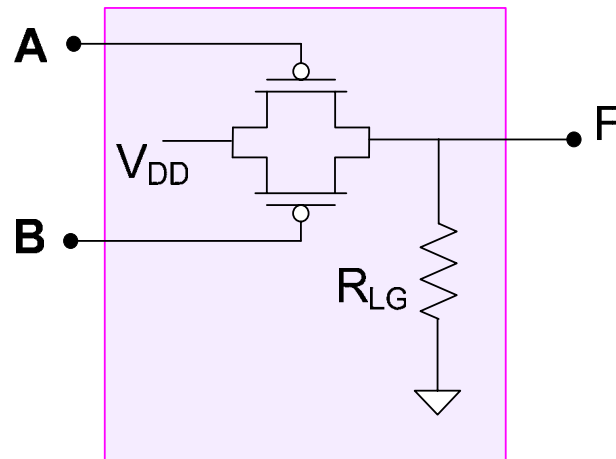
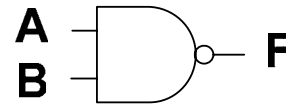




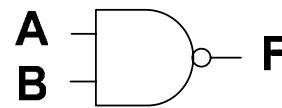
# Pass Transistor Logic Gates



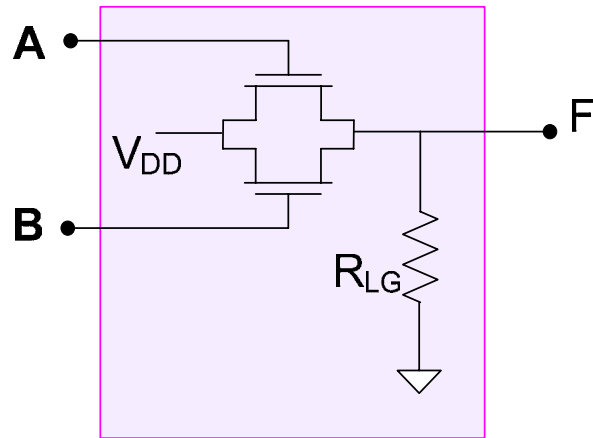
$$F = \overline{A \cdot B}$$



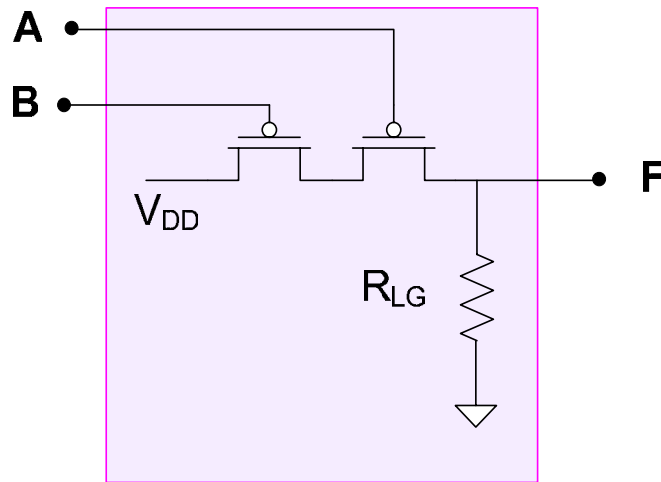
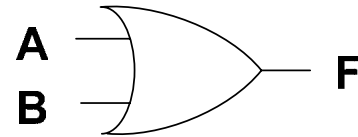
$$F = \overline{A + B}$$



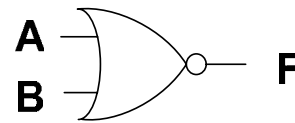
# Pass Transistor Logic Gates



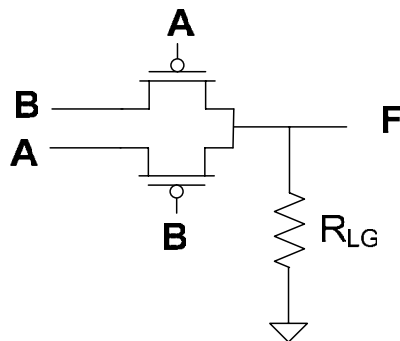
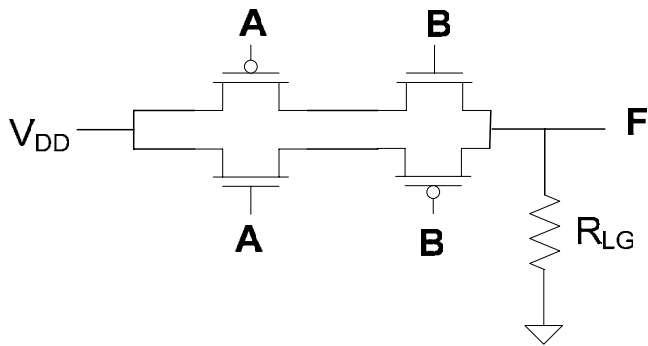
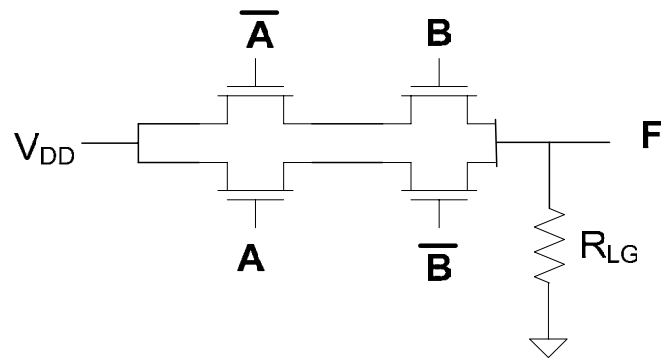
$$F = A + B$$



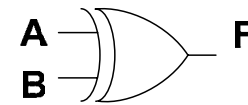
$$F = \overline{A + B}$$



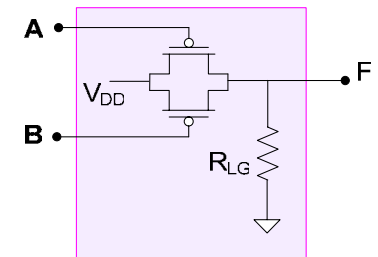
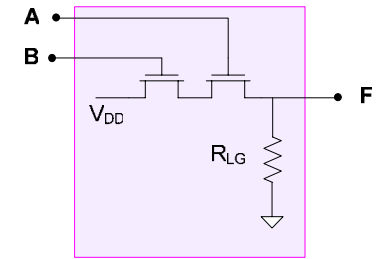
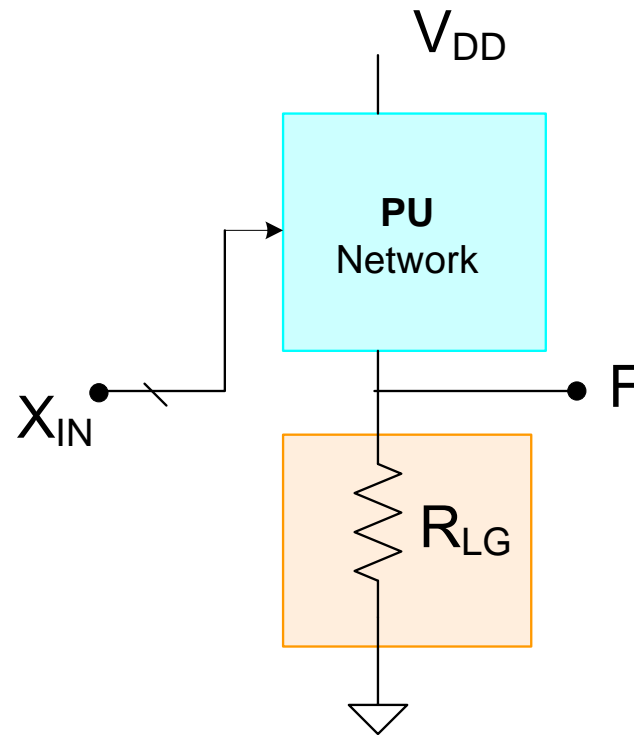
# Pass Transistor Logic Gates



$$F = A \oplus B$$

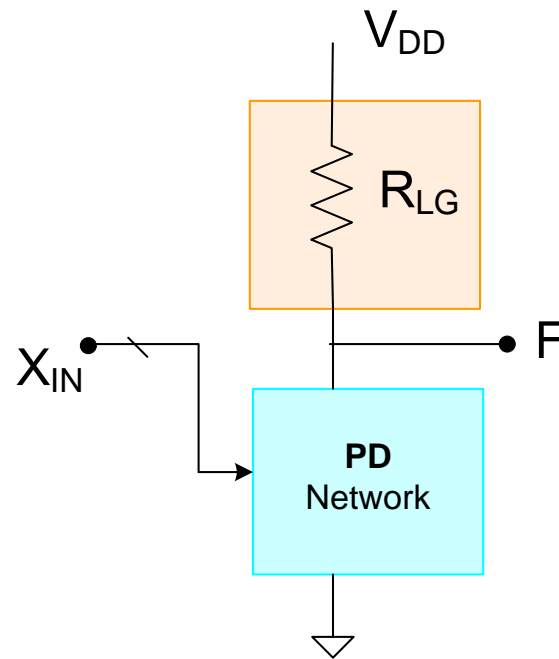


# Pass Transistor Logic Gates



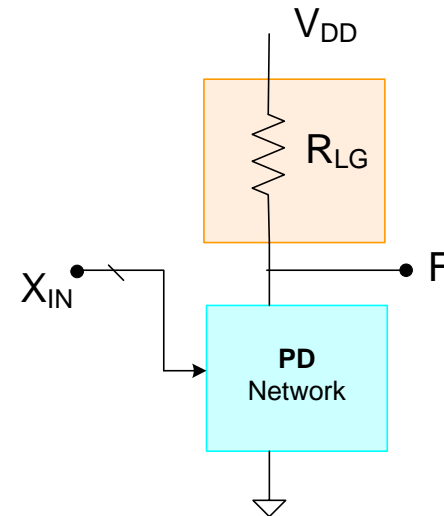
- Observe all PTL gates discussed so far were of this form
- PU network can contain a mixture of n-channel and p-channel devices
- Any of the PU networks used for complex logic gates could also be used in PTL

# Pass Transistor Logic Gates

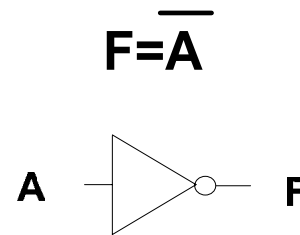
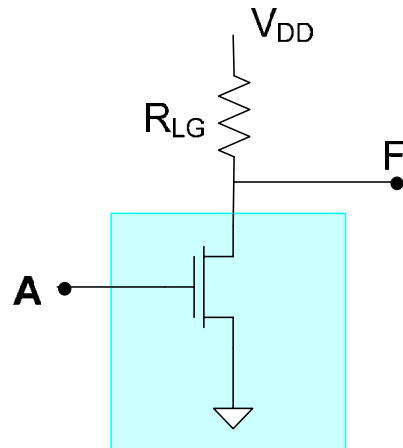


- PTL gates could also be designed with logic in PD network
- PD network can contain a mixture of n-channel and p-channel devices
- Any of the PD networks used in complex logic gates could be used in PTL

# Pass Transistor Logic Gates



As an example:



## Other Logic Styles

Static CMOS Logic

Complex Logic Gates

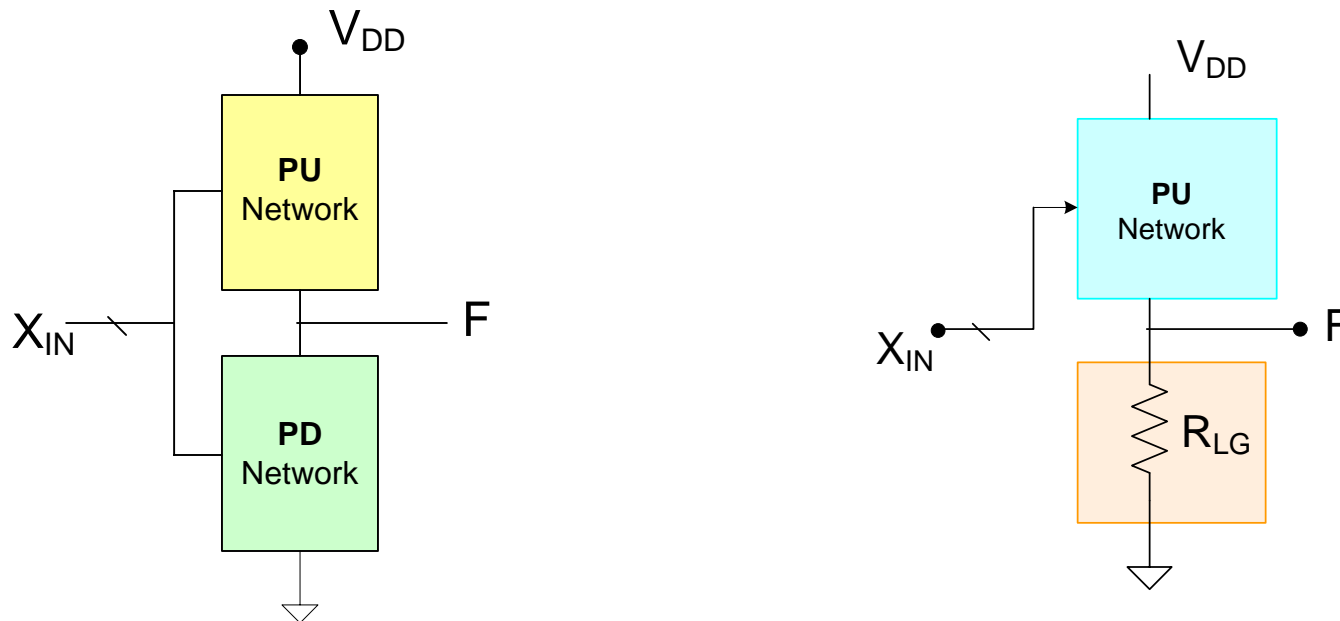
Pass Transistor Logic

Pseudo-NMOS



Dynamic Logic

# Dynamic Logic

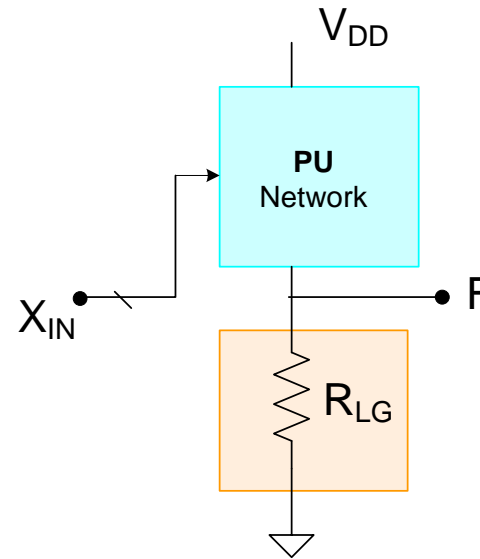
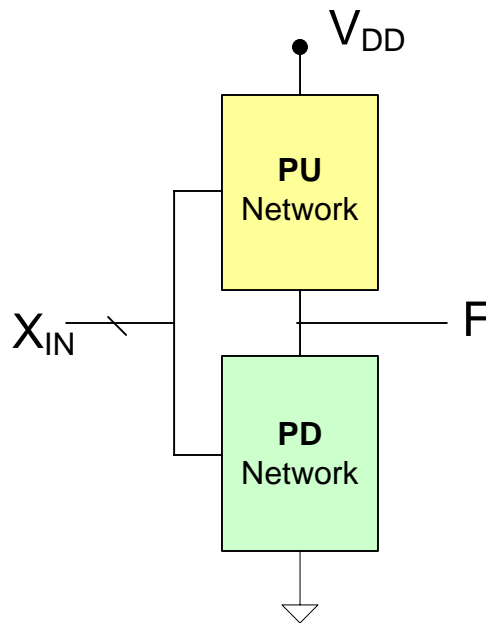


Observations:

- PU network major contributor to dynamic power dissipation
- PU network for complex logic gates requires large devices for good  $t_{LH}$
- PU network requires large area for n-wells
- PU and PD network duplicate logic function



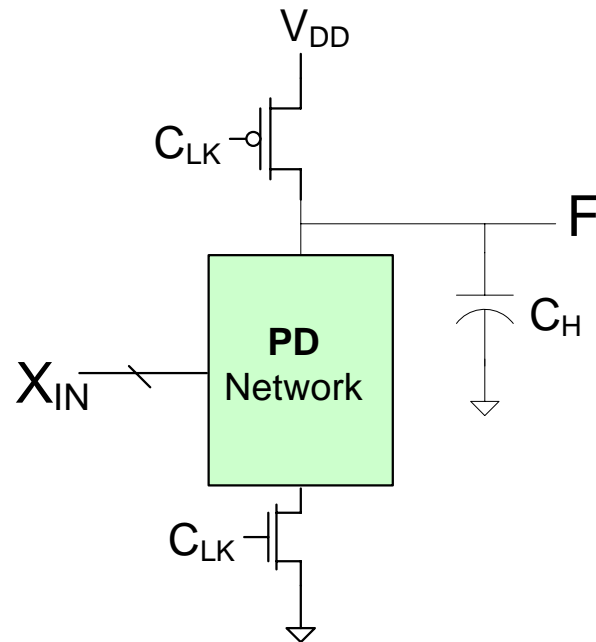
# Dynamic Logic



Question:

Is it possible to eliminate PU Network and still maintain signal swing and zero static power dissipation of complex logic gate approaches?

# Dynamic Logic



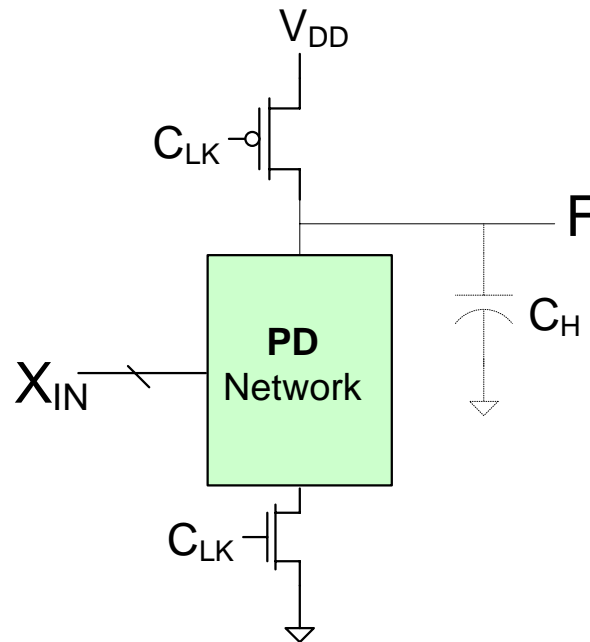
Basic Dynamic Logic Gate

Precharges F to  $V_{DD}$  when  $C_{LK}$  is low (precharge state)

when  $C_{LK}$  is high (evaluate state) discharges  $C_H$  only if PD network conducts

$C_H$  (hold capacitor) can be simply parasitic capacitances on node F

# Dynamic Logic

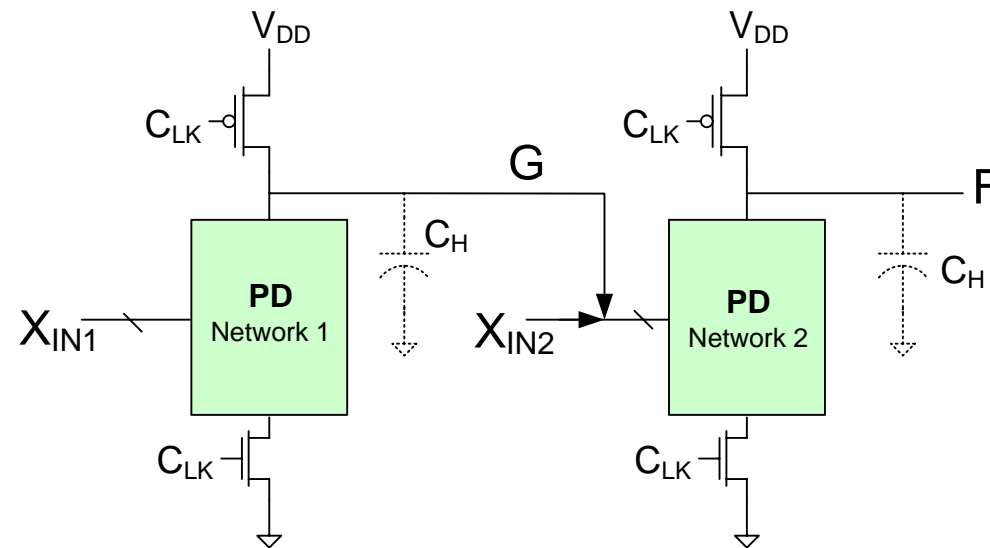


Basic Dynamic Logic Gate

## Positive Attributes:

- Potential for substantial decrease in dynamic power dissipation
- Zero Static Power Dissipation
- Excellent speed
- Reduced area

# Dynamic Logic

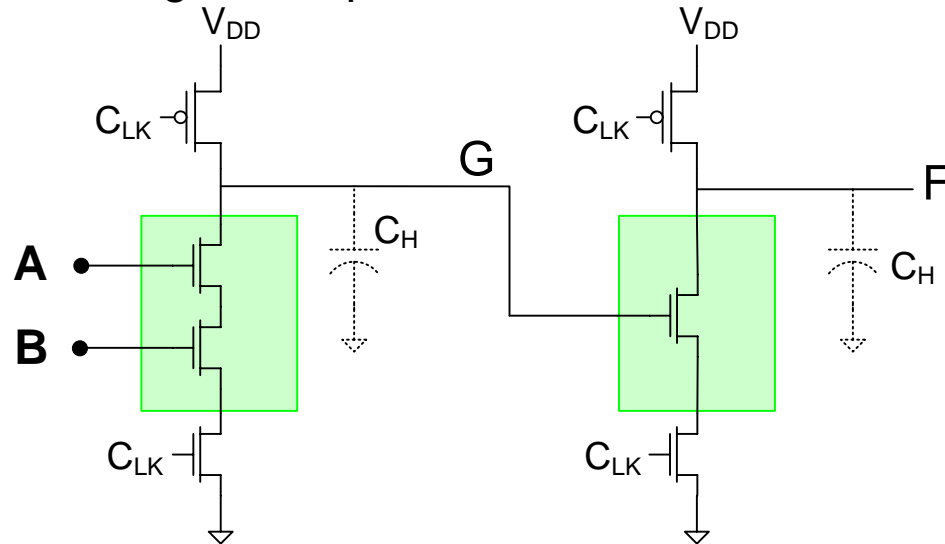


## Negative Attributes:

- Output valid only during evaluate state
- Requires Clock
- Can not be placed in a static hold state
- Premature discharge can occur with cascaded logic (potential stopper !)

# Dynamic Logic

Premature discharge example:



When G is precharged high and is to go Low (A=B=1) on the evaluate state F should be a 1 but may be prematurely discharged while G is high

Alternatively, if A or B are to be 1 but come from another gate where they were low initially, there may be a delay for becoming 1 thus keeping G high even longer thus prematurely discharging F