EE 434
Lecture 5

Improved Device Model

Stick Diagrams

Technology Files

Quiz 3

How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{B}} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

And the number is ….

1 8 7 5 3

6 9 4 2

9

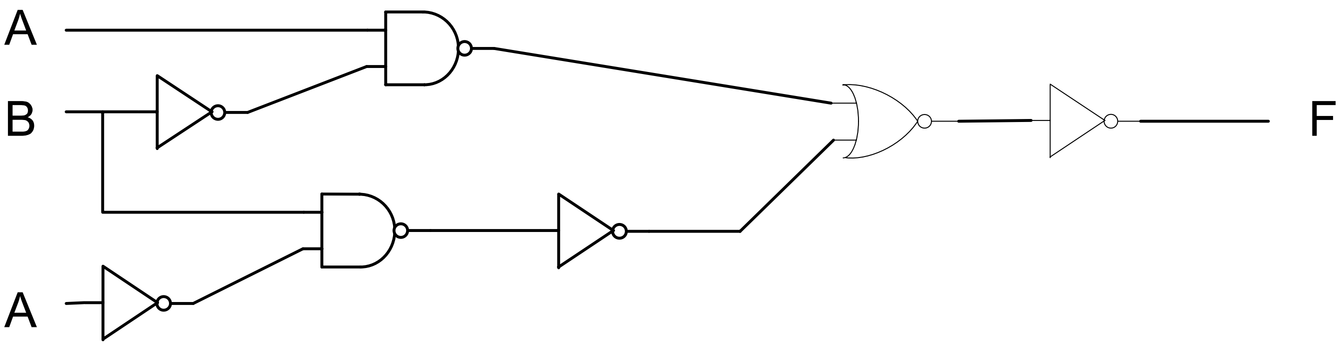
Quiz 3

How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{B}} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution:



20 transistors and 5 levels of logic

Quiz 3

How many transistors are required to realize the function

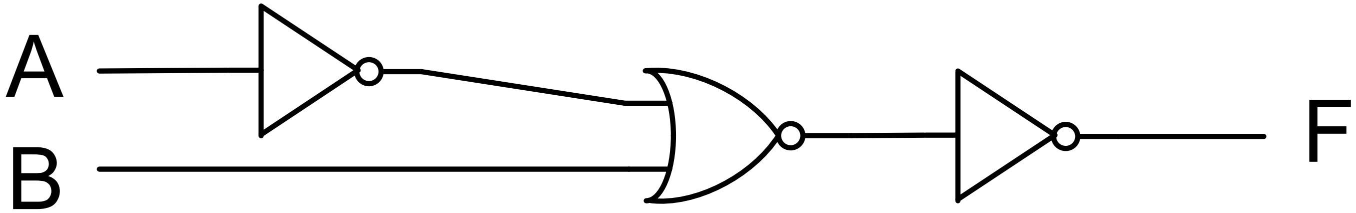
$$F = \overline{A \bullet \overline{B}} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative): From basic Boolean Manipulations

$$F = \overline{A} + \overline{\overline{B}} + \overline{A} \bullet C = \overline{A} + B + \overline{A} \bullet C$$

$$F = \overline{A} \bullet (1 + C) + B = \overline{A} + B$$



8 transistors and 3 levels of logic

Quiz 3

How many transistors are required to realize the function

$$F = \overline{A \bullet \overline{B}} + \overline{A} \bullet C$$

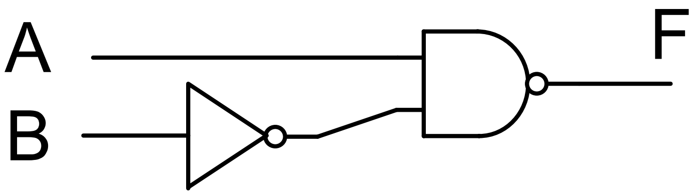
in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):

From basic Boolean Manipulations

$$F = \overline{A} \bullet (1 + C) + B = \overline{A} + B$$

$$F = \overline{\overline{\overline{A} + B}} = \overline{A \bullet \overline{B}}$$



6 transistors and 2 levels of logic

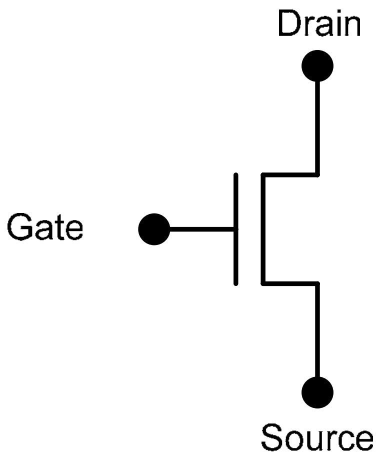
Review from Last Time

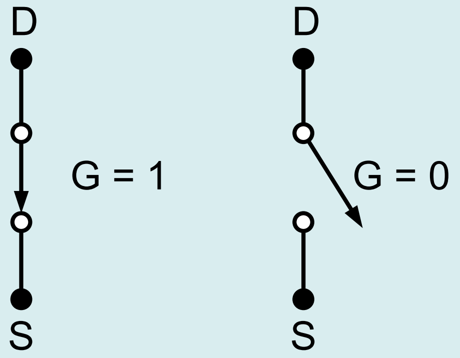
- Simple model of MOSFET was developed
  - hierarchical model structure will be developed
  - generally use simplest model that can be justified
- Simple CMOS gates were introduced
  - Zero power dissipation
  - Rail to Rail Swings
  - Infinitely Fast
  - Simple model may not give sufficiently accurate insight relating to these properties

Review from Last Time

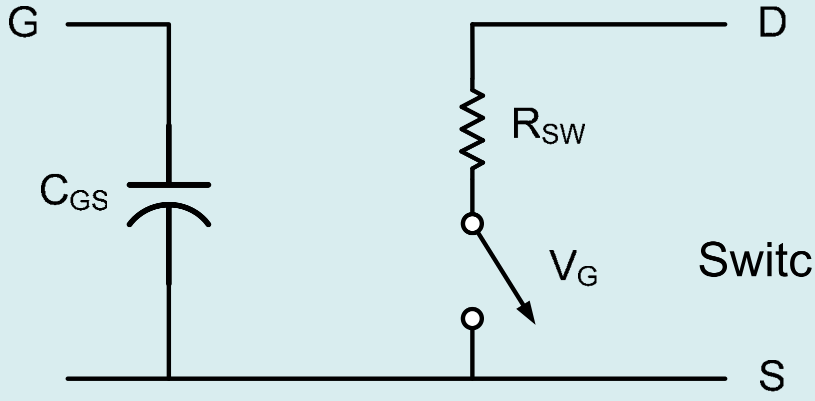
- Different Logic Design Styles Often Used on an Integrated Circuit
  - PTL is one style that can offer significant reductions in complexity
  - Signal Degradation and Static Power Dissipation are issues of concern when using PTL
  - Designer is under complete control of circuits that are placed on the silicon
  - Many designs will mix multiple logic design styles
  - New logic design styles are still being proposed and adopted

Improved Switch-Level Model





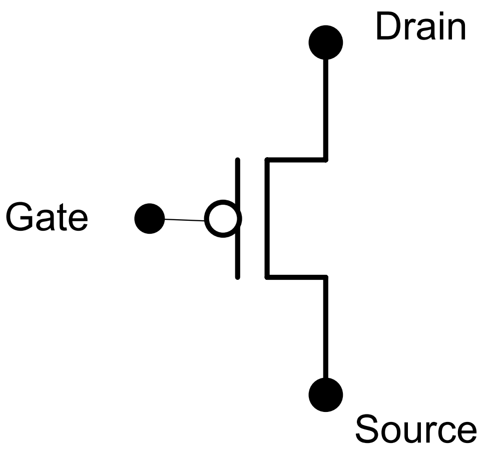
Switch-level model

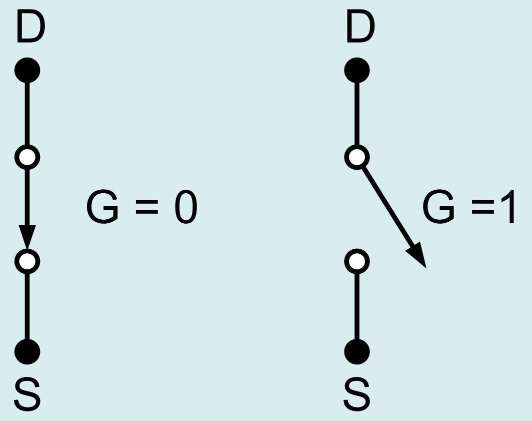


Switch closed for V_G=1

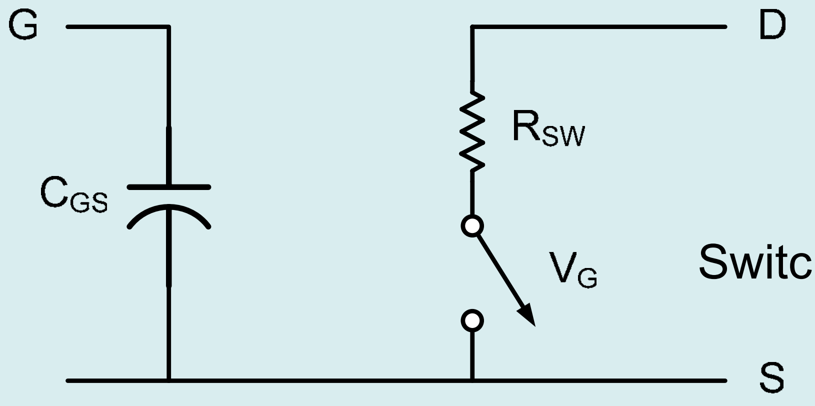
Switch-level model including gate capacitance and drain resistance

Improved Switch-Level Model





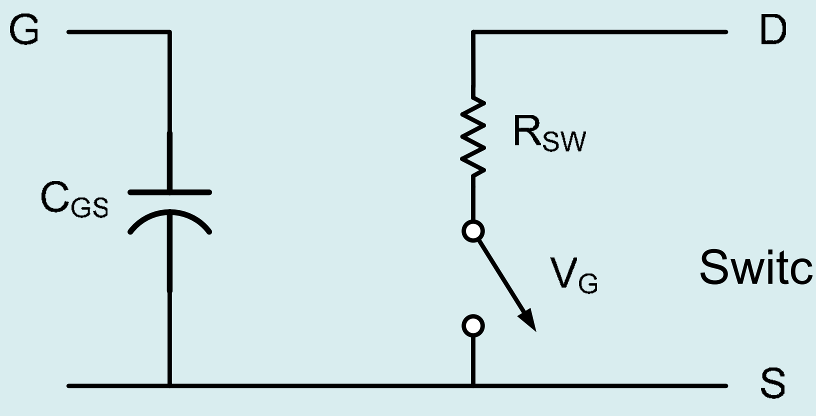
Switch-level model



Switch closed for V_G=0

Switch-level model including gate capacitance and drain resistance

Improved Switch-Level Model



Switch closed for V_G=0

Switch-level model including gate capacitance and drain resistance

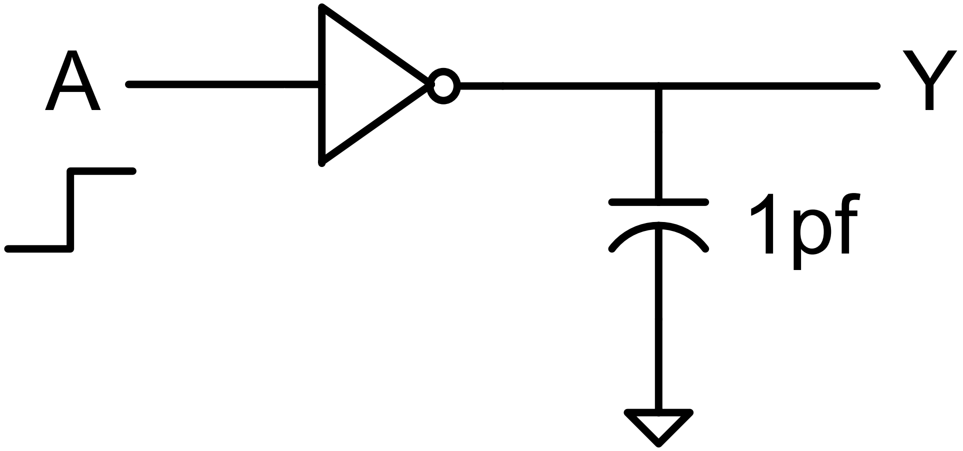
C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

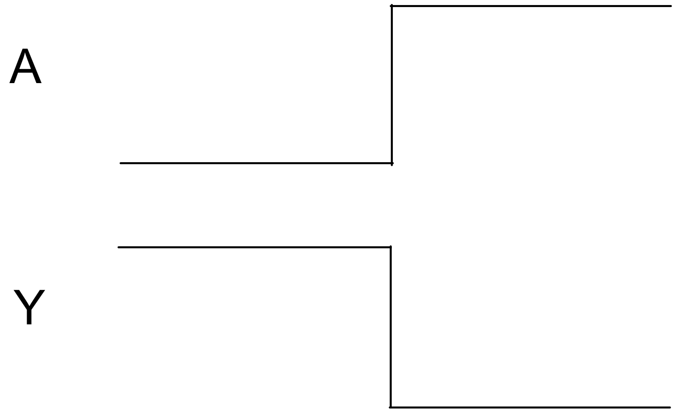
$$\mathbf{C_{GS} \cong 1.5fF} \qquad \mathbf{R_{sw} \cong \left.\begin{matrix} 2K\Omega \;\; n-channel \\ 6K\Omega \;\; p-channel \end{matrix}\right\}}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

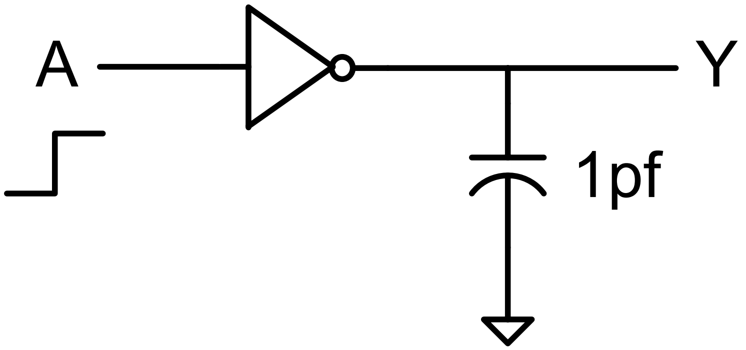
Example



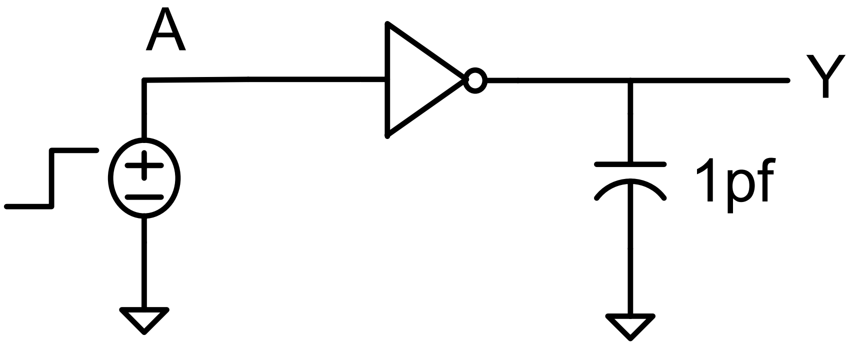
With switch level model



Example (cont)

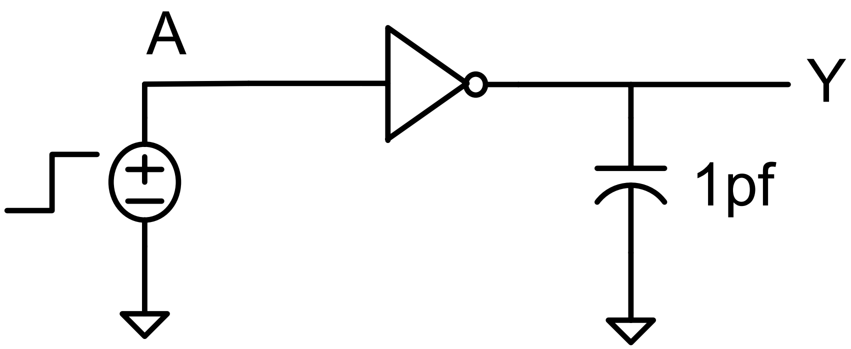


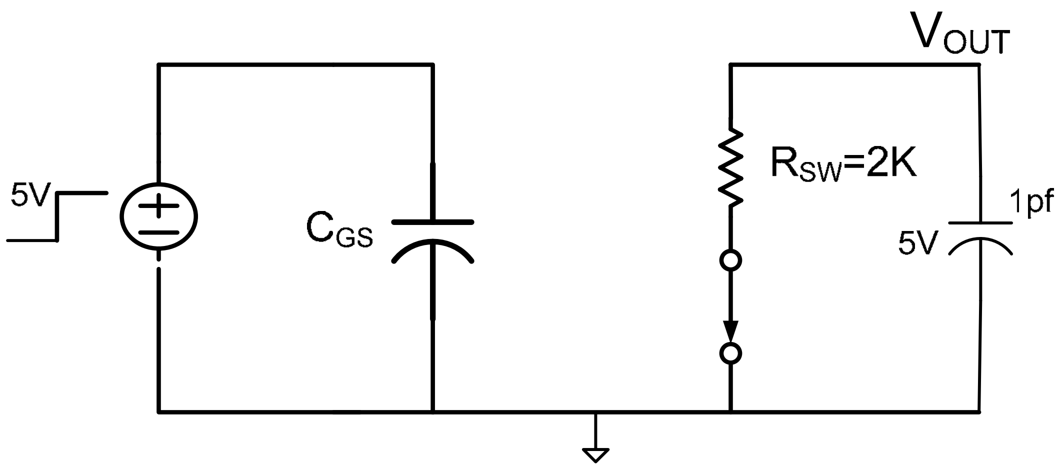
With improved model



Example (cont)

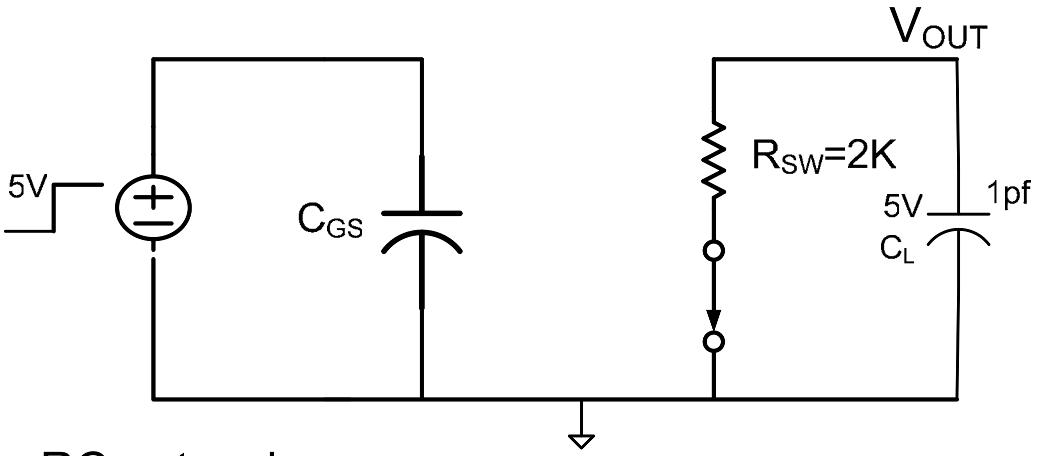
With improved model





Example (cont)

With improved model



Recognize as a first-order RC network

Recall: Step response of any first-order network with LHP pole can be written as

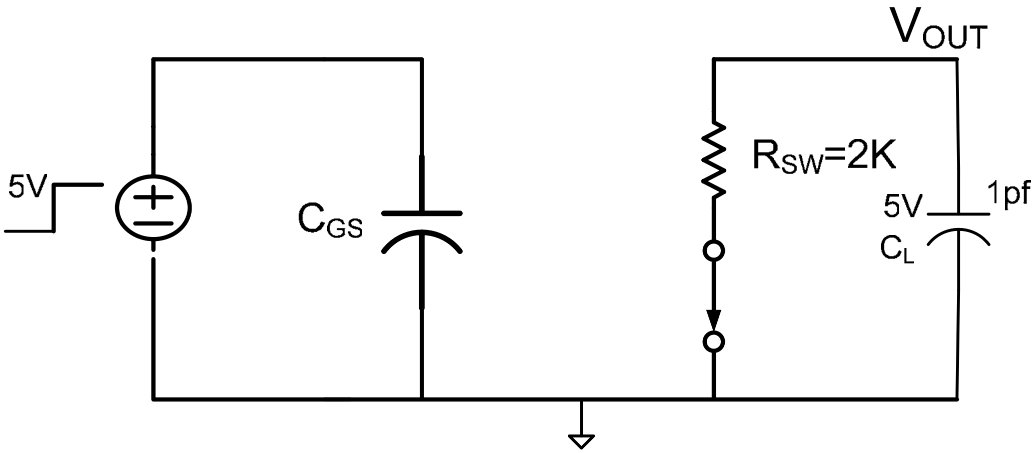
$$y(t) = F + (I - F)e^{-\frac{t}{\tau}}$$

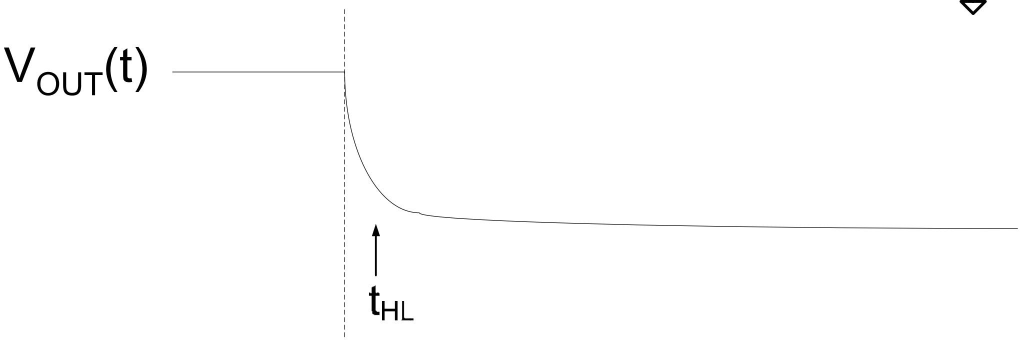
where F is the final value, I is the initial value and τ is the time constant of the circuit

For the circuit above, F=0, I=5 and $\tau = R_{SW}C_L$

Example (cont)

With improved model





$$t_{HL} \cong \frac{1}{R_{SW}C_L} \quad = \frac{1}{2K \bullet 1pF} = .5E - 9\sec = .5n\sec$$

Stick Diagrams

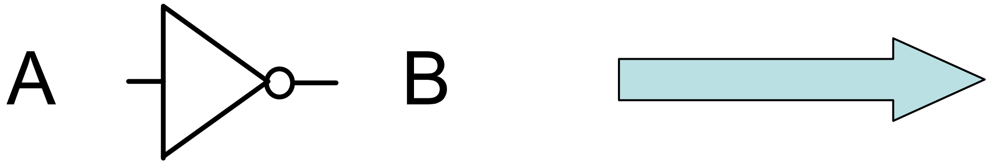
- It is often necessary to obtain information about placement, interconnect and physical-layer structure
- Stick diagrams are often used for small component-count blocks
- Approximate placement, routing, and area information can be obtained rather quickly with the use of stick diagrams

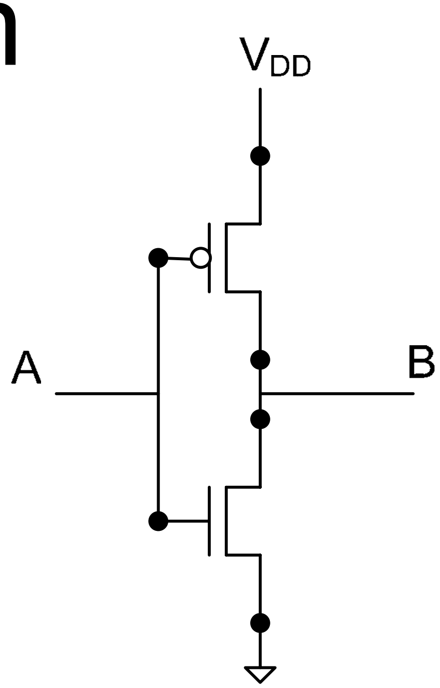
Stick Diagrams

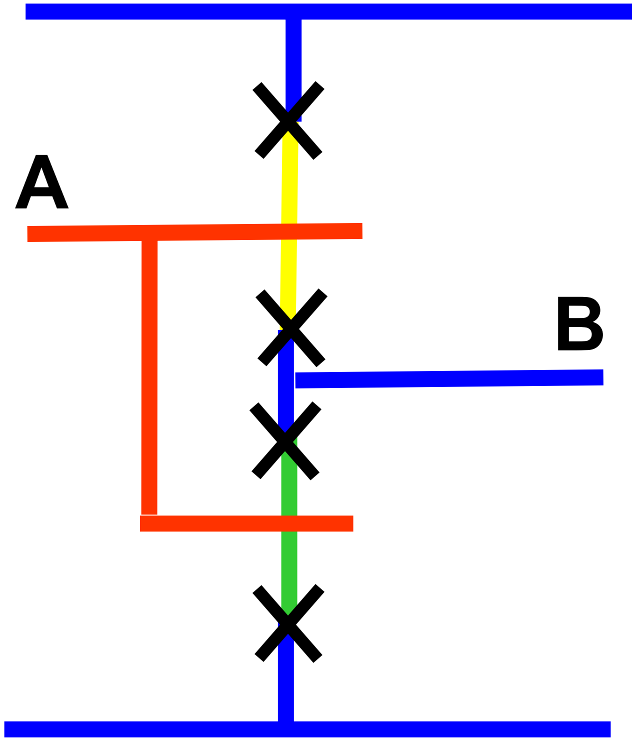
🟦	Metal 1
🟥	poly
🟩	n-diffusion
🟨	p-diffusion
🟪	Metal 2
✕	Contact

Additional layers can be added and color conventions are peronal

Stick Diagram





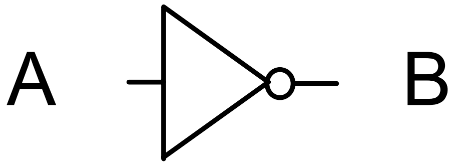


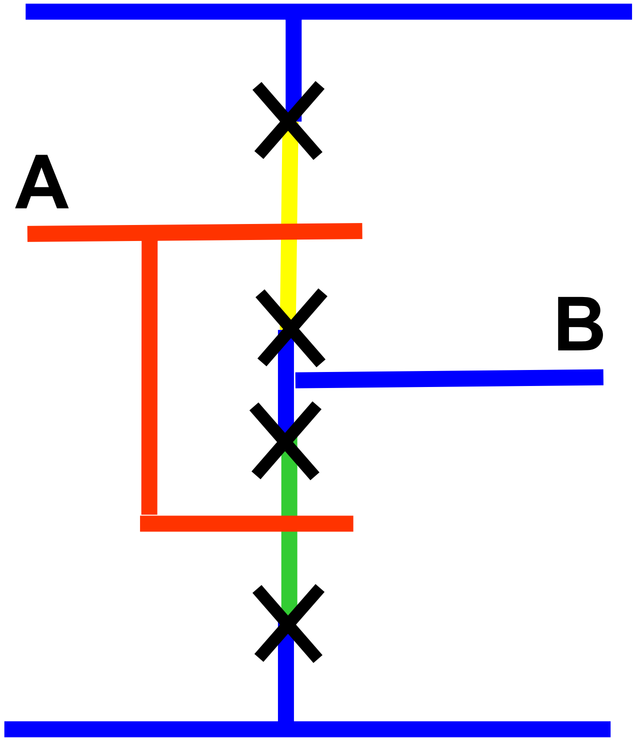
A stick diagram is not a layout but gives the basic structure that will be instantiated in the actual layout itself

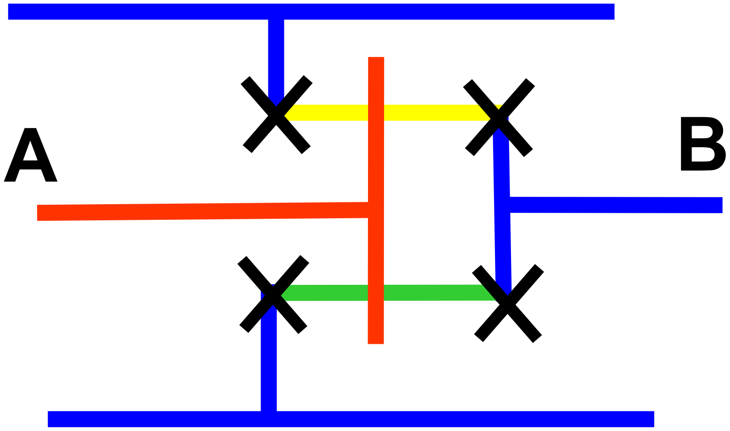
Modifications can be made much more quickly on a stick diagram than on a layout

Iteration may be needed to come up with a good layout structure

Stick Diagram







Alternate Representation

Technology Files

Technology Files

- Provide Information About Process
  - Process Flow (Fabrication Technology)
  - Model Parameters
  - Design Rules
- Serve as Interface Between Design Engineer and Process Engineer
- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries

Technology Files

- Process Flow (Fabrication Technology) (will finish discussion next week)
- Model Parameters (will discuss in detail after device models are introduced)
- Design Rules

Design Rules

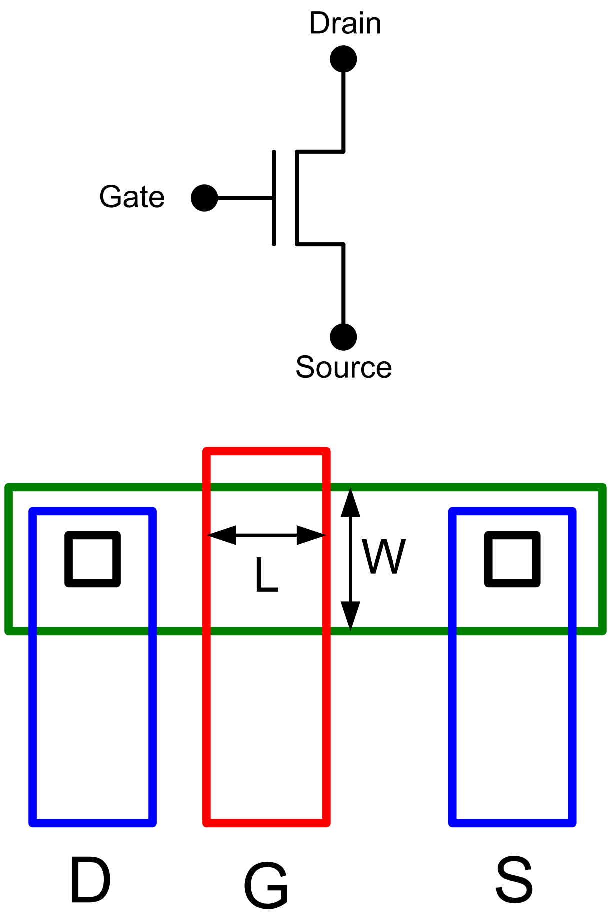
- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

- Very large number of devices can be reliably made with the design rules of a process

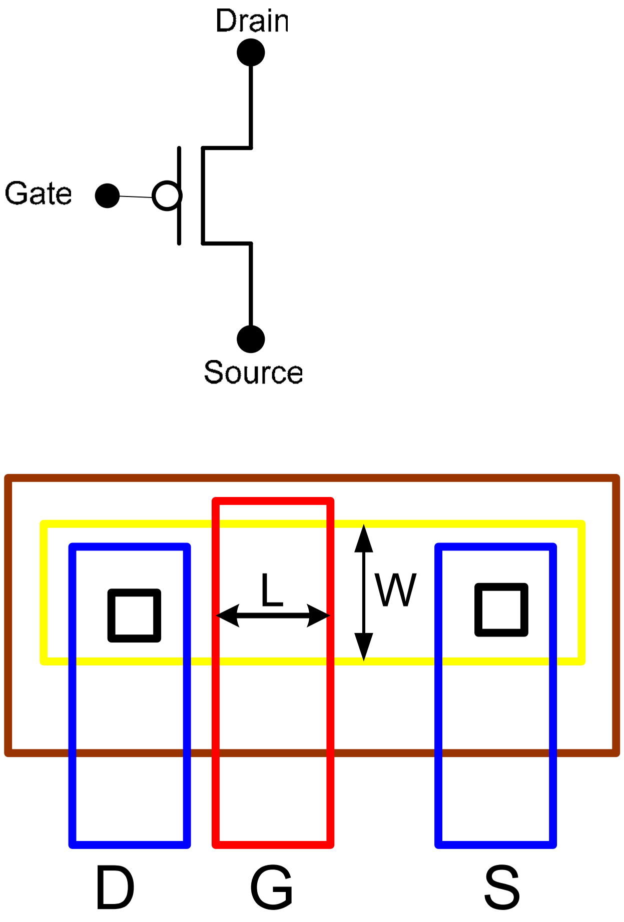
- Yield and performance unpredictable and often low if rules are violated

- Compatible with design rule checker in integrated toolsets

Design Rules – consider transistors



Layout



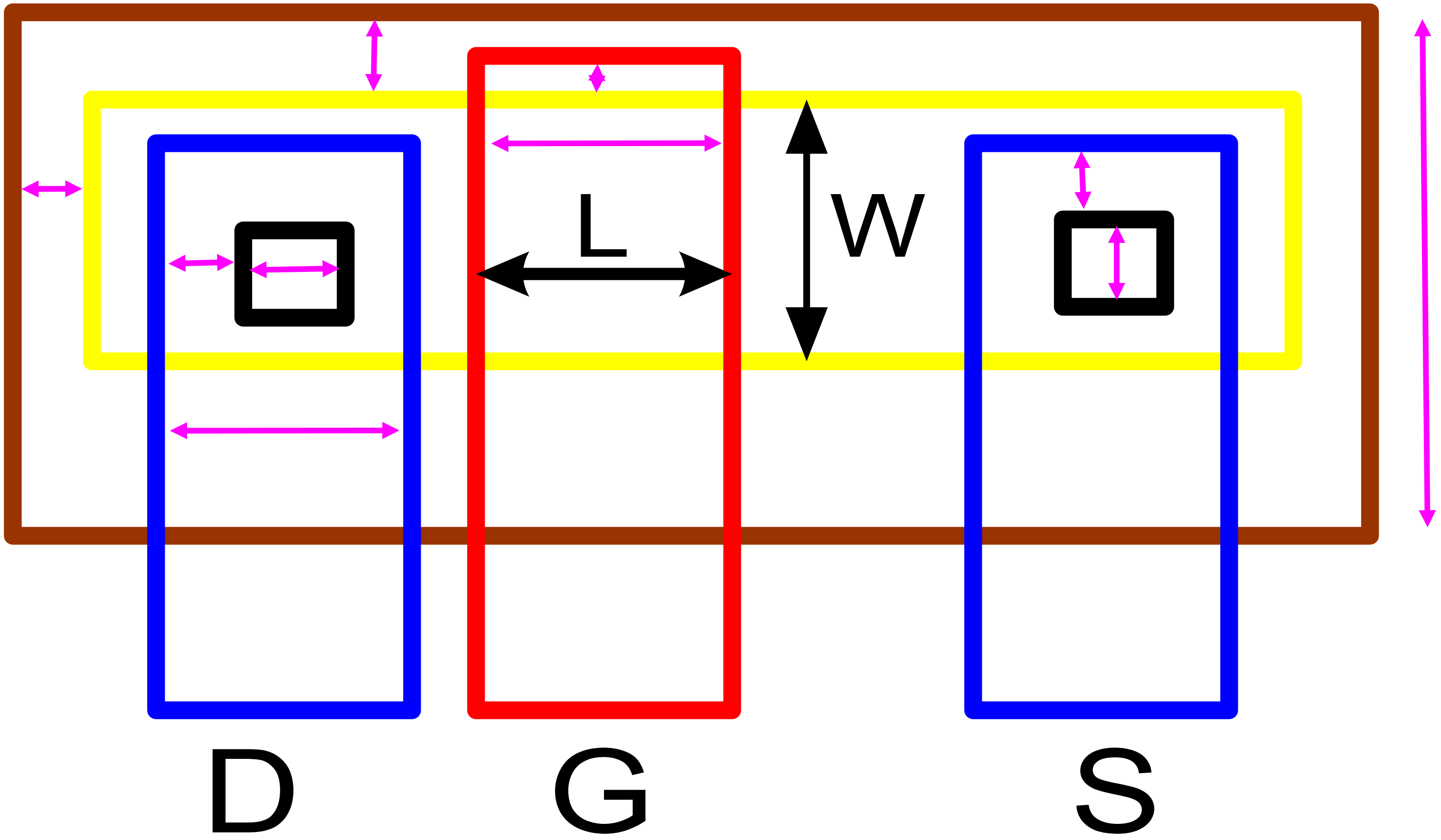
Layout

Layer Map

🟨	p-active
🟩	n-active
🟥	Poly 1
🟦	Metal 1
🟫	n-well
⬛	contact

Layout always represented in a top view in two dimensions

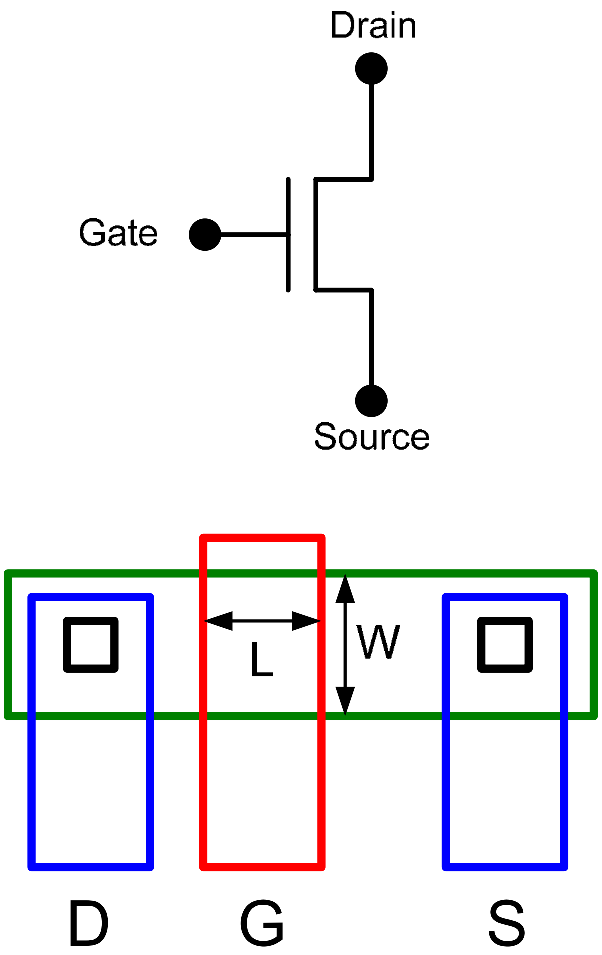
Design Rules

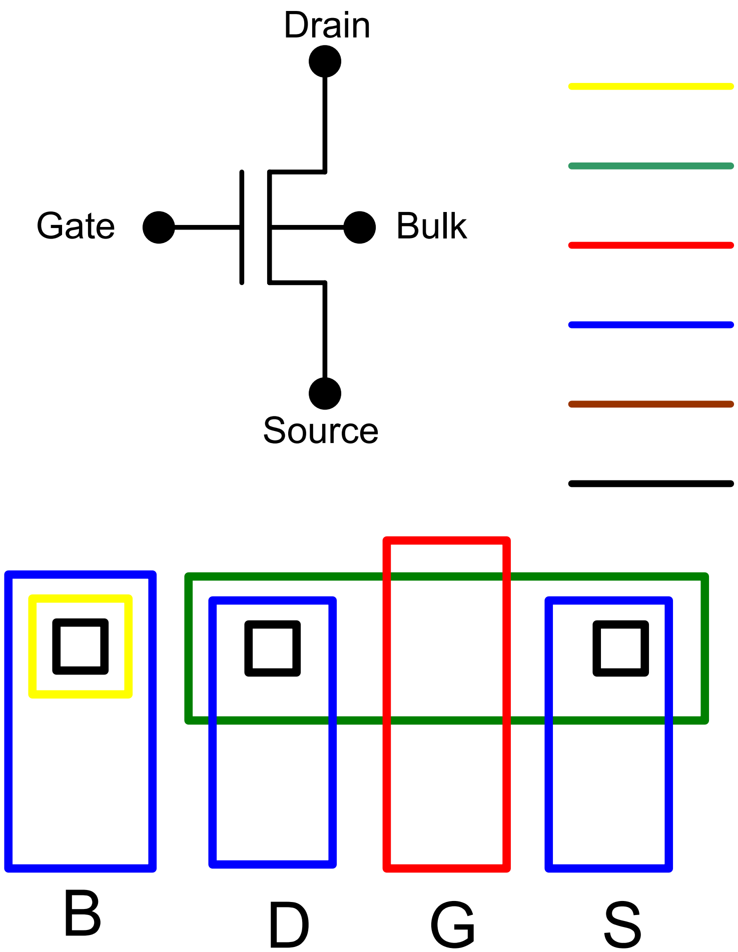


Design rules give minimum feature sizes and spacings

Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)

Design Rules – consider transistors



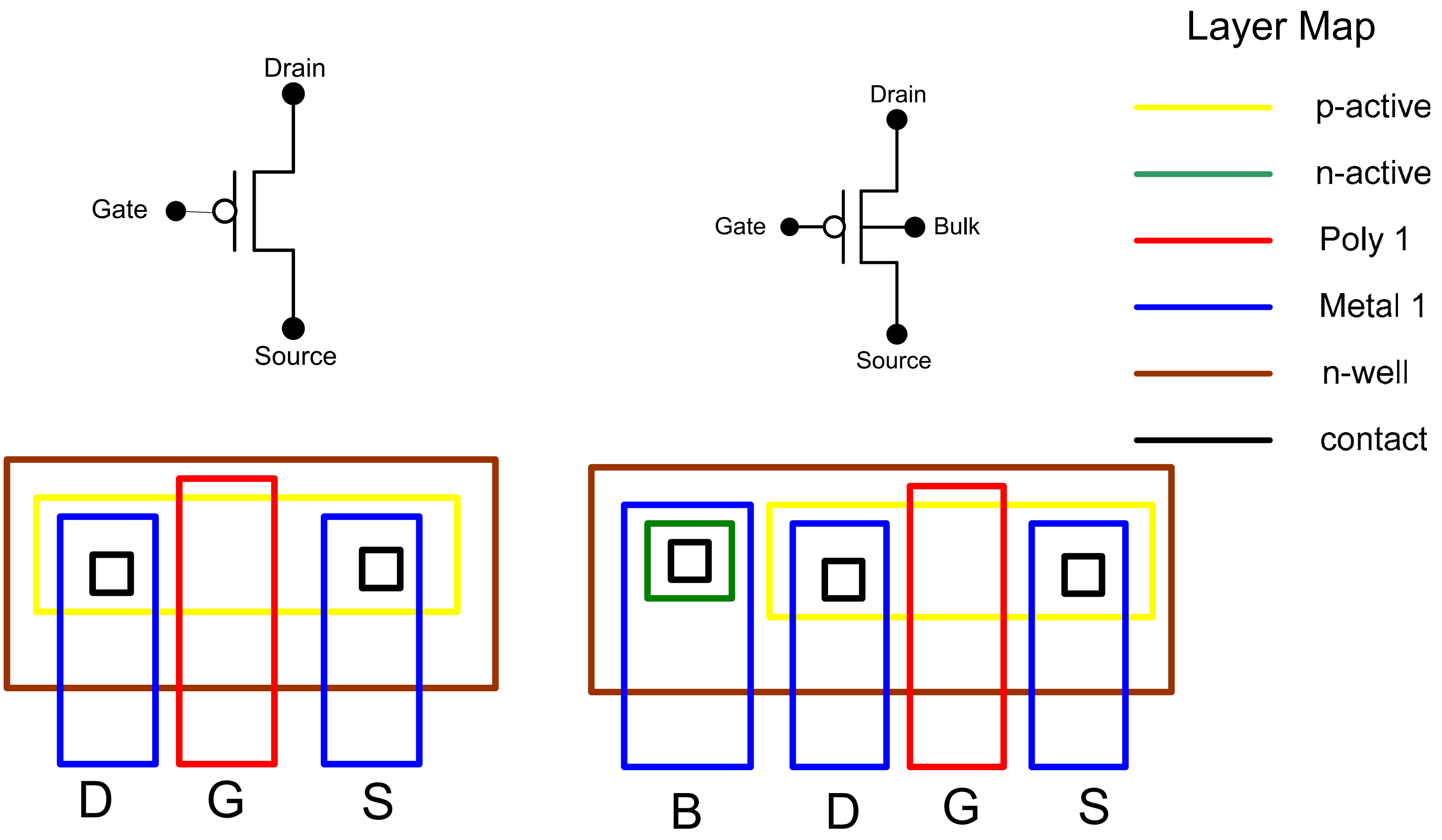


Layer Map

- 🟨 p-active
- 🟩 n-active
- 🟥 Poly 1
- 🟦 Metal 1
- 🟫 n-well
- ⬛ contact

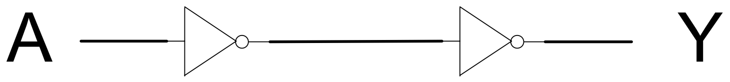
- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors**

Design Rules – consider transistors

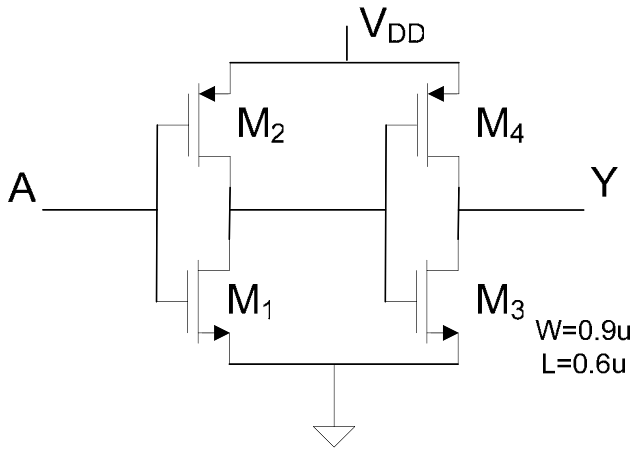


- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors is they share the same well**

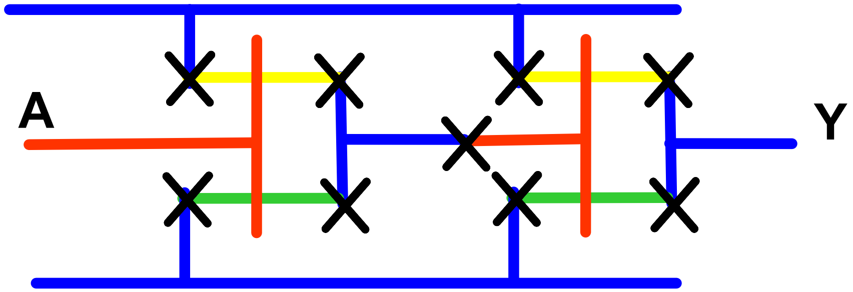
Design Rules (example)



Logic Circuit



Circuit Schematic (Including Device Sizing)



Stick Diagram

End of Lecture 5