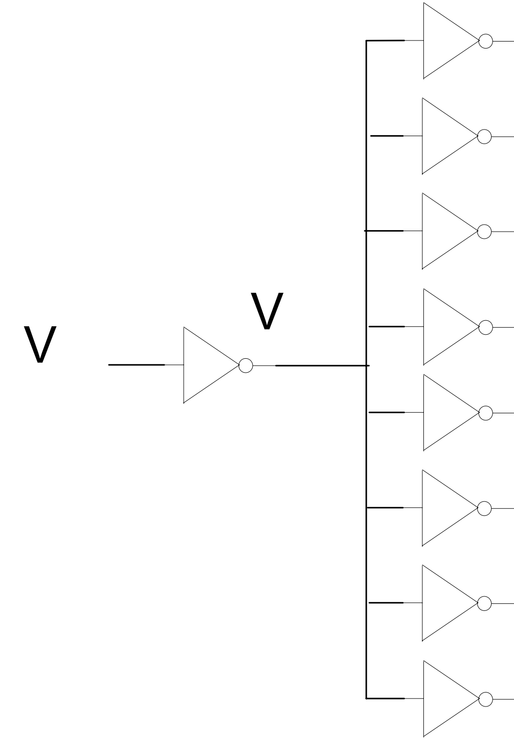
EE 434
Lecture 6

Process Technology

Quiz 4

If an n-channel MOS transistor is modeled with an input capacitance of 2fF and an on resistance of 5KΩ and a p-channel transistor with an input capacitance of 6fF and an on resistance of 5KΩ, determine the H to L transition time at the output of a standard CMOS inverter if it is driving 8 identical inverters. Assume the input an ideal step from 0 to V_{DD}.



And the number is ….

1

8

3

5

4

6

9

7

2

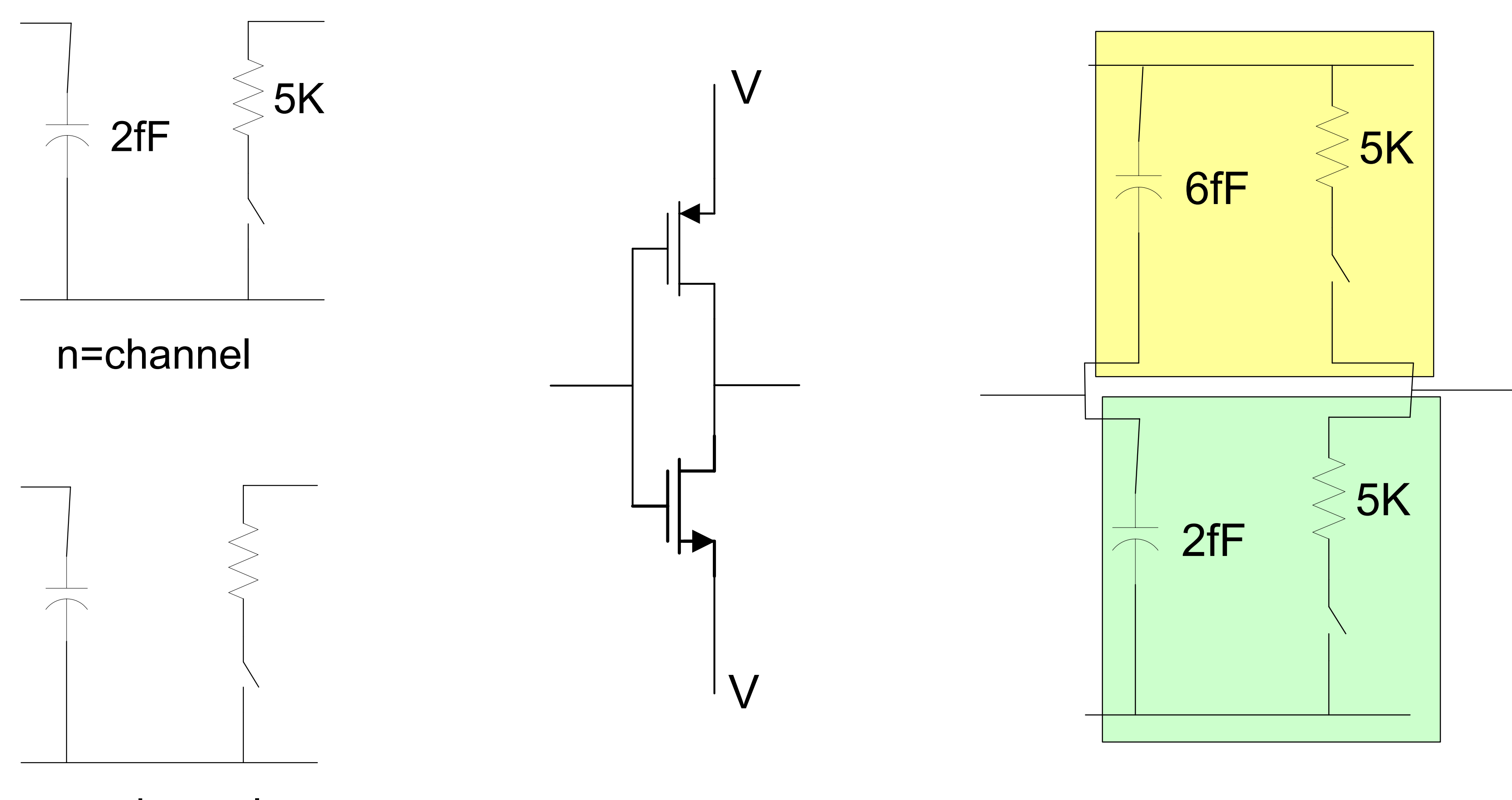
And the number is ….

1 7 3 4 9

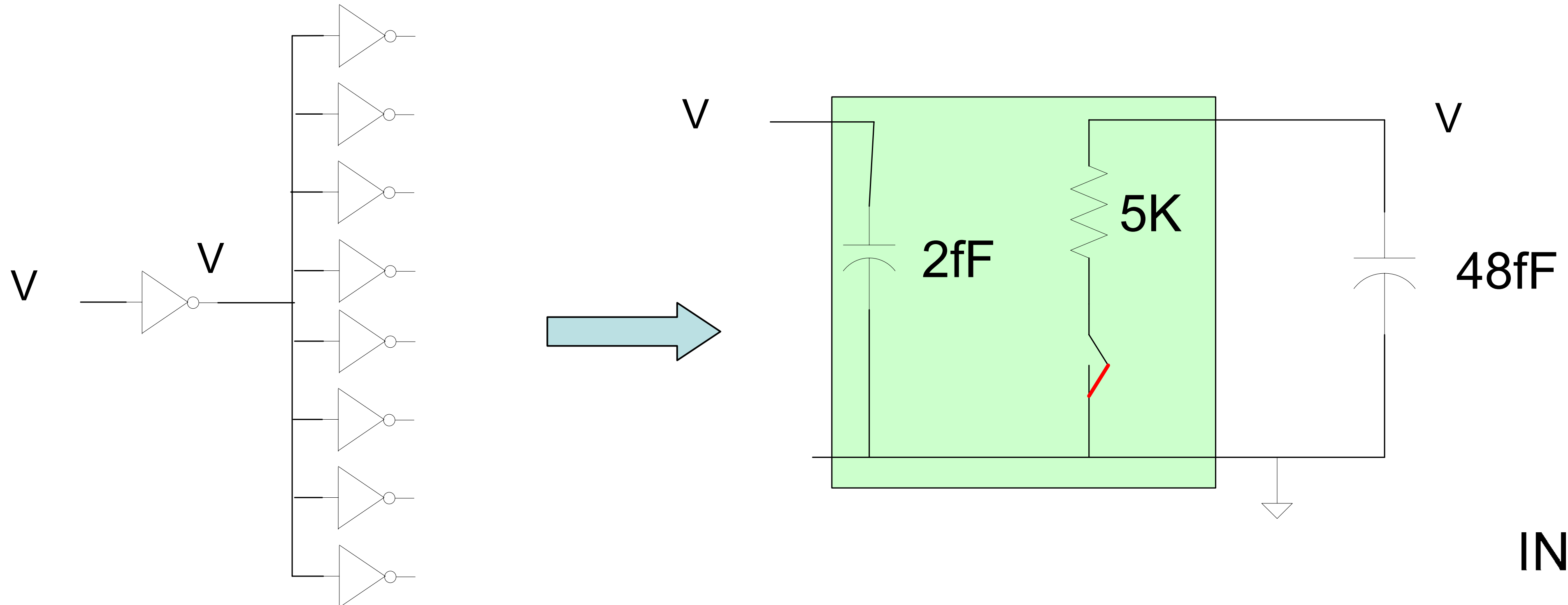
2

6 8 2 5

Quiz 4 Solution:



Quiz 4 Solution:



$t_{HL}=R_{PD}C_L=5K\ 48fF = 0.24ns$

OUT

IN

Technology Files

- Process Flow (Fabrication Technology) (will finish discussion next week)
- Model Parameters (will discuss in detail after device models are introduced)
- Design Rules

Design Rules

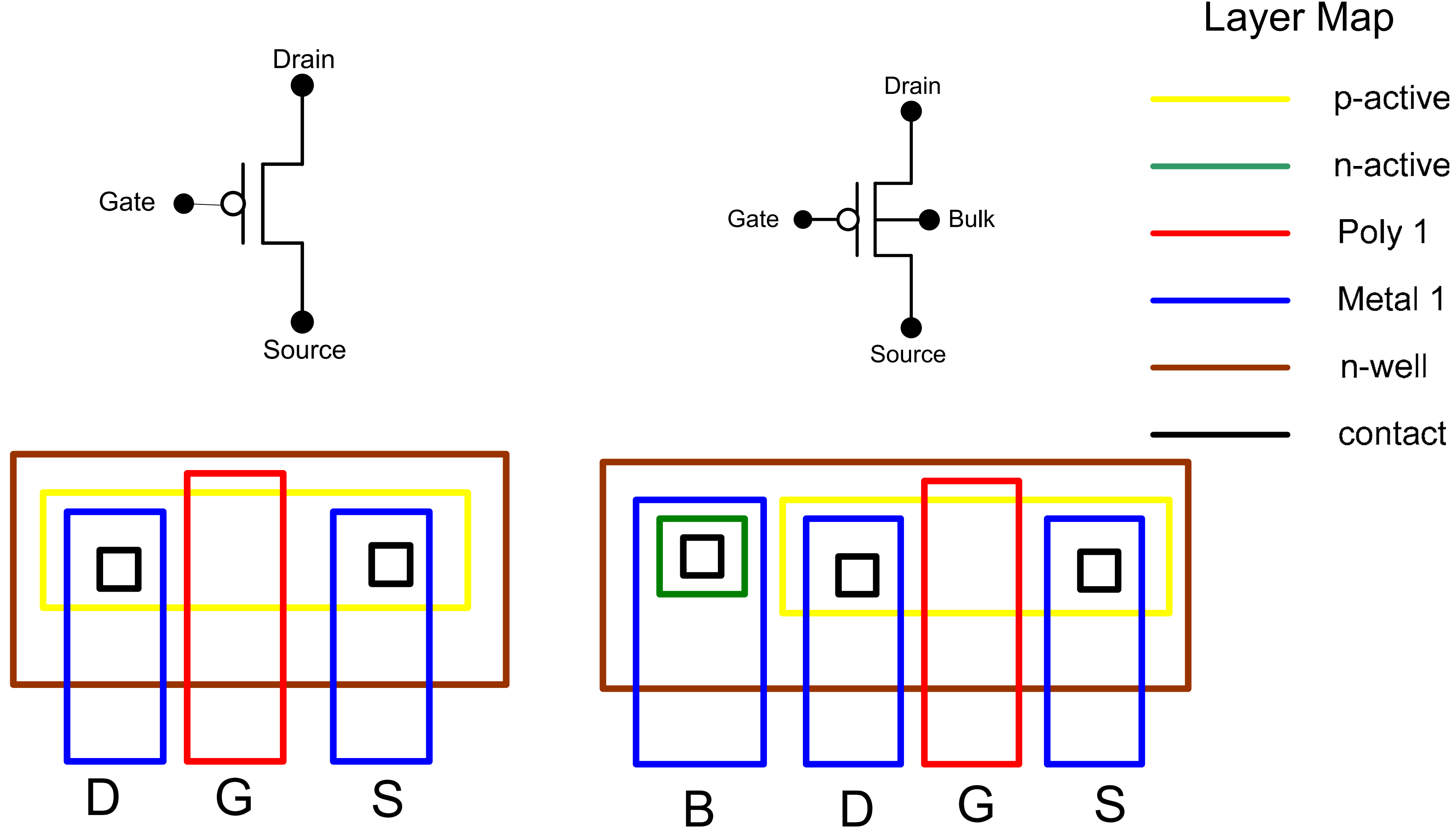
- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

- Very large number of devices can be reliably made with the design rules of a process

- Yield and performance unpredictable and often low if rules are violated

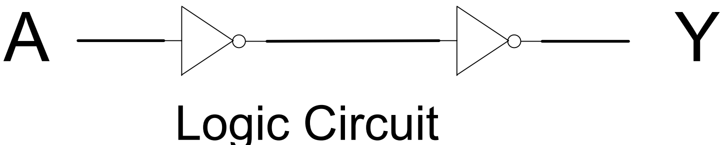
- Compatible with design rule checker in integrated toolsets

Design Rules – consider transistors

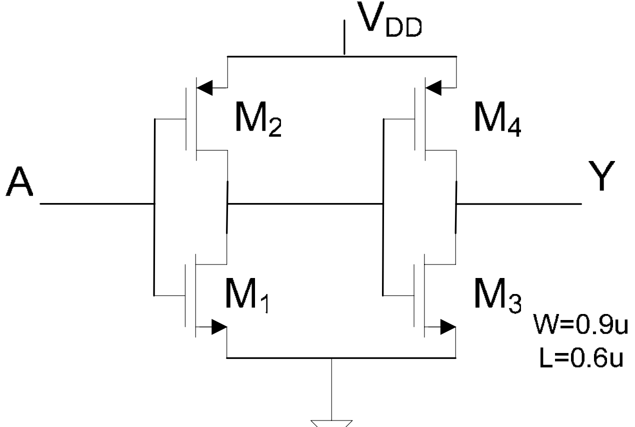


- **Bulk connection needed**
- **Single bulk connection can often be used for several (many) transistors is they share the same well**

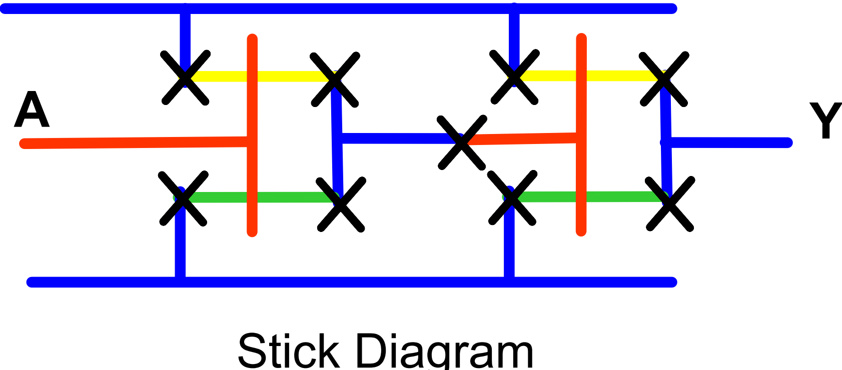
Design Rules (example)



Logic Circuit

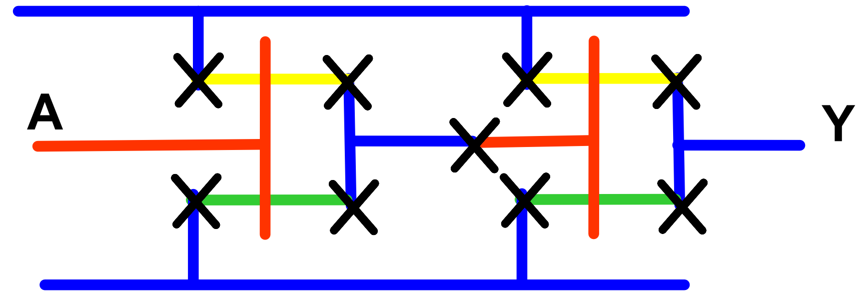


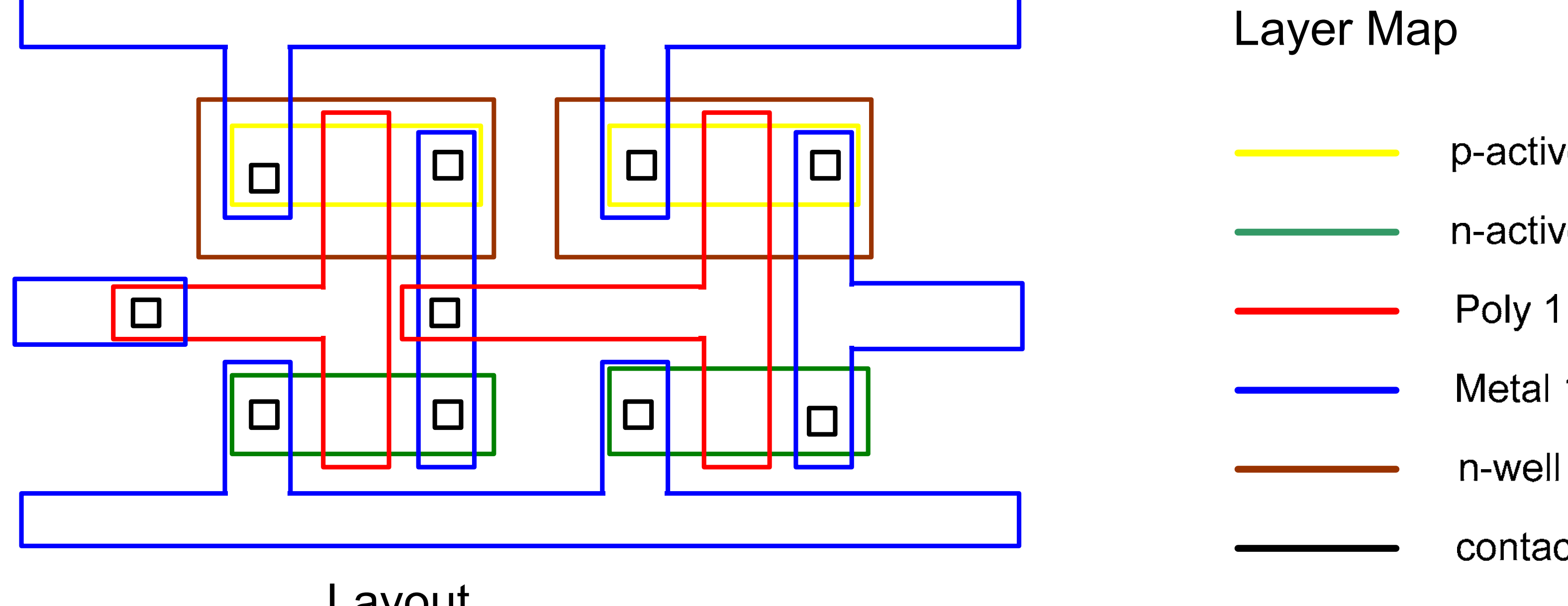
Circuit Schematic (Including Device Sizing)



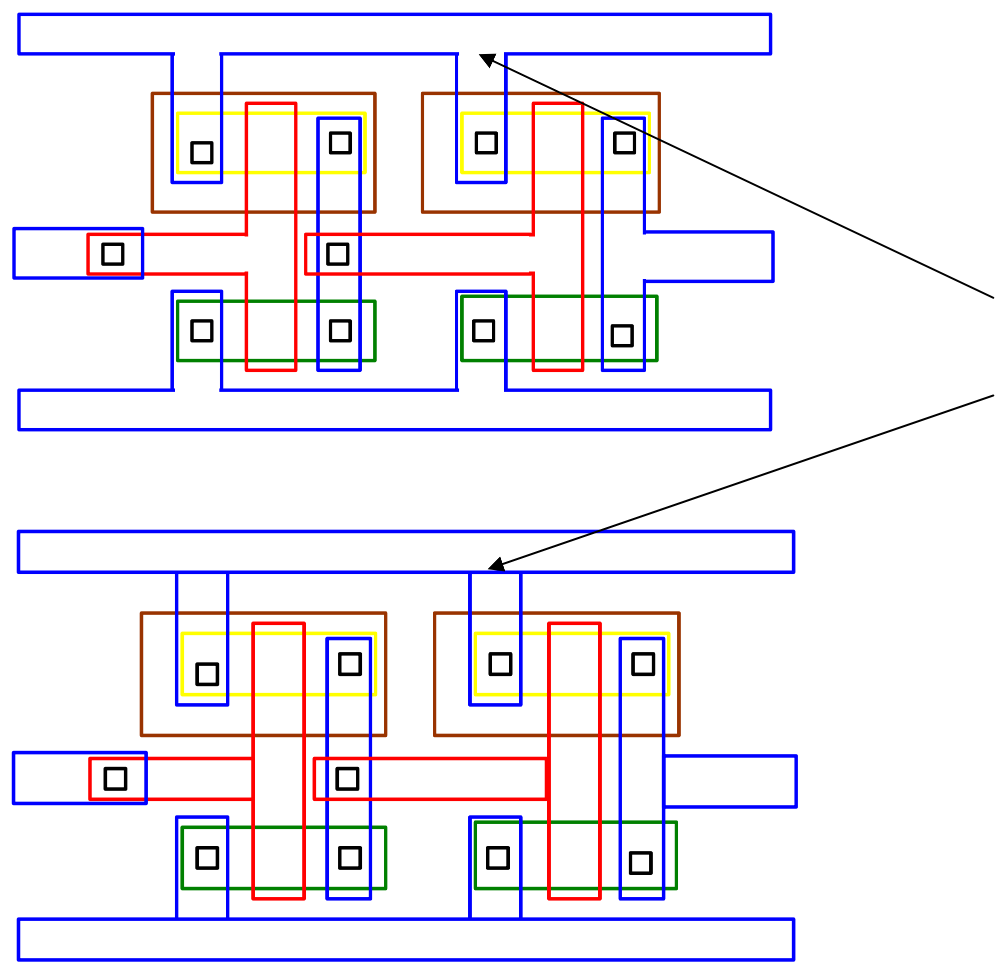
Stick Diagram

Design Rules (example)



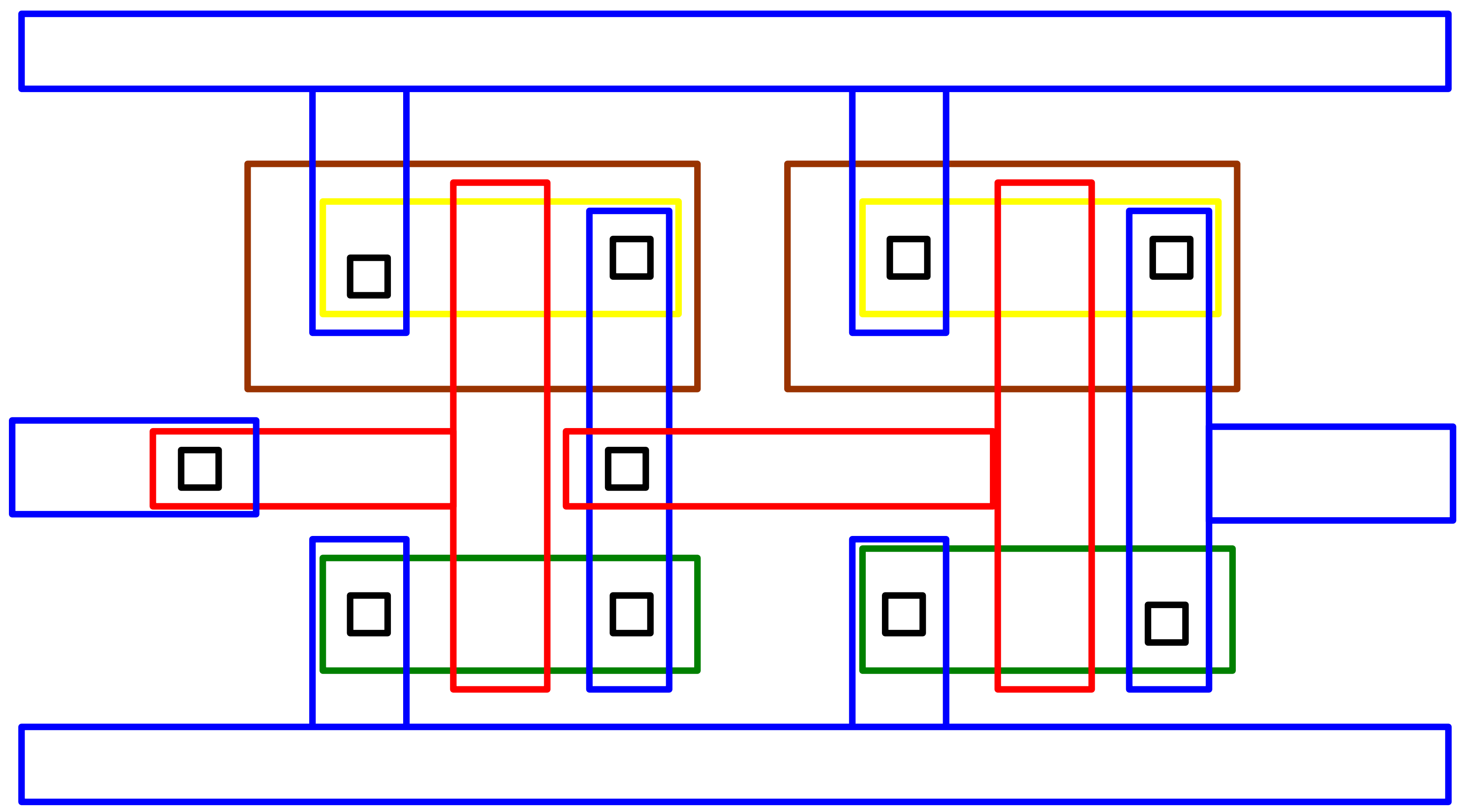


Design Rules (example)



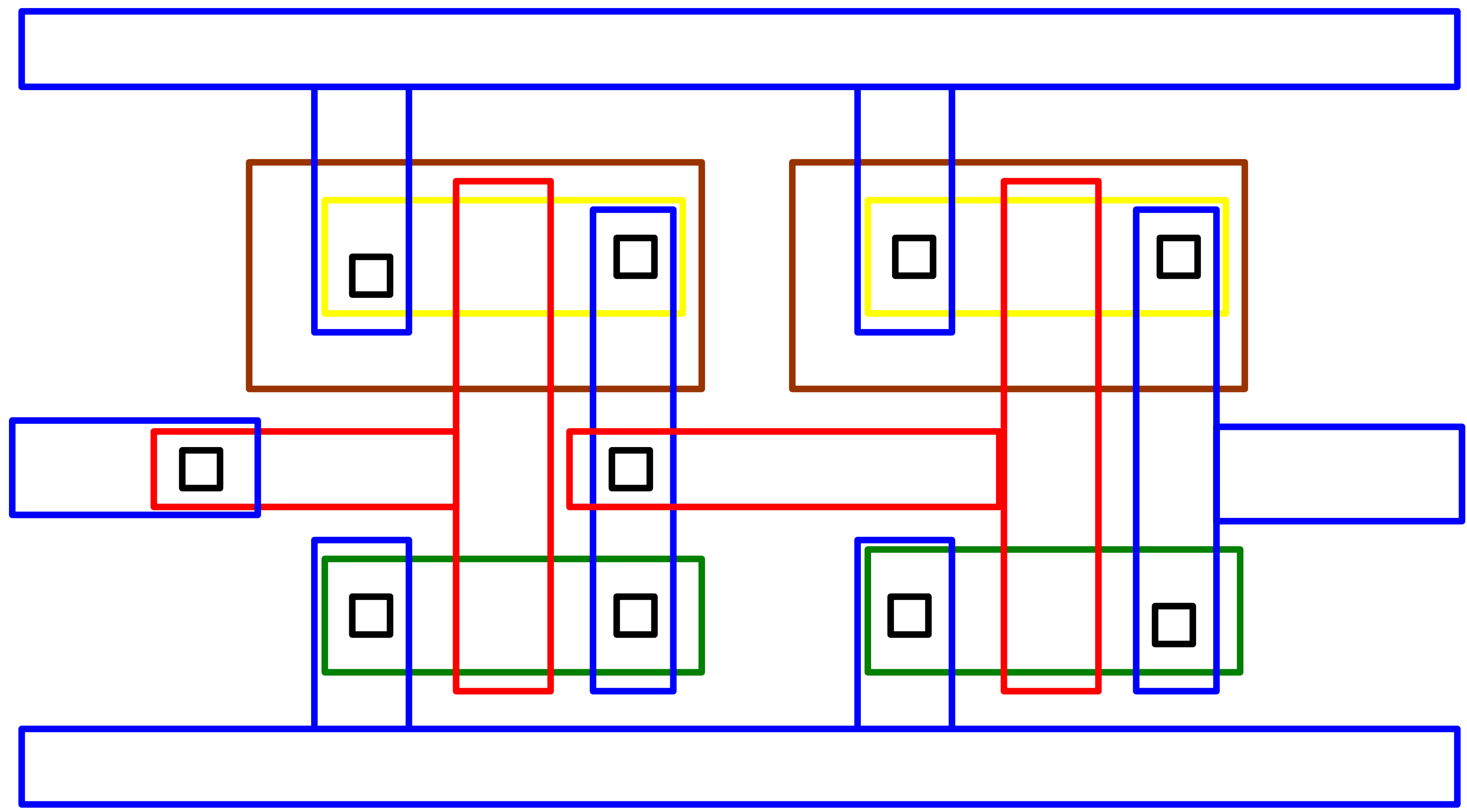
- Polygons merged in Geometric Description File (GDF)
- Separate rectangles generally more convenient to represent

Design Rules (example)



- Design rules must be satisfied throughout the design
- DRC runs incrementally during layout in most existing tools to flag most problems
- DRC can catch layout errors but not circuit design errors

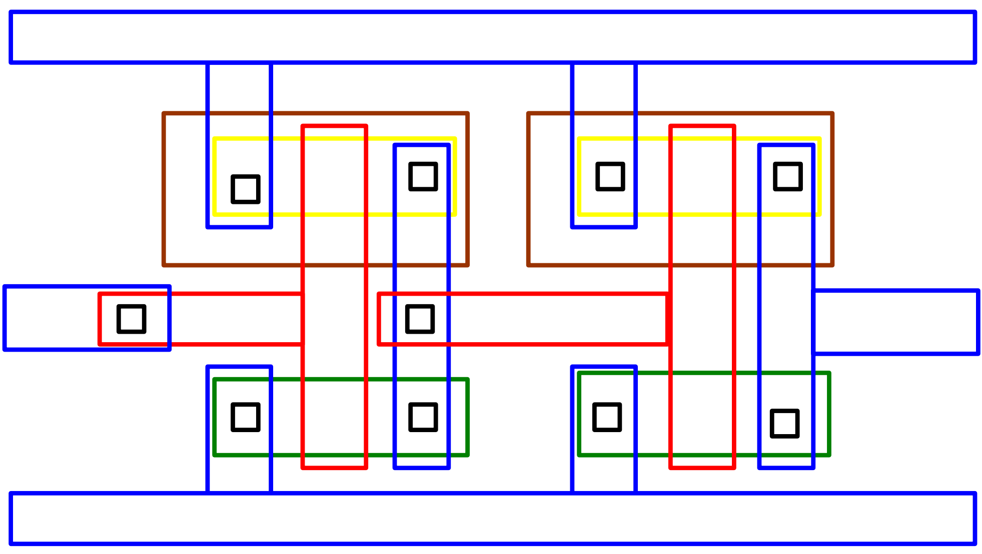
Design Rules (example)



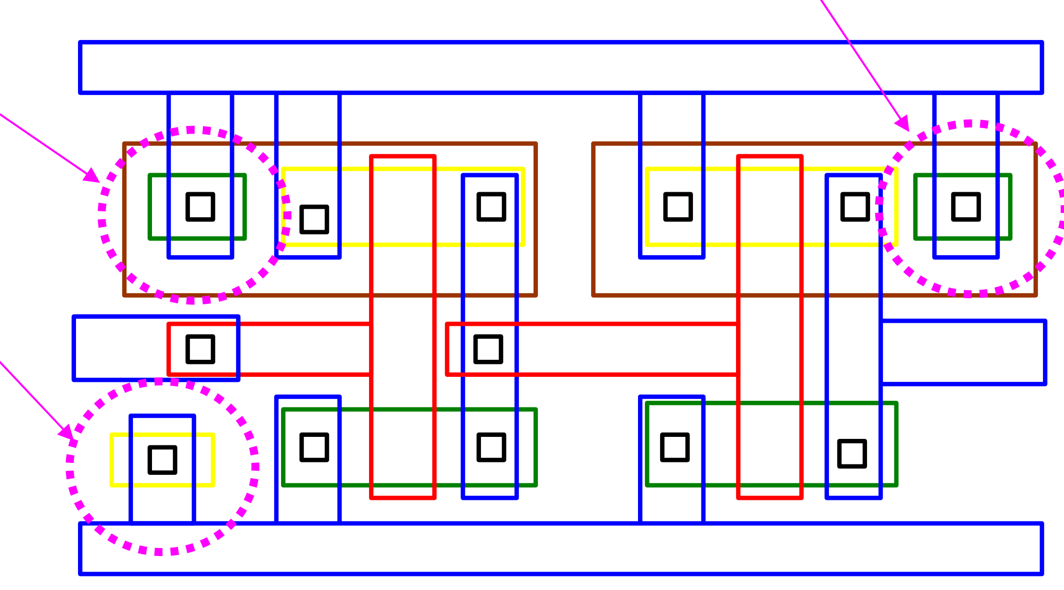
What is wrong with this layout ?

Bulk connections missing!

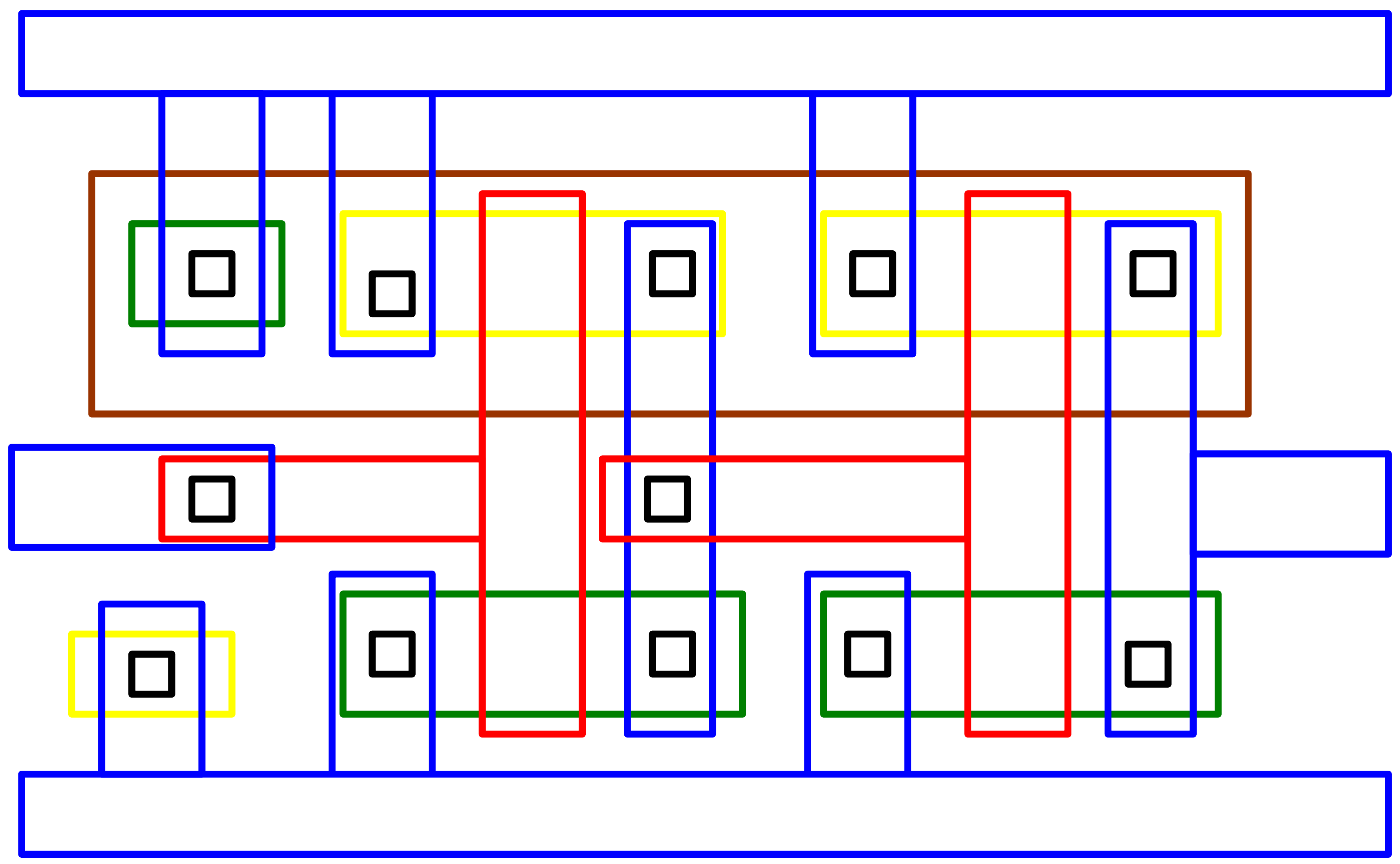
Design Rules (example)



- Note diffusions needed for bulk connections
- Note p-well connections increase area a significant amount
- Note p-wells are both connected to V_{DD} in this circuit

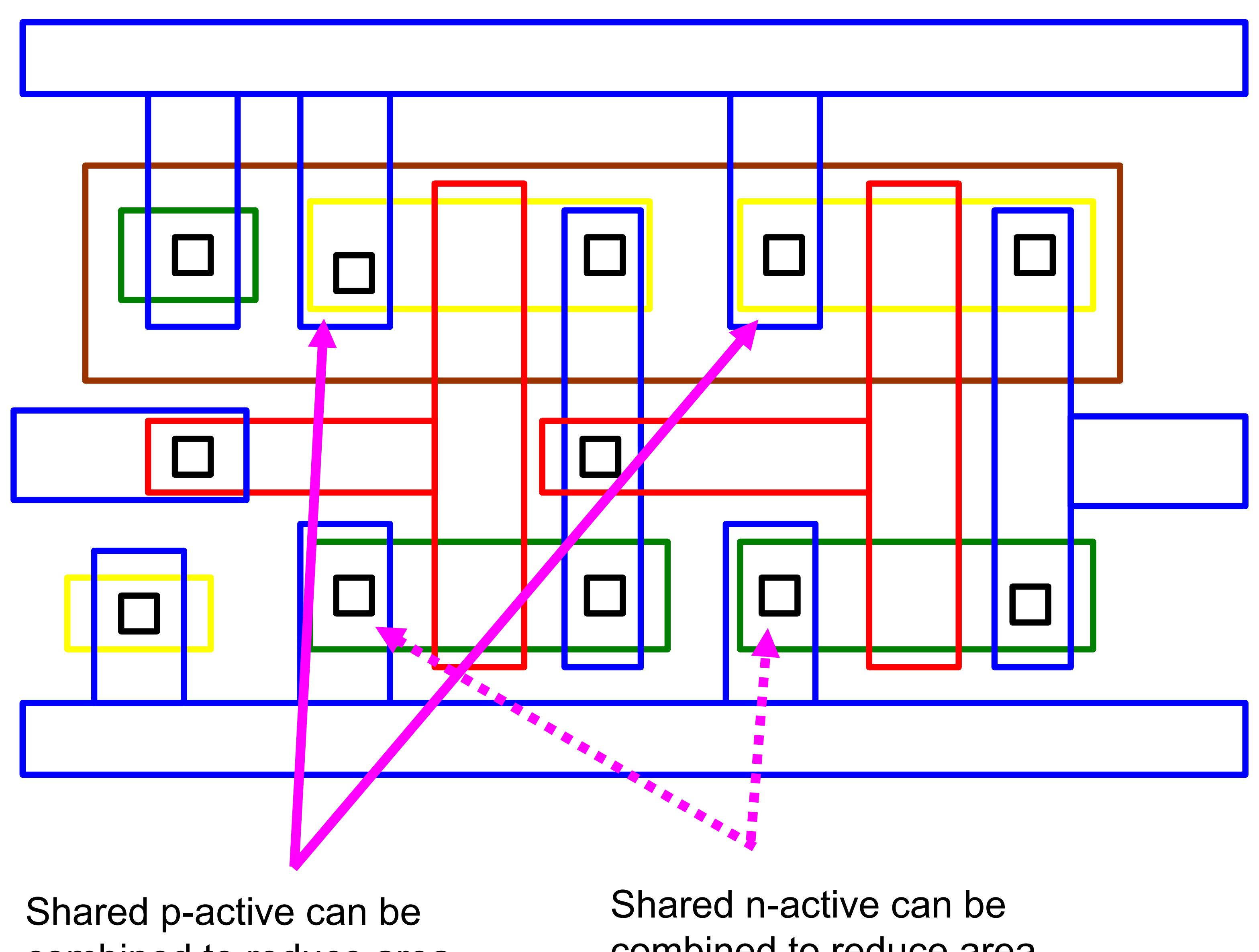


Design Rules (example)



Layout with shared p-well reduces area

Design Rules (example)



Design Rules

- Design rules can be given in absolute dimensions for every rule
- Design rules can be parameterized and given relative to a parameter
  - Makes movement from one process to another more convenient
  - Easier for designer to remember
  - Some penalty in area efficiency
  - Often termed λ-based design rules
  - Typically λ is ½ the minimum feature size in a process

Design Rules

- See www.MOSIS.org for design rules

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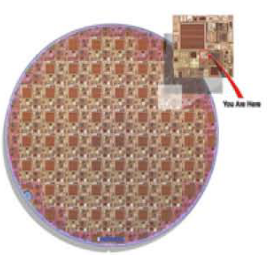

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AMIS - austriamicrosytems - IBM - TSMC
All Fabricators

Fabrication Schedule

AUG 15: AMI_ABN
AUG 15: TSMC 0.25
AUG 15: IBM 8RF-LM
AUG 22: AMI I2T100
AUG 29: TSMC 0.18
AUG 29: AMS S35D4
AUG 29: Ommic GaAs
SEP 06: AMI_C5
SEP 12: IBM 5HP/AM
SEP 12: IBM 8RF-DM
SEP 12: AMS C35B4
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Projects submitted to MOSIS for fabrication can be designed using either vendor-independent, scalable rules (MOSIS SCMOS Rules), or design rules specific to a process.

Vendor and MOSIS SCMOS Design Rules

Vendor Rules
Vendors consider their rules, process specifications, and SPICE parameters proprietary and make them available to MOSIS commercial account holders in different ways.

SCMOS Rules
MOSIS Scalable CMOS (SCMOS) is a set of logical layers together with their design rules, which provide a nearly process- and metric-independent interface to all CMOS fabrication processes available through MOSIS.

Related Links
- Fabrication Schedule
- Customer Support
- MOSIS Products

Fabrication Schedule
AUG 15: AMI_ABN
AUG 15: TSMC 0.25
AUG 15: IBM 8RF-LM
AUG 22: AMI I2T100
AUG 29: TSMC 0.18
AUG 29: AMS S35D4
AUG 29: Ommic GaAs
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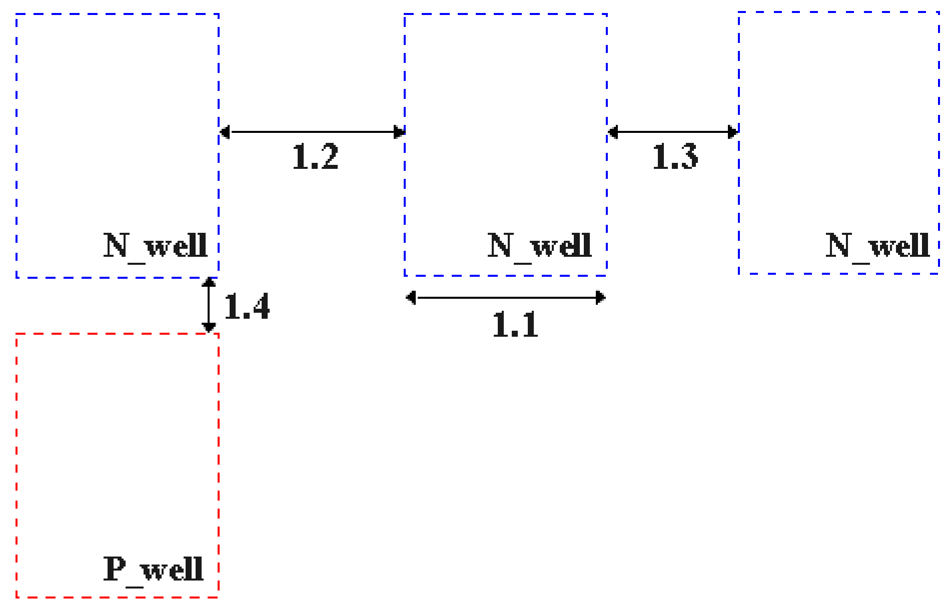
Design Rules

- See www.MOSIS.org for design rules
- Some of these files are on class WEB site
  - SCMOS Rules Updated Sept 2005.pdf
  - Mosis Rules Pictorial.pdf

SCMOS Layout Rules - Well

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9	18	18
1.3	Minimum spacing between wells at same potential	6	6	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0

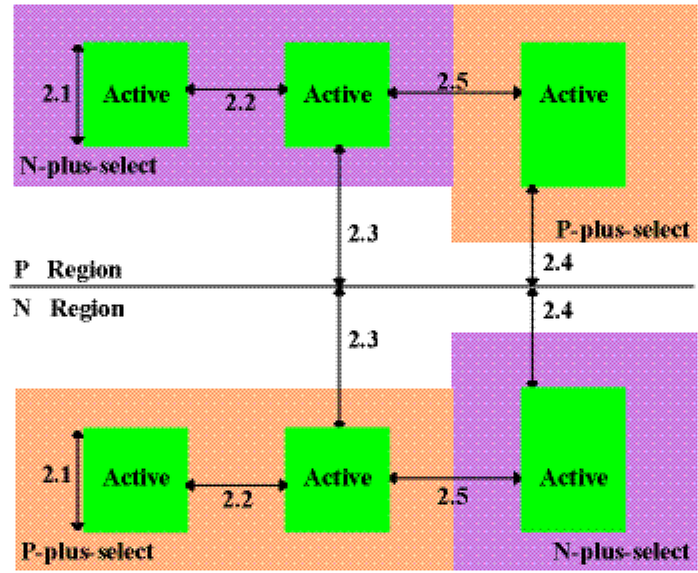


SCMOS Layout Rules - Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4

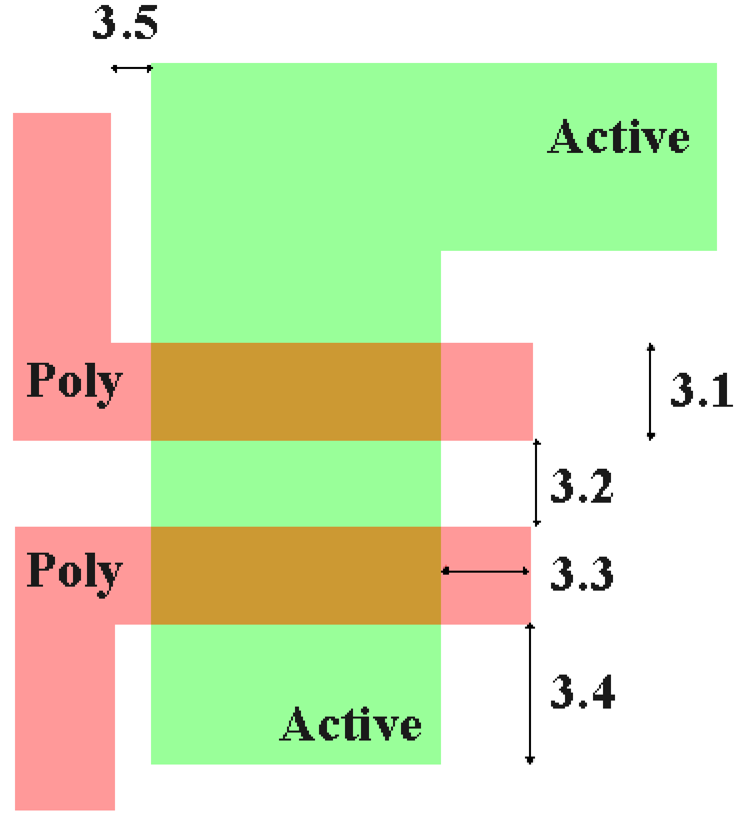
* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

Process	Design Technology	Design Lambda (micrometers)	Minimum Width (lambda)
AMI_ABN	SCNA, SCNE	0.80	5
AMI_C5F/N	SCN3M, SCN3ME	0.35	9
AMI_C5F/N	SCN3M_SUBM, SCN3ME_SUBM	0.30	10



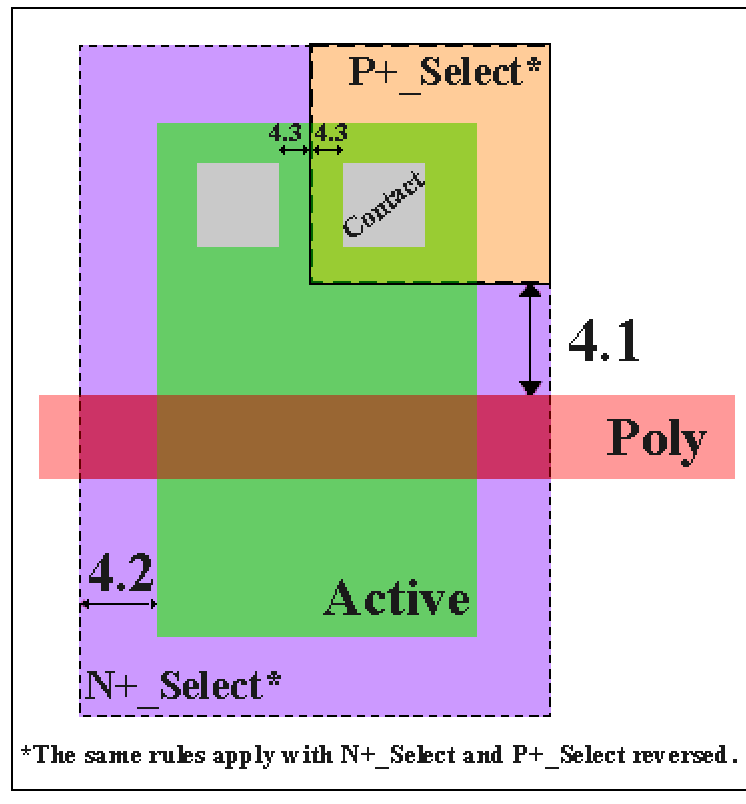
SCMOS Layout Rules - Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



SCMOS Layout Rules - Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	2	4



SCMOS Layout Rules - Contact to Poly

On 0.50 micron process (and all finer feature size processes), it is required that all features on the insulator layers (CONTACT, VIA, VIA2) must be of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

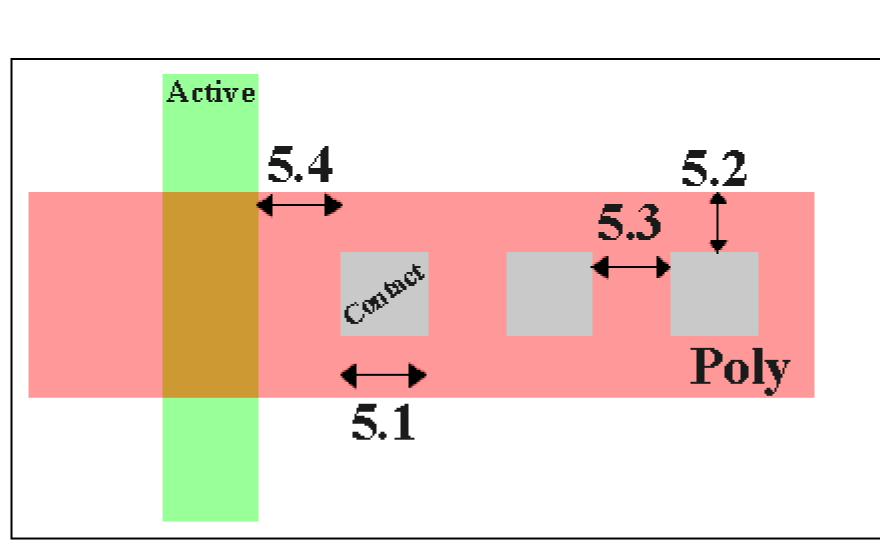
If your design cannot tolerate 1.5 lambda contact overlap in 5.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 5.1, 5.3, and 5.4, still apply and are unchanged.

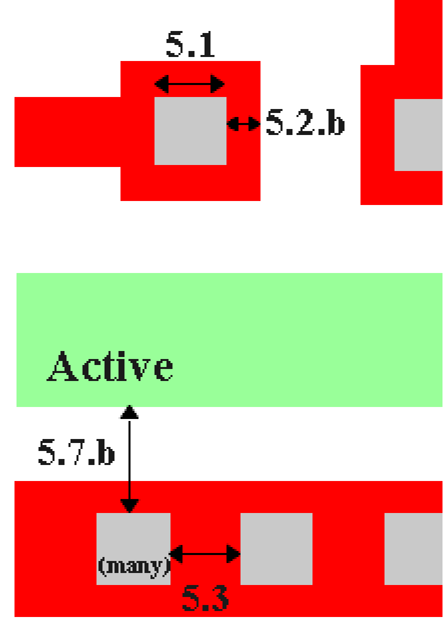
Simple Contact to Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2
5.2	Minimum poly overlap	1.5	1.5	1.5
5.3	Minimum contact spacing	2	3	4
5.4	Minimum spacing to gate of transistor	2	2	2

Alternative Contact to Poly

Rule	Description	Lambda		
	SCMOS	SUBM	DEEP	
5.2.b	Minimum poly overlap	1	1	1
5.5.b	Minimum spacing to other poly	4	5	5
5.6.b	Minimum spacing to active (one contact)	2	2	2
5.7.b	Minimum spacing to active (many contacts)	3	3	3





Simple Poly to Contact Alternative (

SCMOS Layout Rules - Contact to Active

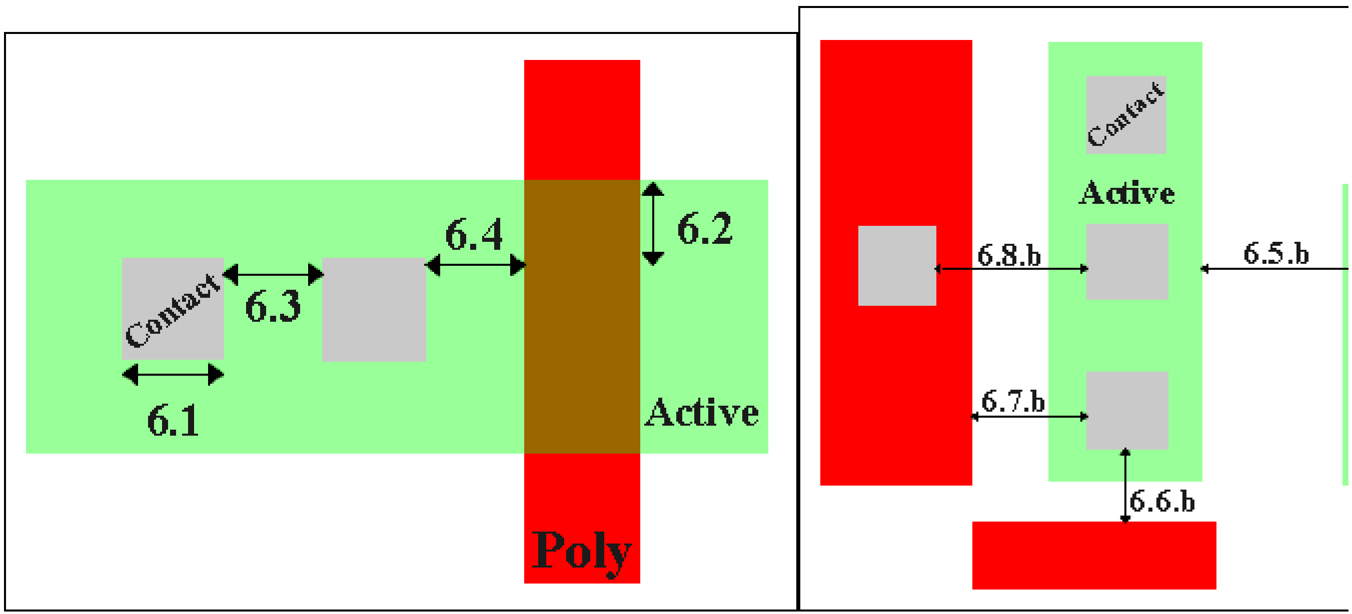
If your design cannot handle the 1.5 lambda contact overlap in 6.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 6.1, 6.3, and 6.4, still apply and are unchanged. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

Simple Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2
6.2	Minimum active overlap	1.5	1.5	1.5
6.3	Minimum contact spacing	2	3	4
6.4	Minimum spacing to gate of transistor	2	2	2

Alternative Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.2.b	Minimum active overlap	1	1	1
6.5.b	Minimum spacing to diffusion active	5	5	5
6.6.b	Minimum spacing to field poly (one contact)	2	2	2
6.7.b	Minimum spacing to field poly (many contacts)	3	3	3
6.8.b	Minimum spacing to poly contact	4	4	4

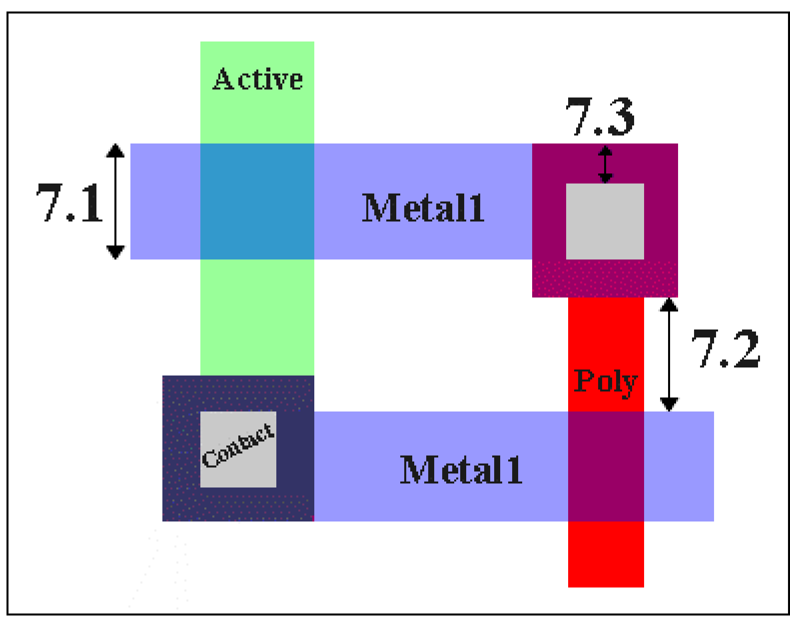


Simple Contact to Active

Alternative Contac

SCMOS Layout Rules - Metal1

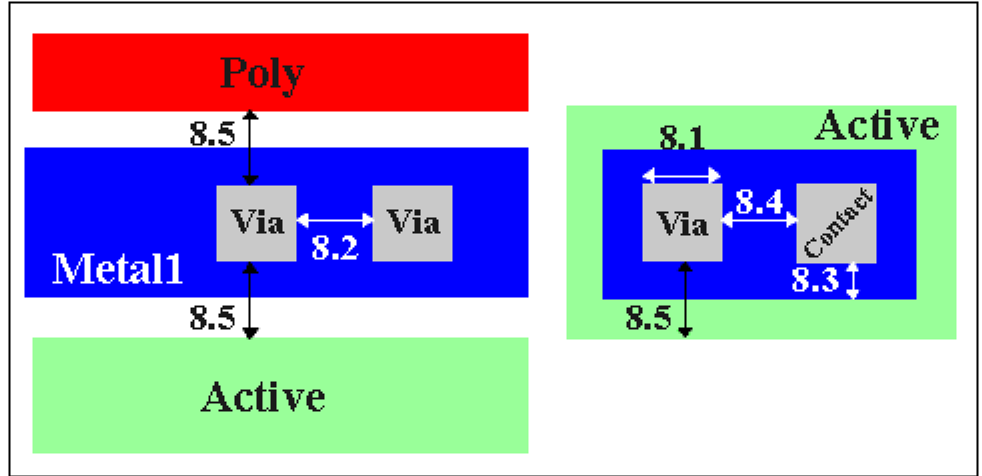
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
7.1	Minimum width	3	3	3
7.2	Minimum spacing	2	3	3
7.3	Minimum overlap of any contact	1	1	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	4	6	6



SCMOS Layout Rules - Via

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

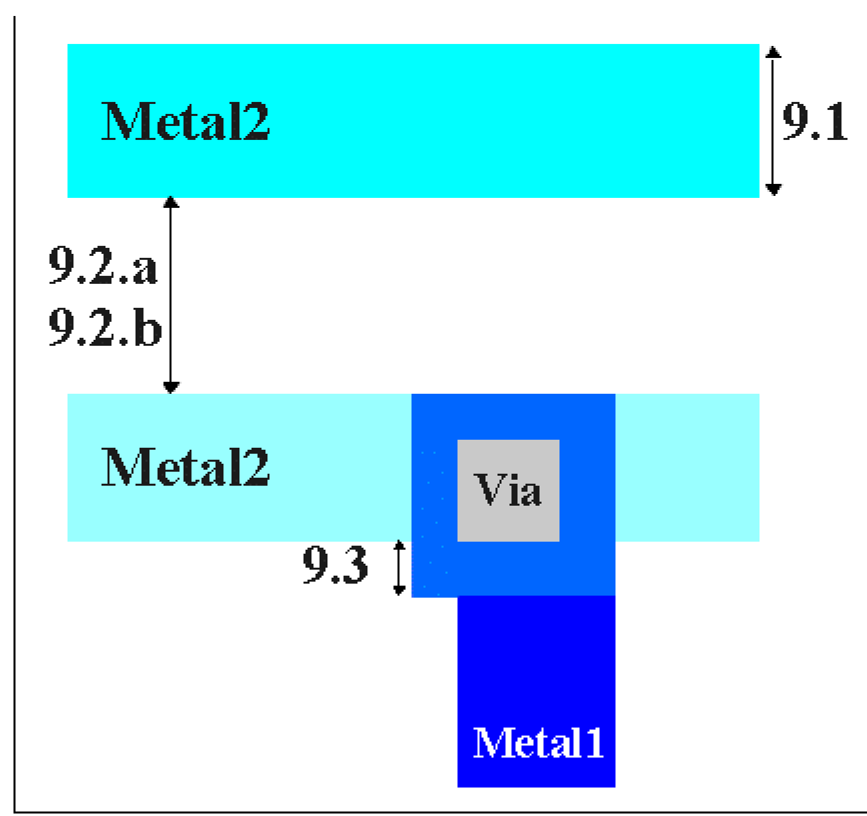
Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
8.1	Exact size	2 x 2	n/a	n/a	2 x 2	2 x 2	3 x 3
8.2	Minimum via1 spacing	3	n/a	n/a	3	3	3
8.3	Minimum overlap by metal1	1	n/a	n/a	1	1	1
8.4	Minimum spacing to contact for technology codes mapped to processes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3MLC)	2	n/a	n/a	2	2	n/a
8.5	Minimum spacing to poly or active edge for technology codes mapped to processes that do not allow stacked vias (NOTE: list is not same as for 8.4)	2	n/a	n/a	2	2	n/a



SCMOS Layout Rules - Metal2

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
9.1	Minimum width	3	n/a	n/a	3	3	3
9.2	Minimum spacing	3	n/a	n/a	3	3	4

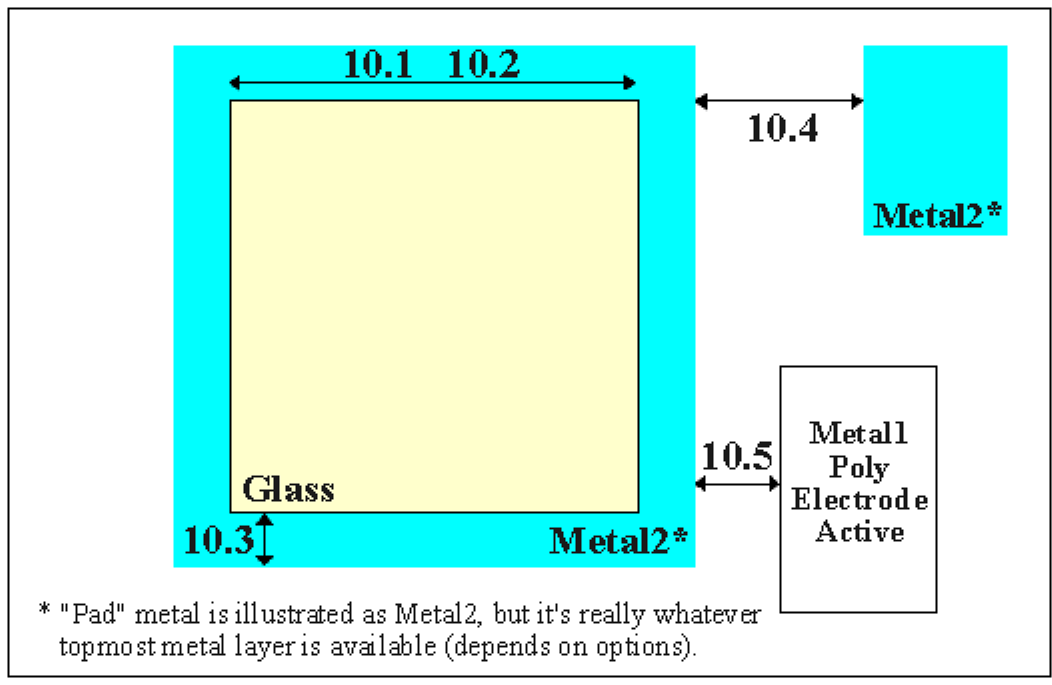
9.3	Minimum overlap of via1	1	n/a	n/a	1	1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	n/a	n/a	6	6	8



SCMOS Layout Rules - Overglass

Note that rules in this section are in units of microns. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.

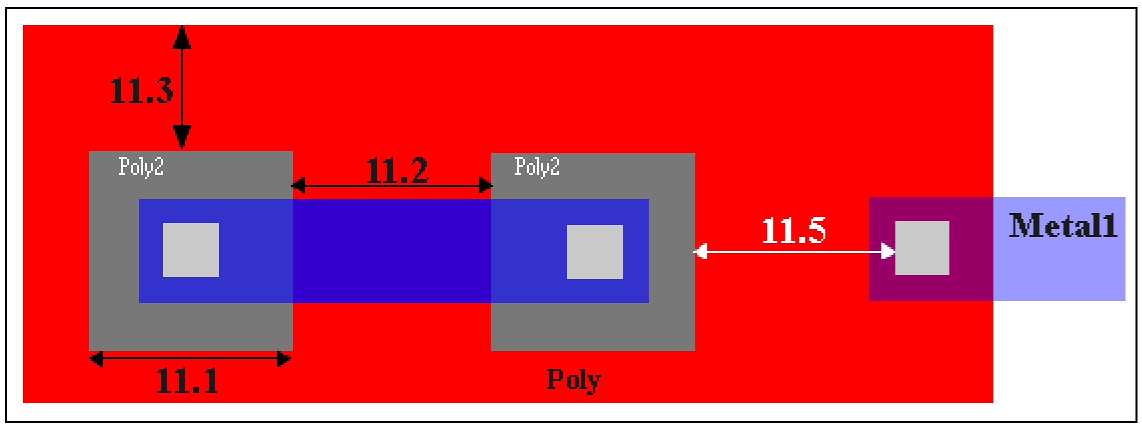
Rule	Description	Microns
10.1	Minimum bonding passivation opening	60
10.2	Minimum probe passivation opening	20
10.3	Pad metal overlap of passivation	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to active, poly or poly2	15



SCMOS Layout Rules - Poly2 for Capacitor

The poly2 layer is a second polysilicon layer (physically above the standard, or first, poly layer). The oxide between the two polys is the capacitor dielectric. The capacitor area is the area of coincident poly and electrode.

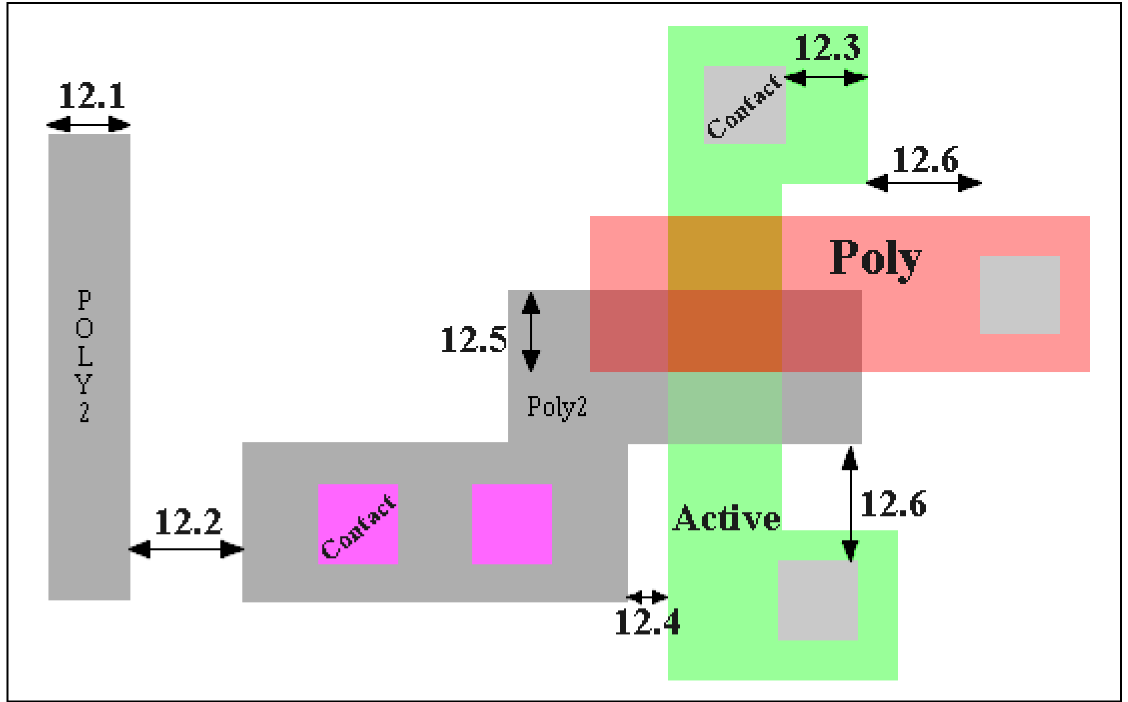
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
11.1	Minimum width	3	7	n/a
11.2	Minimum spacing	3	3	n/a
11.3	Minimum poly overlap	2	5	n/a
11.4	Minimum spacing to active or well edge (not illustrated)	2	2	n/a
11.5	Minimum spacing to poly contact	3	6	n/a
11.6	Minimum spacing to *unrelated* metal	2	2	n/a



SCMOS Layout Rules - Poly2 for Transistor
Same poly2 layer as for caps

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
12.1	Minimum width	2	2	n/a
12.2	Minimum spacing	3	3	n/a
12.3	Minimum electrode gate overlap of active	2	2	n/a

12.4	Minimum spacing to active	1	1	n/a
12.5	Minimum spacing or overlap of poly	2	2	n/a
12.6	Minimum spacing to poly or active contact	3	3	n/a

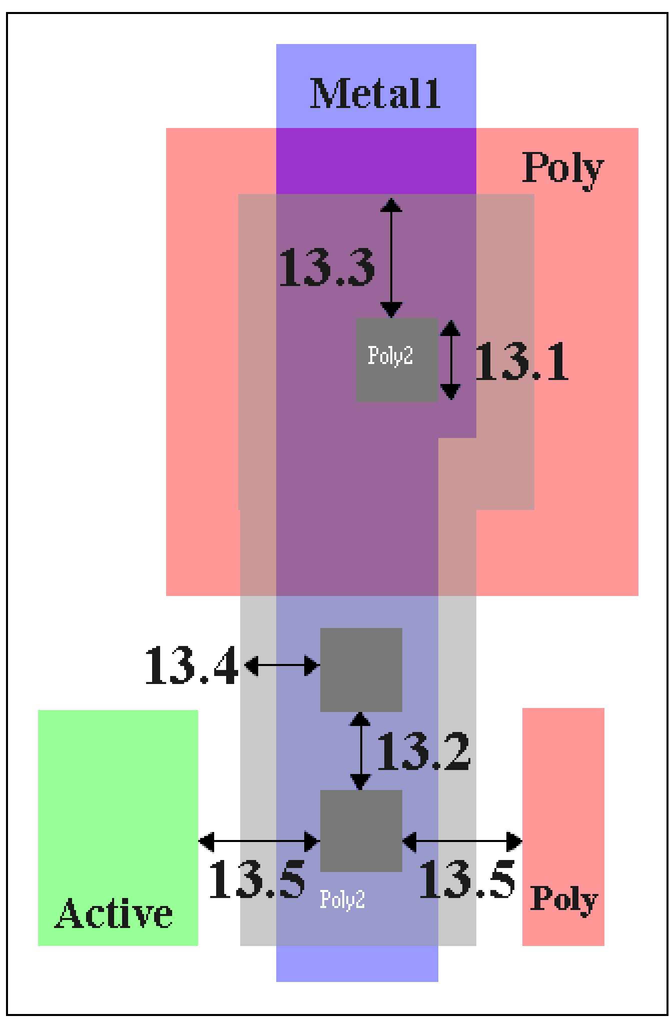


SCMOS Layout Rules - Poly2 Contact

The poly2 is contacted through the standard contact layer, similar to the first poly. The overlap numbers are larger, however.

Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
13.1	Exact contact size	2 x 2	2 x 2	n/a
13.2	Minimum contact spacing	2	3	n/a
13.3	Minimum electrode overlap (on capacitor)	3	3	n/a
13.4	Minimum electrode overlap (not on capacitor)	2	2	n/a
13.5	Minimum spacing to poly or active	3	3	n/a

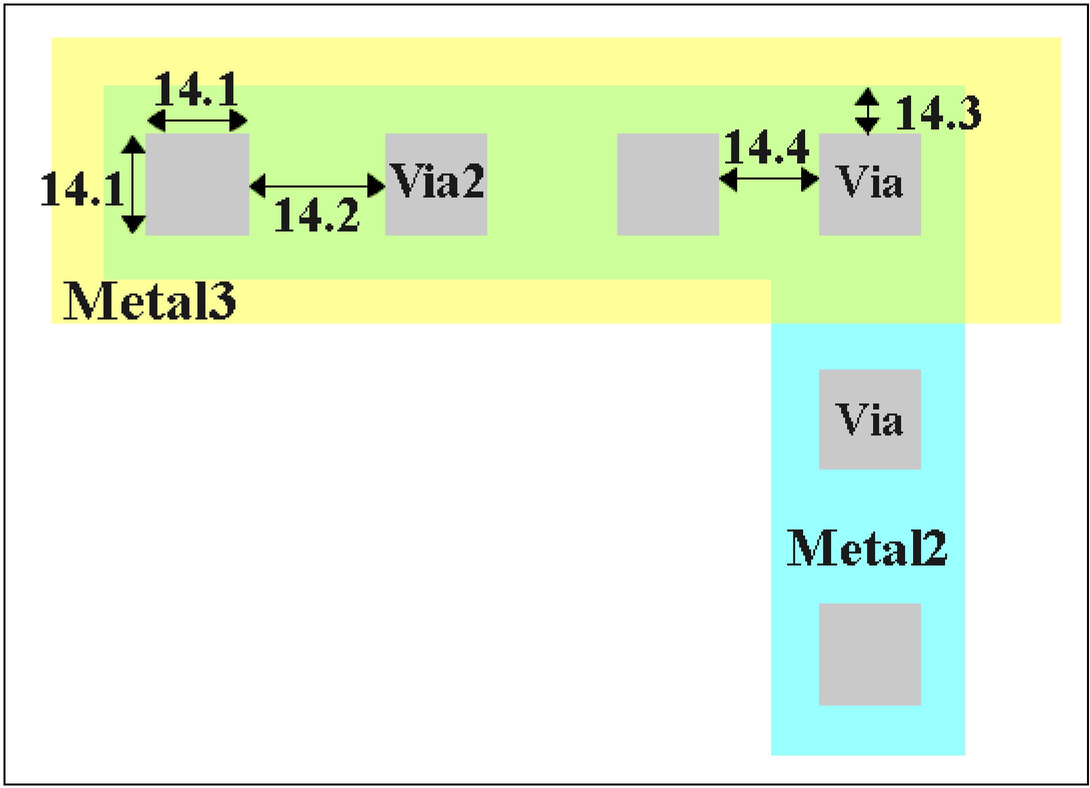

Metal1
Poly
13.3
Poly2
13.1
13.4
13.2
13.5
13.5
Poly2
Active
Poly

Note: Only Rules 1 through 11 are applicable to the AMI 0.5u process

SCMOS Layout Rules - Via2

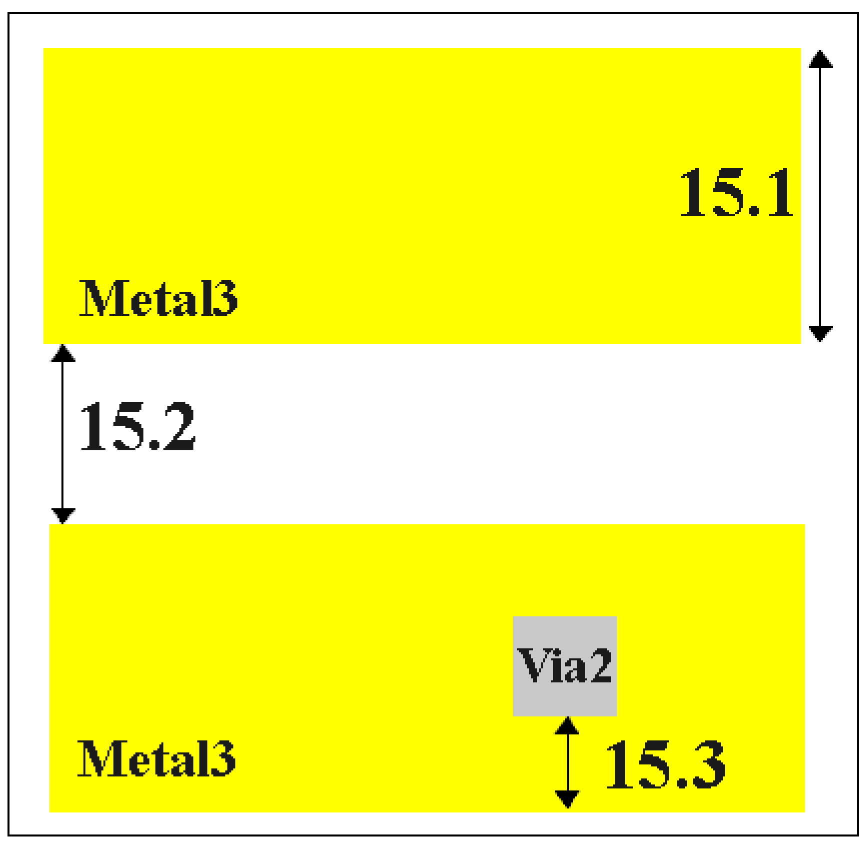
Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
14.1	Exact size	2x2	2x2	n/a	2x2	2x2	3x3
14.2	Minimum spacing	3	3	n/a	3	3	3
14.3	Minimum overlap by metal2	1	1	n/a	1	1	1
14.4	Minimum spacing to via1 for technology codes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3ME, SCN3MLC)	2	2	n/a	2	2	n/a
14.5	Via2 may be placed over contact						



SCMOS Layout Rules - Metal3

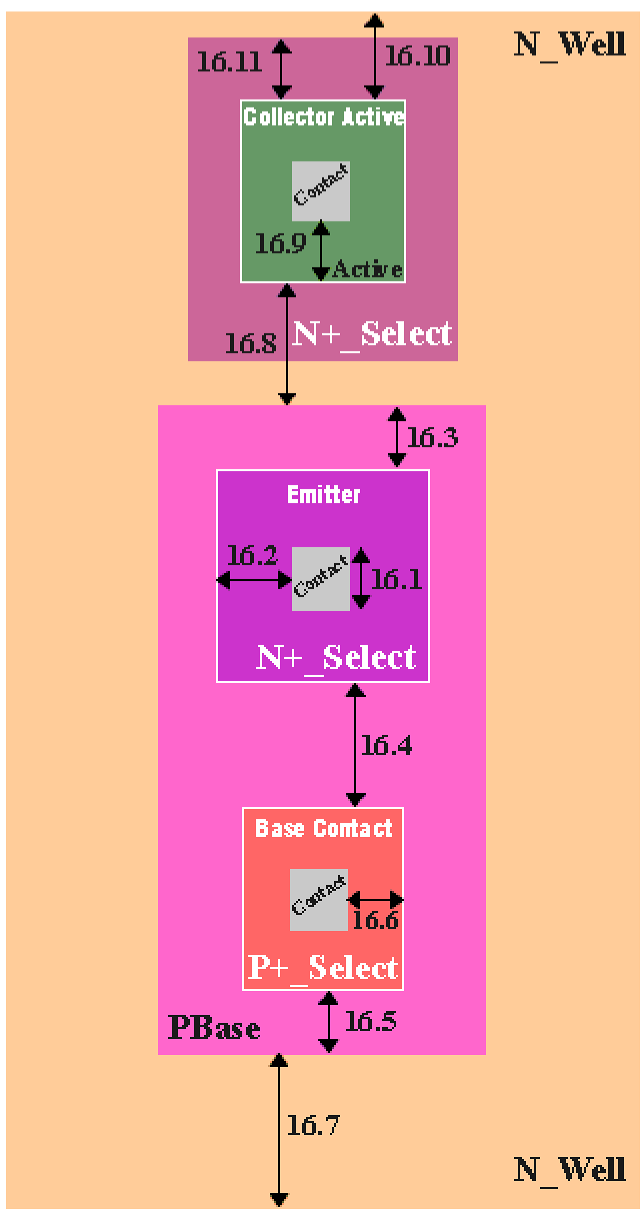
Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
15.1	Minimum width	6	5	n/a	3	3	3
15.2	Minimum spacing to metal3	4	3	n/a	3	3	4
15.3	Minimum overlap of via2	2	2	n/a	1	1	1
15.4	Minimum spacing when either metal line is wider than 10 lambda	8	6	n/a	6	6	8



SCMOS Layout Rules - Pbase (Analog Option)

The pbase layer is an active area that is implanted with the pbase implant to form the base of the NPN bipolar transistor. The base contact is enclosed in p-select. The emitter is an n-select region within (and on top of) the base. The entire pbase sits in an *n*-well that is the collector. The collector contact is a well contact, but the overlaps are larger. Active should not be used inside of pbase.

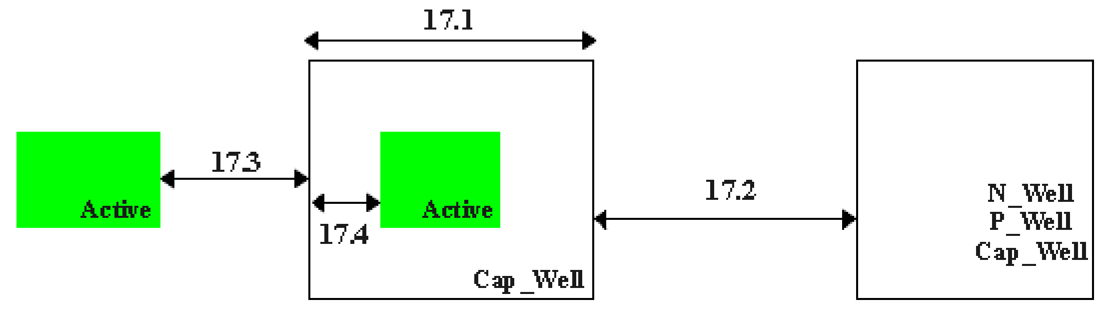
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
16.1	All active contact	2 x 2	n/a	n/a
16.2	Minimum emitter select overlap of contact	3	n/a	n/a
16.3	Minimum pbase overlap of emitter select	2	n/a	n/a
16.4	Minimum spacing between emitter select and base select	4	n/a	n/a
16.5	Minimum pbase overlap of base select	2	n/a	n/a
16.6	Minimum base select overlap of contact	2	n/a	n/a
16.7	Minimum nwell overlap of pbase	6	n/a	n/a
16.8	Minimum spacing between pbase and collector active	4	n/a	n/a
16.9	Minimum collector active overlap of contact	2	n/a	n/a
16.10	Minimum nwell overlap of collector active	3	n/a	n/a
16.11	Minimum select overlap of collector active	2	n/a	n/a


N_Well
16.11
16.10
Collector Active
Contact
16.9
Active
16.8
N+_Select
16.3
Emitter
16.2
Contact
16.1
N+_Select
16.4
Base Contact
Contact
16.6
P+_Select
PBase
16.5
16.7
N_Well

SCMOS Layout Rules - Capacitor Well

The capacitor well described in this and the next rule only apply to SCN3MLC and SCN3MLC_SUBM technology codes manufactured on an Agilent/HP AMOS14TB run.

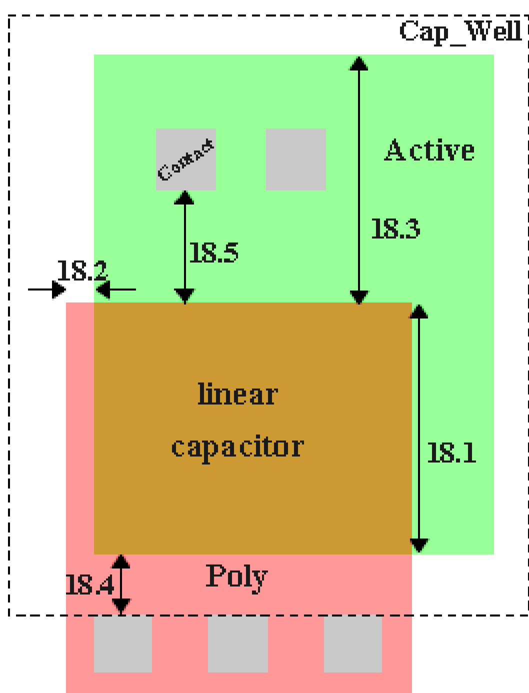
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
17.1	Minimum width	10	12	n/a
17.2	Minimum spacing	9	18	n/a
17.3	Minimum spacing to external active	5	6	n/a
17.4	Minimum overlap of active	5	6	n/a



SCMOS Layout Rules - Linear Capacitor (Linear Capacitor Option)

These rules illustrate the construction of a linear capacitor in a capacitor well. The capacitor itself is the region of overlapped poly and active. The active area is electrically connected to the cap well

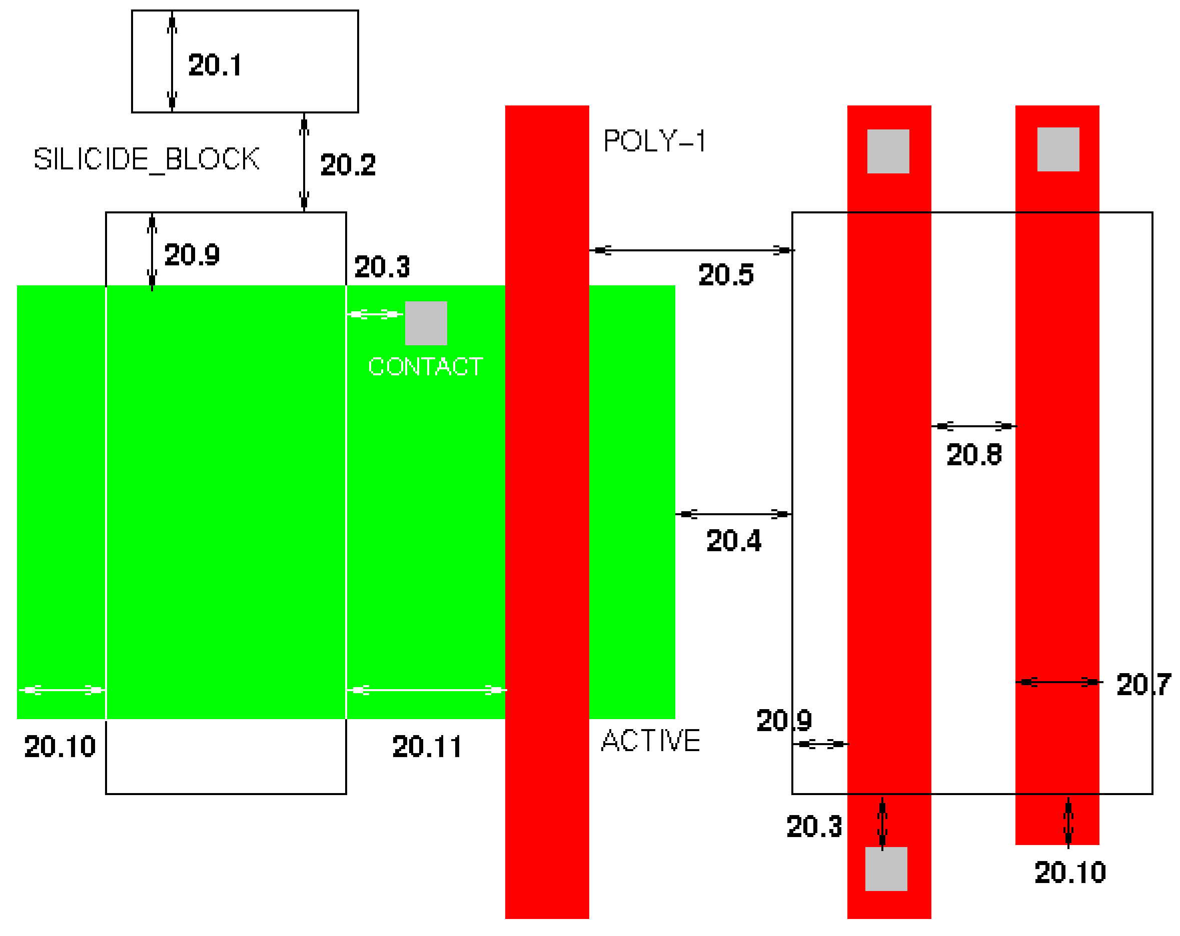
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
18.1	Minimum width	3	3	n/a
18.2	Minimum poly extension of active	2	2	n/a
18.3	Minimum active overlap of poly	3	3	n/a
18.4	Minimum poly contact to active	2	2	n/a
18.5	Minimum active contact to poly	6	6	n/a


Cap_Well
Contact
Active
18.3
18.5
18.2
linear
capacitor
18.1
18.4
Poly

SCMOS Layout Rules - Silicide Block

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
20.1	Minimum SB width	4	4	4
20.2	Minimum SB spacing	4	4	4
20.3	Minimum spacing, SB to contact (no contacts allowed inside SB)	2	2	2
20.4	Minimum spacing, SB to external active	2	2	2
20.5	Minimum spacing, SB to external poly	2	2	2
20.6	Resistor is poly inside SB; poly ends stick out for contacts the entire resistor must be outside well and over field			
20.7	Minimum poly width in resistor	5	5	5
20.8	Minimum spacing of poly resistors (in a single SB region)	7	7	7
20.9	Minimum SB overlap of poly or active	2	2	2
20.10	Minimum poly or active overlap of SB	3	3	3
20.11	Minimum spacing, SB to poly (in a single active region)	3	5	5

NOTE: Some processes do not support both silicide block over active and silicide block over poly. Refer to the individual process description pages.

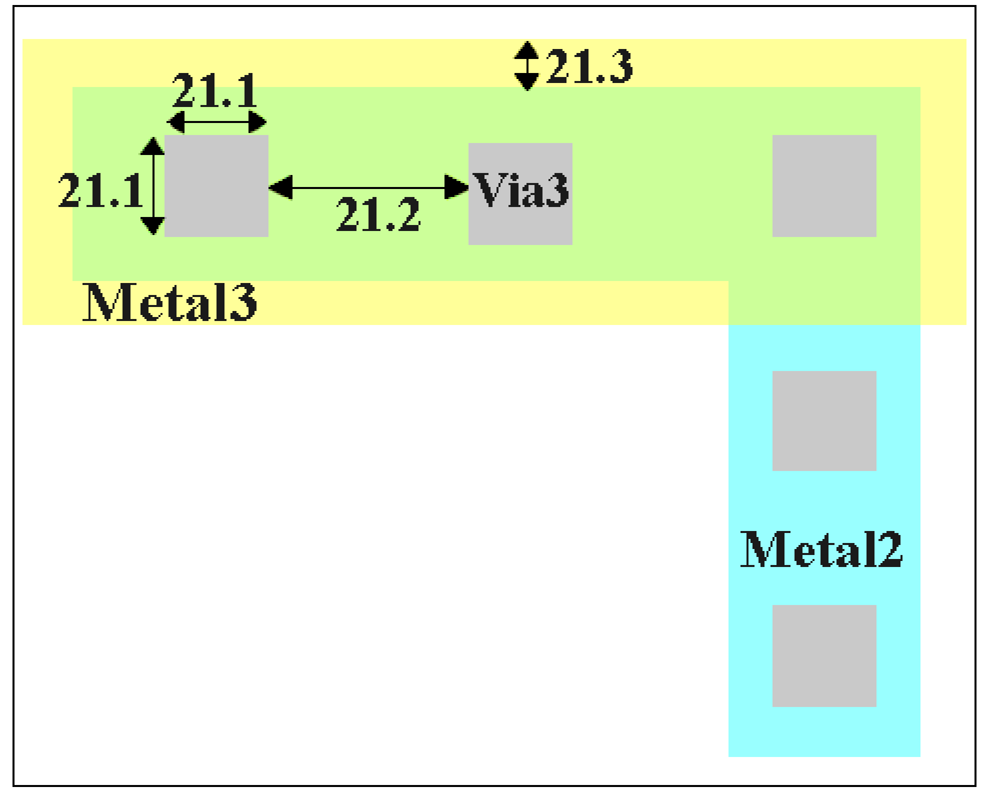

20.1
SILICIDE_BLOCK
20.2
POLY-1
20.9
20.3
20.5
CONTACT
20.8
20.4
20.7
20.9
20.10
20.11
ACTIVE
20.3
20.10

SCMOS Layout Rules - Via3

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

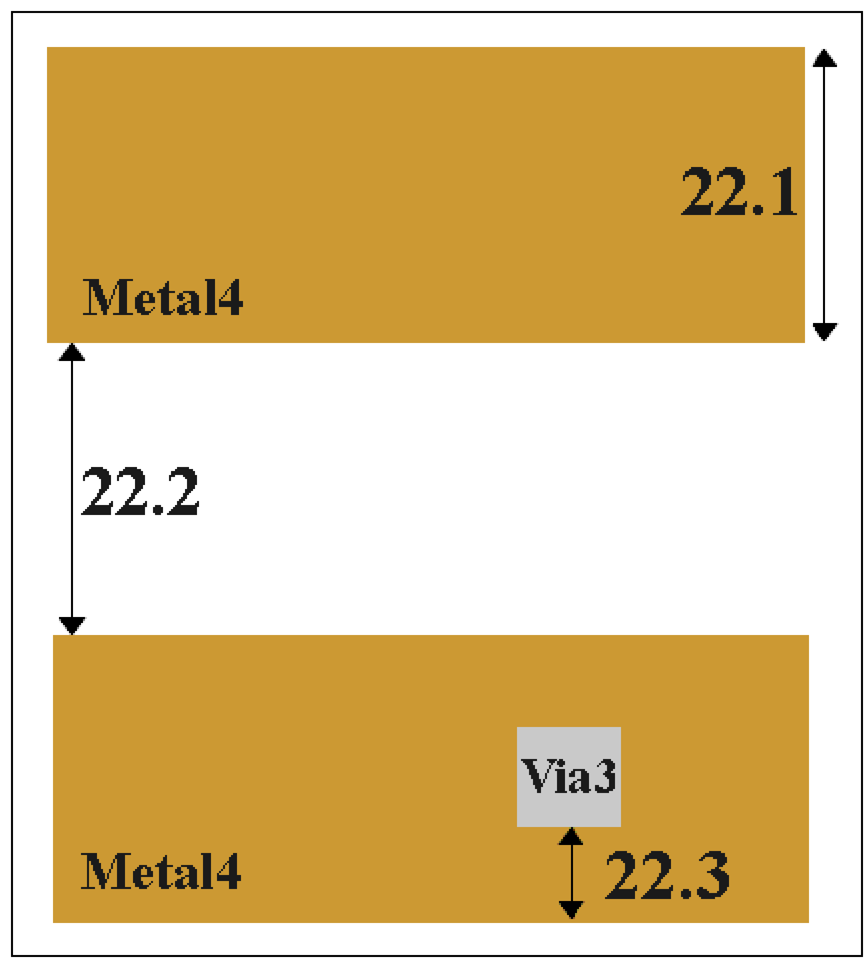
Rule	Description	Lambda					
		4 metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
21.1	Exact size	2x2	2x2	n/a	n/a	2x2	3x3
21.2	Minimum spacing	3	3 *	n/a	n/a	3	3
21.3	Minimum overlap by Metal3	1	1	n/a	n/a	1	1

*** Exception: Use lambda=4 for rule 21.2 only when using SCN4M_SUBM for Agilent/HP GMOS10QA 0.35 micron process**



SCMOS Layout Rules - Metal4

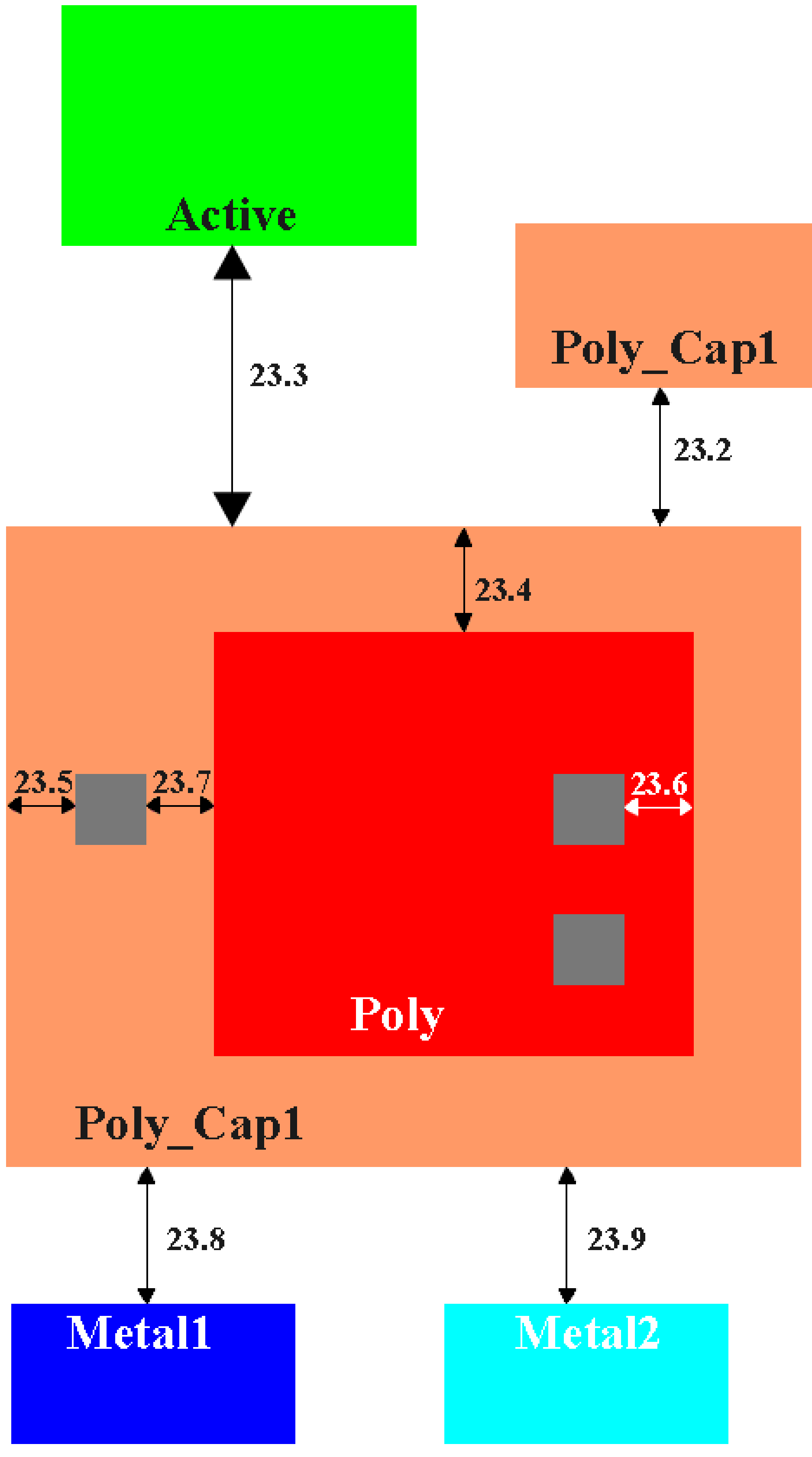
Rule	Description	Lambda					
		4 Metal Process			5+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
22.1	METAL4 width	6	6	n/a	n/a	3	3
22.2	METAL4 space	6	6	n/a	n/a	3	4
22.3	METAL4 overlap of VIA3	2	2	n/a	n/a	1	1
22.4	Minimum spacing when either metal line is wider than 10 lambda	12	12	n/a	n/a	6	8



SCMOS Layout Rules - SCNPC with POLY_CAP

The two plates of an SCNPC capacitor are POLY and POLY_CAP1. The POLY_CAP1 must surround the POLY everywhere; the area of the capacitor is the area of the POLY. POLY is physically on top of POLY_CAP1, so that contact to the POLY_CAP1 must be made in the region where it extends beyond the POLY. The capacitor may be in the well or the substrate, but may not straddle a well boundary. The only metal that may cross over a capacitor is the connecting METAL1 wires.

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
23.1	Minimum POLY_CAP1 width. This is lithographic; the minimum to build a real capacitor is greater than 12 lambda	8	n/a	n/a
23.2	Minimum spacing, POLY_CAP1 to POLY_CAP1 (neighboring capacitor)	4	n/a	n/a
23.3	Minimum spacing, POLY_CAP1 to ACTIVE (all capacitors must be over field)	8	n/a	n/a
23.4	Minimum overlap, POLY_CAP1 over POLY	3	n/a	n/a
23.5	Minimum overlap, POLY_CAP1 over CONTACT	2	n/a	n/a
23.6	Minimum overlap, POLY over CONTACT (in a capacitor only; still 1 lambda elsewhere)	2	n/a	n/a
23.7	Minimum spacing, POLY to CONTACT-to-POLY_CAP1	2	n/a	n/a
23.8	Minimum spacing, unrelated METAL1 to POLY_CAP1	4	n/a	n/a
23.9	Minimum spacing, METAL2 to POLY_CAP1	2	n/a	n/a


Active
23.3
Poly_Cap1
23.2
23.4
23.5
23.7
23.6
Poly
Poly_Cap1
23.8
23.9
Metal1
Metal2

SCMOS Layout Rules - Thick Active

THICK_ACTIVE is a layer used for those processes offering two different thicknesses of gate oxide (typically for the layout of transistors that operate at two different voltage levels). The ACTIVE layer is used to delineate all the active areas, regardless of gate oxide thickness. THICK_ACTIVE is used to mark those ACTIVE areas that will have the thicker gate oxide; ACTIVE areas outside THICK_ACTIVE will have the thinner gate oxide. THICK_ACTIVE by itself (not covering any ACTIVE polygon) is meaningless.

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
24.1	Minimum width	4	4	4
24.2	Minimum spacing	4	4	4
24.3	Minimum ACTIVE overlap	4	4	4
24.4	Minimum space to external ACTIVE	4	4	4
24.5	Minimum poly width in a THICK_ACTIVE gate	3	3	3
24.6	Every ACTIVE region is either entirely inside THICK_ACTIVE or entirely outside THICK_ACTIVE			

SCMOS Layout Rules - Via4
(SUBM and DEEP)

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		5 Metal Process			6+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
25.1	Exact size	n/a	2x2	3x3	n/a	2x2	3x3
25.2	Minimum spacing	n/a	3	3	n/a	3	3
25.3	Minimum overlap by Metal4	n/a	1	1	n/a	1	1

SCMOS Layout Rules - Metal5
(SUBM and DEEP)

Any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer.

Rule	Description	Lambda					
		5 Metal Process			6+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
26.1	Minimum width	n/a	4	4	n/a	3	3
26.2	Minimum spacing to Metal5	n/a	4	4	n/a	3	4
26.3	Minimum overlap of Via4	n/a	1	2	n/a	1	1
26.4	Minimum spacing when either metal line is wider than 10 lambda	n/a	8	8	n/a	6	8

SCMOS Layout Rules - High Res

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
27.1	Minimum HR width	4	4	n/a
27.2	Minimum HR spacing	4	4	n/a
27.3	Minimum spacing, HR to contact (no contacts allowed inside HR)	2	2	n/a
27.4	Minimum spacing, HR to external active	2	2	n/a
27.5	Minimum spacing, HR to external poly2	2	2	n/a
27.6	Resistor is poly2 inside HR; poly2 ends stick out for contacts, the entire resistor must be outside well and over field			
27.7	Minimum poly2 width in resistor	5	5	n/a
27.8	Minimum spacing of poly2 resistors (in a single HR region)	7	7	n/a
27.9	Minimum HR overlap of poly2	2	2	n/a

SCMOS Layout Rules - CAP_TOP_METAL for SCMOS_DEEP (and SUBM)

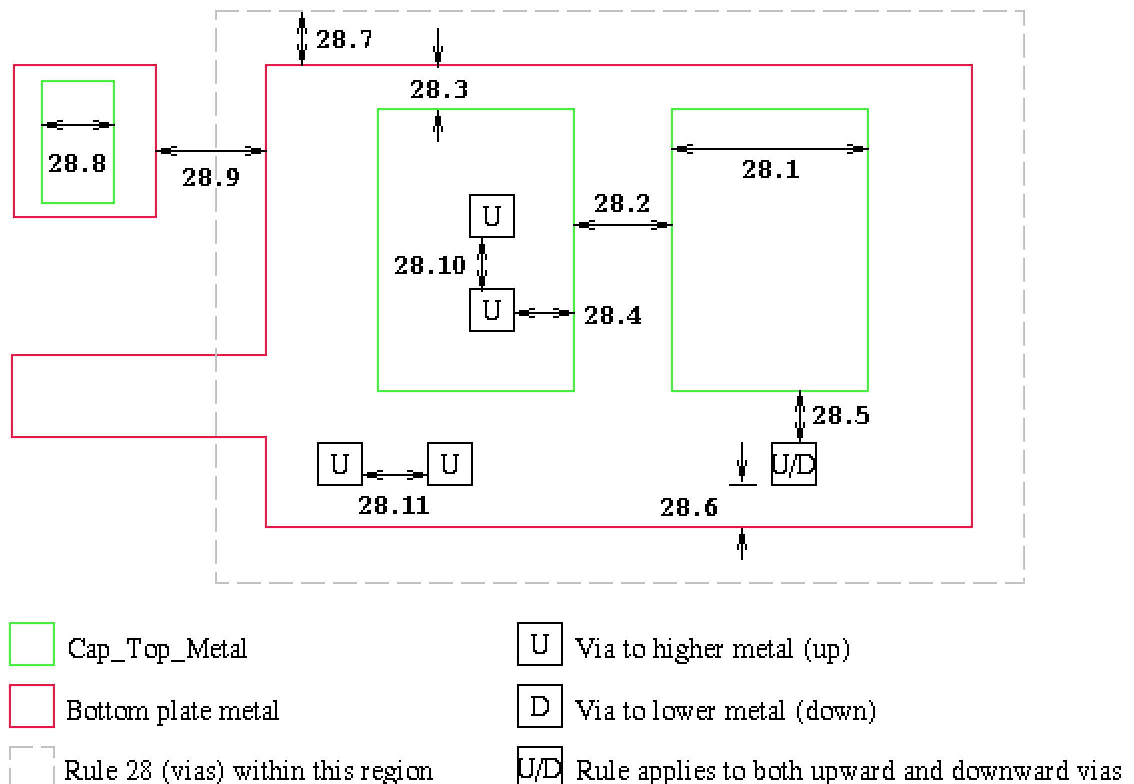
The CAP_TOP_METAL layer is used exclusively for the construction of metal-to-metal capacitors. The bottom plate of the capacitor is one of the regular metal layers, as specified below. CAP_TOP_METAL is the upper plate of the capacitor; it is sandwiched physically between the bottom plate metal and the next metal layer above, with a thin dielectric between the bottom plate and the upper (CAP_TOP_METAL) plate.

The CAP_TOP_METAL can only be contacted from the metal above; the bottom plate metal can be contacted from below or above (subject, in either case, to rule 28.5), and/or by bottom metal extending outside of the capacitor region (rule 28.7). Use of all (legal) upward vias within that region should be maximized. CAP_TOP_METAL must always be contained entirely within the bottom plate metal.

Process	Bottom Plate	Top Plate	Top Plate Contact
TSMC_025	METAL4	CAP_TOP_METAL	VIA4 and METAL5
TSMC_018	METAL5	CAP_TOP_METAL	VIA5 and METAL6

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
28.1	Minimum Width, Capacitor	n/a	40	45
28.2	Minimum Spacing (2 capacitors sharing a single bottom plate)	n/a	12	14
28.3	Minimum bottom metal overlap (including dummy shapes)	n/a	4	5
28.4	Minimum overlap of via	n/a	3	3
28.5	Minimum spacing to bottom metal via	n/a	4	5
28.6	Minimum bottom metal overlap of its via	n/a	2	2
28.7	Rule applicability region extends beyond bottom plate	n/a	25	25
28.8	Minimum width, dummy shapes (having no vias)	n/a	4	5
28.9	Minimum bottom plate to other bottom plate metal	n/a	8	9
28.10	Minimum via separation, on CAP_TOP_METAL	n/a	20	23
28.11	Minimum (upward) via separation on bottom metal	n/a	40	45
28.12	Maximum CAP_TOP_METAL width and length	n/a	30 um	
28.13	Maximum bottom metal plate width and length	n/a	35 um	

28.14	No vias from bottom plate downward, directly under top plate CAP_TOP_METAL; dummy metal shapes under capacitor region, discouraged.
28.15	No active or passive circuitry under capacitor region



SCMOS Layout Rules - Via5 (SUBM and DEEP)

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda		
		6 Metal Process		
		SCMOS	SUBM	DEEP
29.1	Exact size	n/a	3 x 3	4 x 4
29.2	Minimum spacing	n/a	4	4
29.3	Minimum overlap by Metal5	n/a	1	1

SCMOS Layout Rules - Metal6 (SUBM and DEEP)

Any designer using the SCMOS rules who wants the TSMC Thick_Top_Metal must draw the top metal to comply with the TSMC rules for that layer.

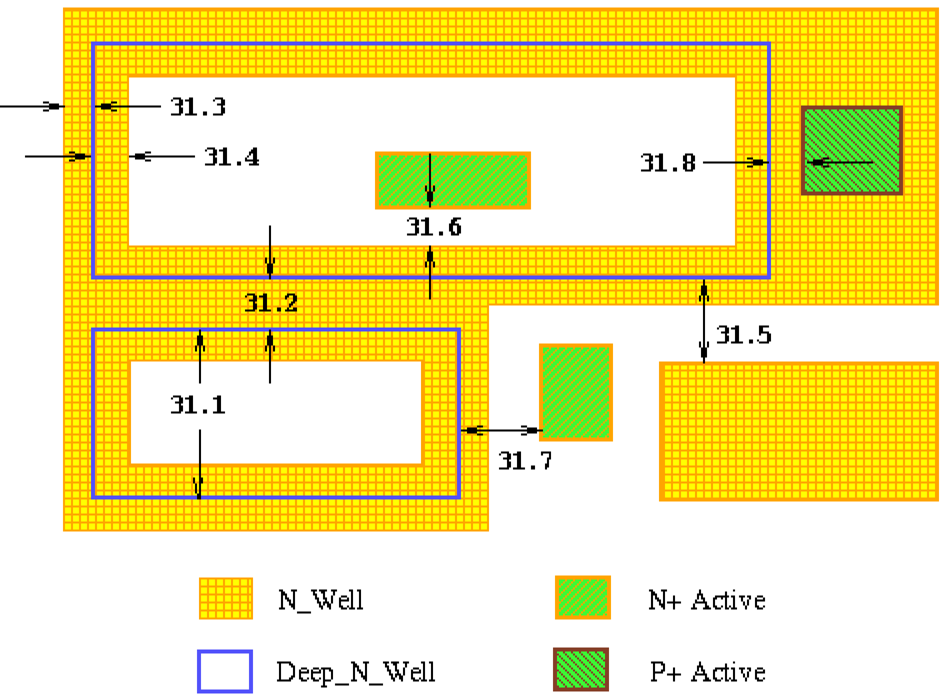
Rule	Description	Lambda		
		6 Metal Process		
		SCMOS	SUBM	DEEP
30.1	Minimum width	n/a	5	5
30.2	Minimum spacing to Metal6	n/a	5	5
30.3	Minimum overlap of Via5	n/a	1	2
30.4	Minimum spacing when either metal line is wider than 10 lambda	n/a	10	10

SCMOS Layout Rules - DEEP_N_WELL for SCMOS_DEEP (and SUBM)

The DEEP_N_WELL layer provides access to the DNW layer in the TSMC 0.18 and 0.25 processes. This provides a layering sometimes called "triple-well" in which an n-well sits in the p-substrate, and then a p-well sits fully inside of the n-well; it is then possible to construct NMOS devices inside of that isolated p-well. The isolated p-well is surrounded by a fence of standard N_WELL (around its periphery), and by DEEP_N_WELL underneath. The N_WELL fence makes direct electrical contact with the DEEP_N_WELL plate beneath it.

DEEP_N_WELL is available in technology codes SCN5M_SUBM, SCN5M_DEEP, SCN6M_SUBM and SCN6M_DEEP but only where these are to be fabricated on TSMC foundry runs. To gain a better understanding of this layer, the TSMC vendor-rule design rule documentation should be studied.

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
31.1	Minimum Width, Deep_N_Well	n/a	30	34
31.2	Minimum Spacing, Deep_N_Well to Deep_N_Well	n/a	50	56
31.3	Minimum extension, N_Well beyond Deep_N_Well edge	n/a	15	17
31.4	Minimum overlap, N_Well over Deep_N_Well edge	n/a	20	23
31.5	Minimum spacing, Deep_N_Well to unrelated N_Well	n/a	35	39
31.6	Minimum spacing, N+Active in isolated P-well, to N_Well	n/a	5	6
31.7	Minimum spacing, external N+Active to Deep_N_Well	n/a	30	34
31.8	Minimum spacing, P+Active in N_Well to its Deep_N_Well	n/a	10	13


31.3
31.4
31.8
31.6
31.2
31.5
31.1
31.7
N_Well
N+ Active
Deep_N_Well
P+ Active

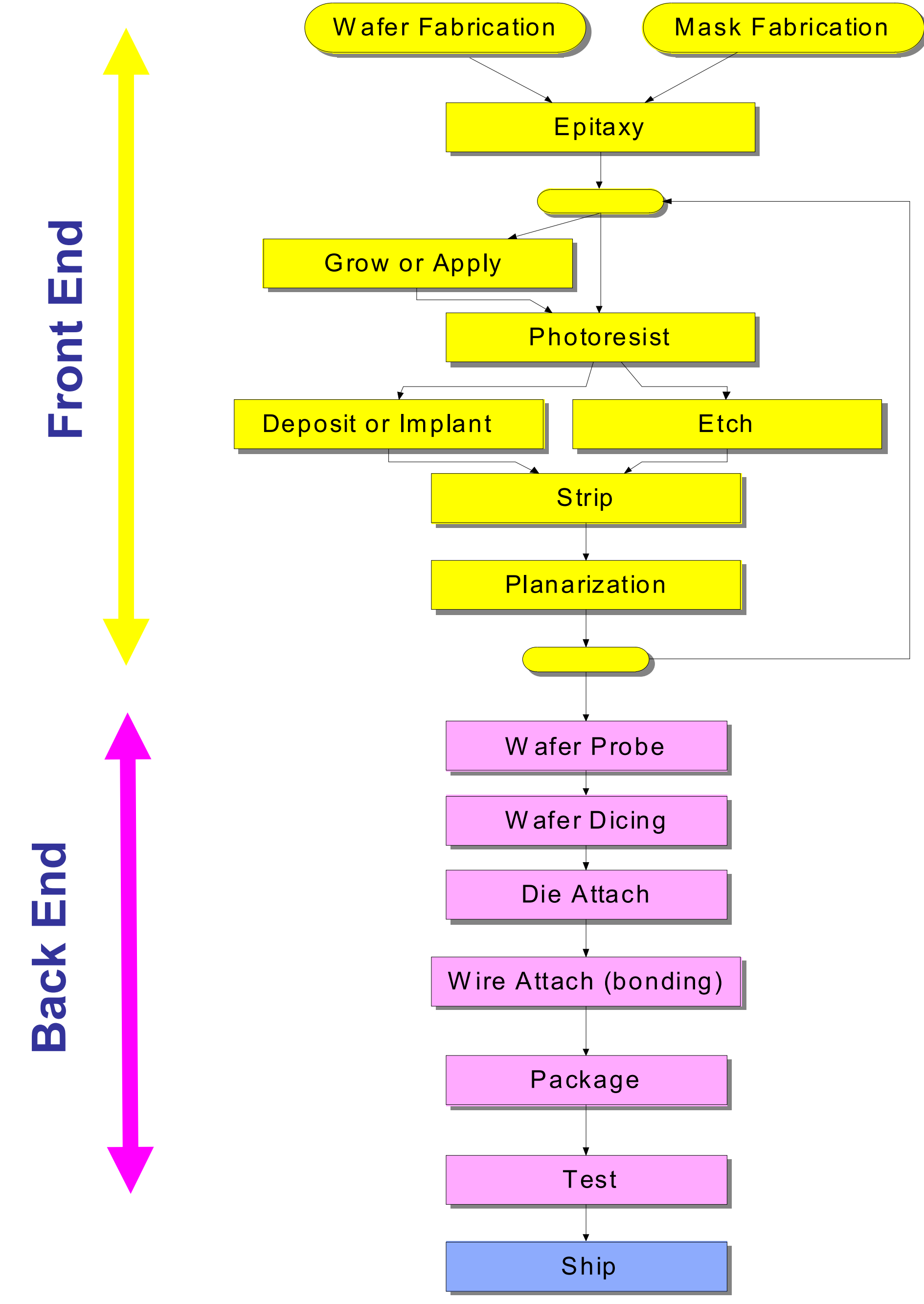
IC Fabrication Technology

See Chapter 1 and 3 of WH
or Chapter 2 GAS for details

IC Fabrication Technology

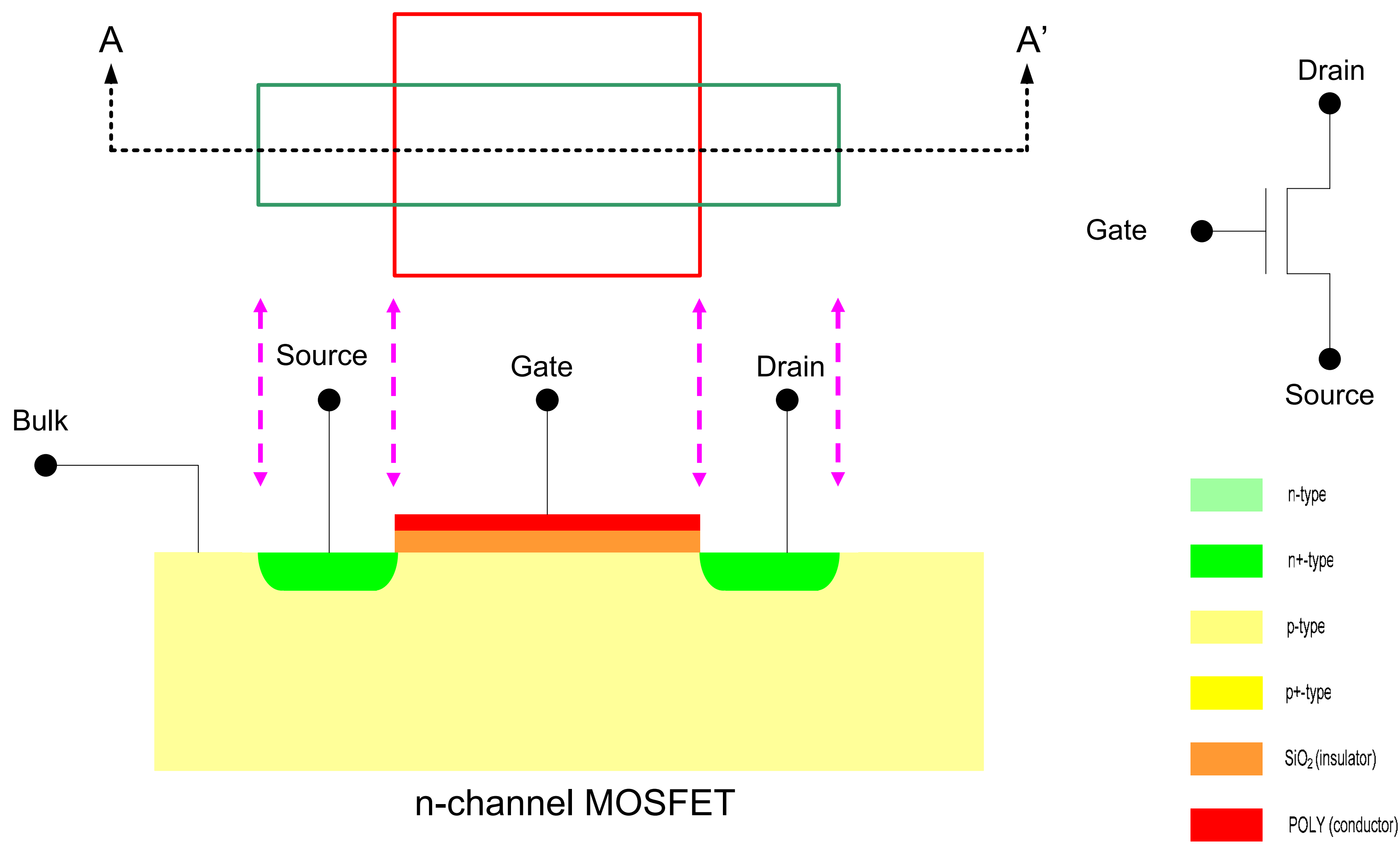
- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Generic Process Flow



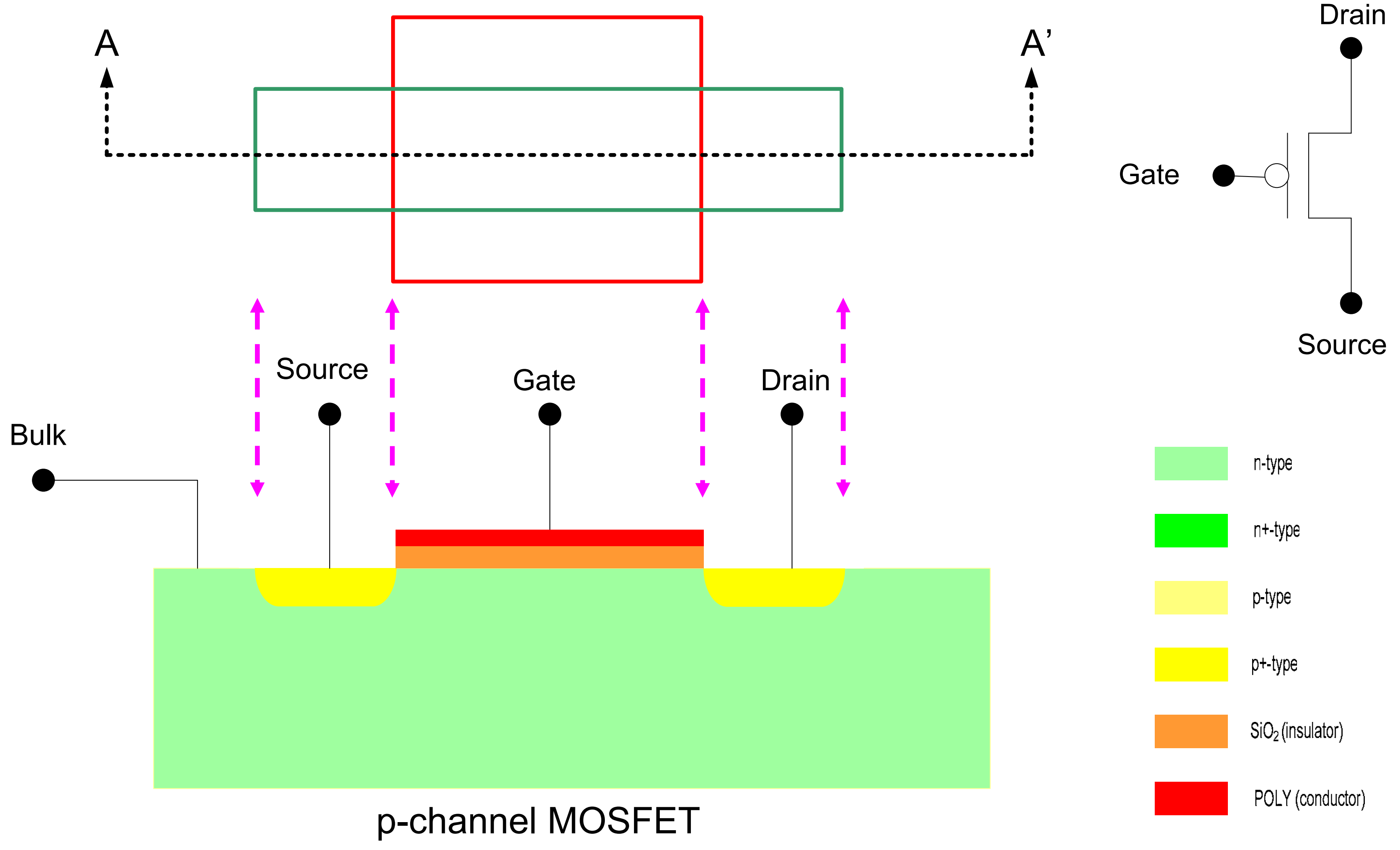
Review

MOS Transistor



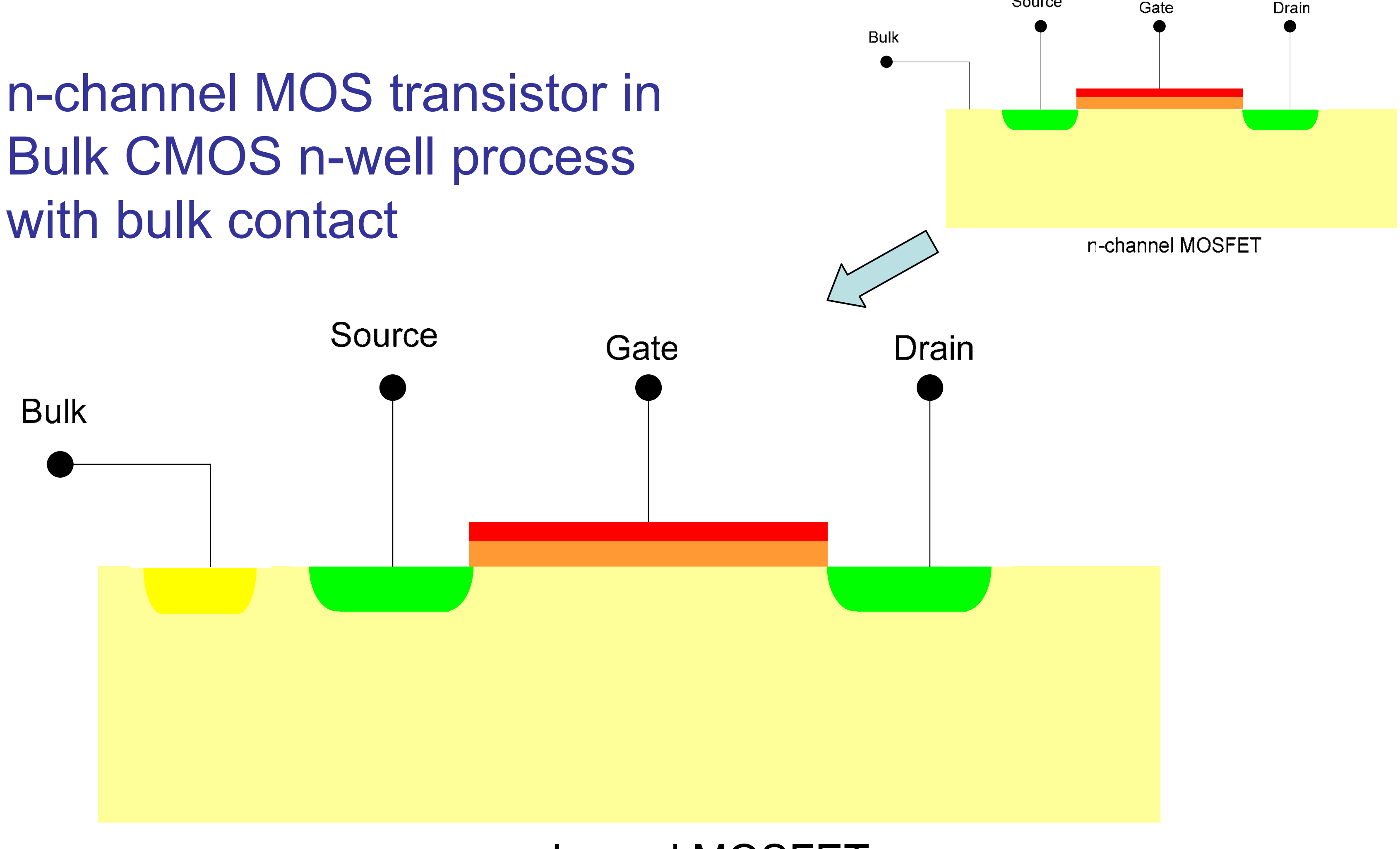
Review

MOS Transistor



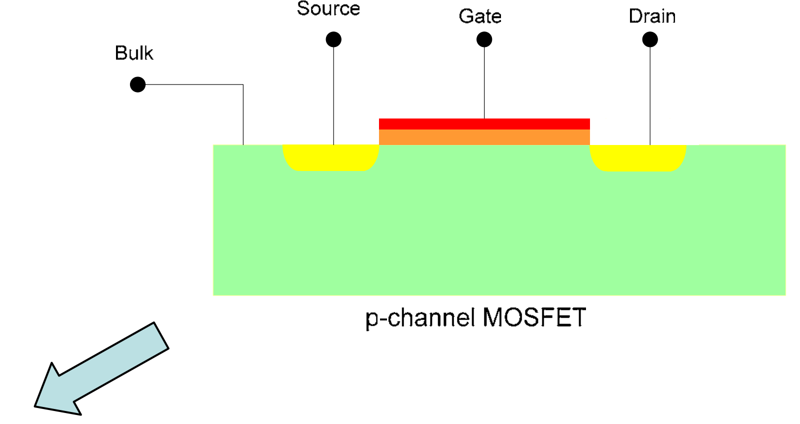
MOS Transistor

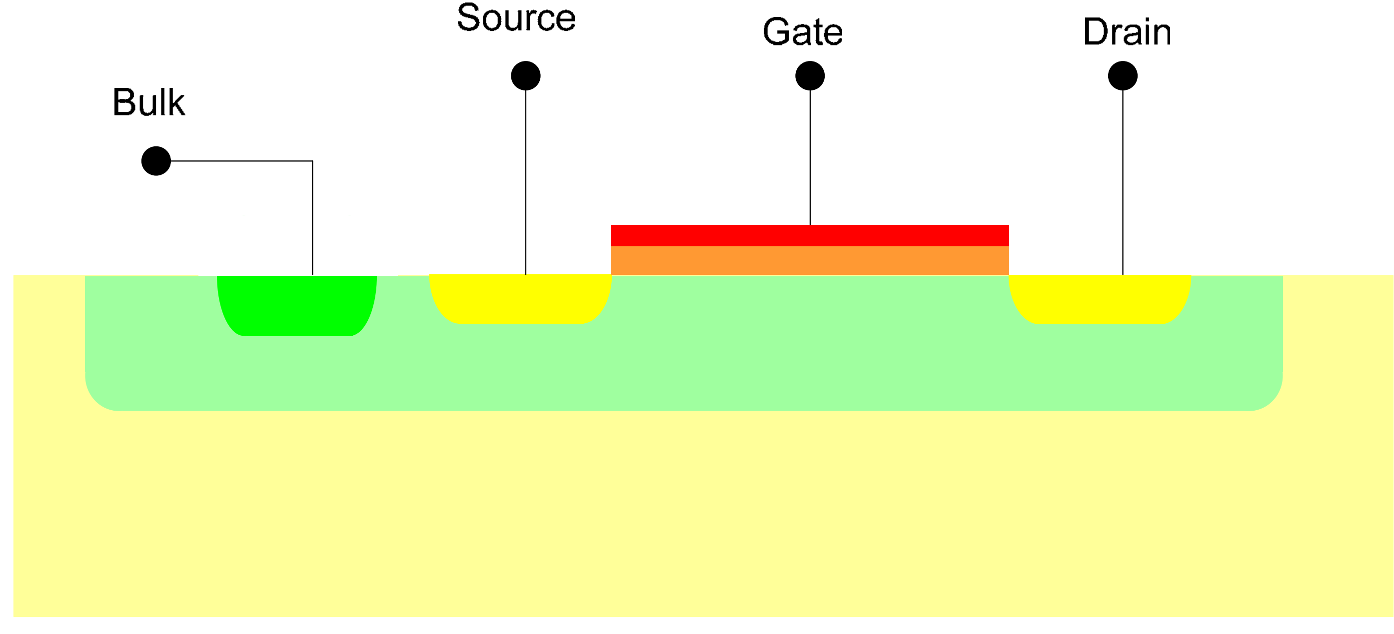
n-channel MOS transistor in Bulk CMOS n-well process with bulk contact



MOS Transistor

p-channel MOS transistor in
Bulk CMOS n-well process
with bulk contact and well (tub)

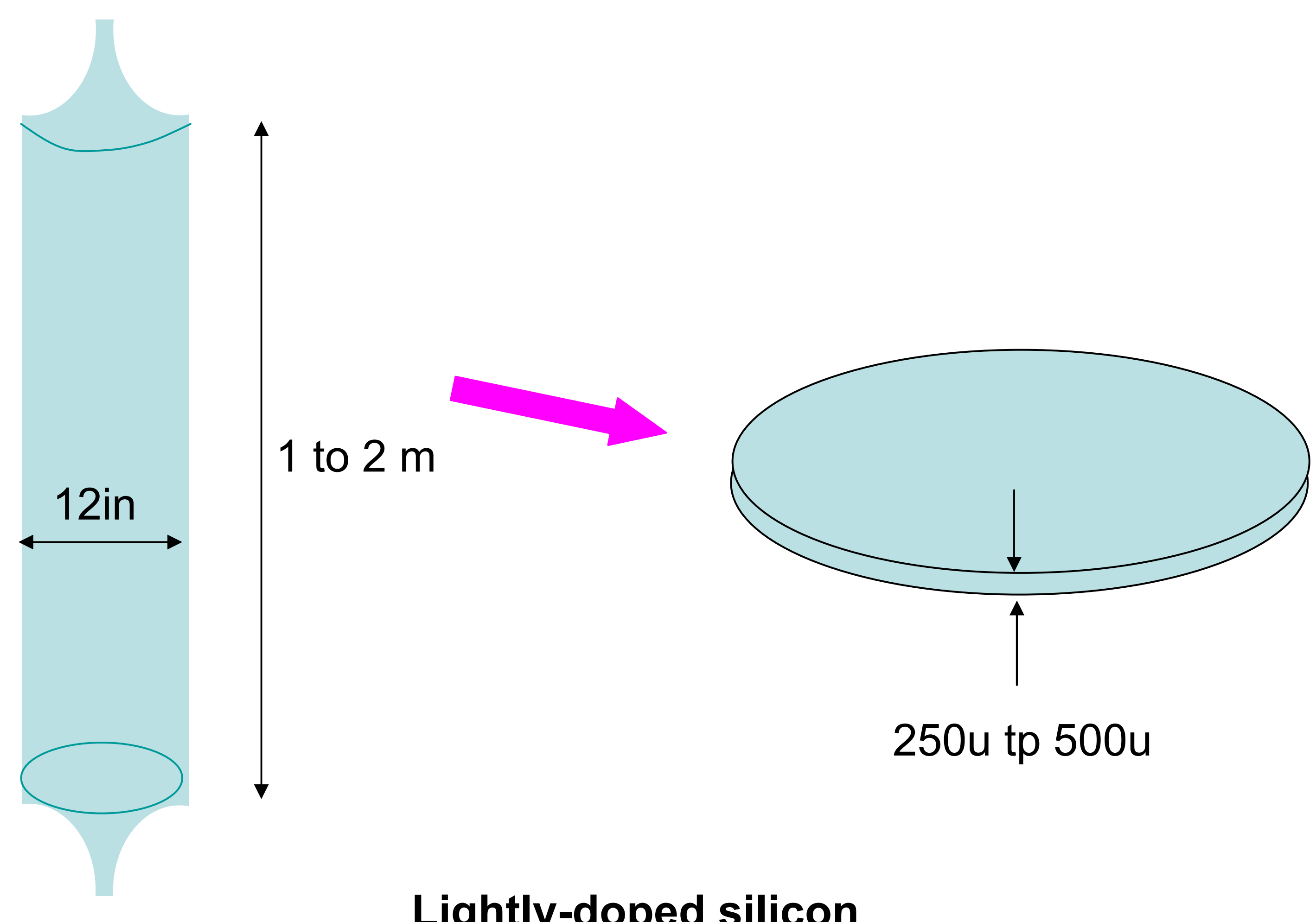




Crystal Preparation

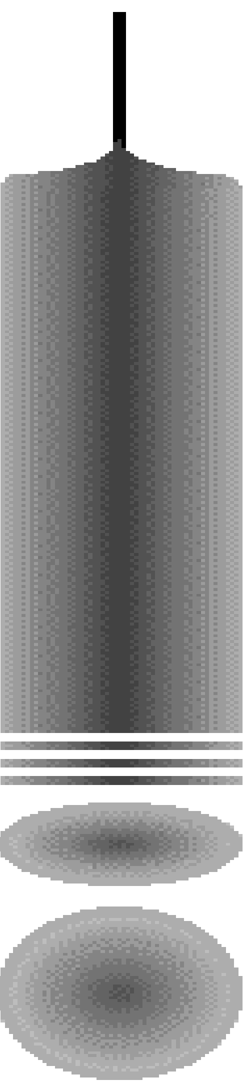
- Large crystal is grown (pulled)
  - 12 inches in diameter and 1 to 2 m long
  - Sliced to 250u to 500u thick
    - Prefer to be much thinner but thickness needed for mechanical integrity
  - 4 to 8 cm/hr pull rate
  - T=1430 ^{o}C
- Crystal is sliced to form wafers
- Cost for 12" wafer around $200
- 5 companies provide 90% of worlds wafers
- Somewhere around 400,000 12in wafers/month

Crystal Preparation



Lightly-doped silicon
Excellent crystalline structure

Crystal Preparation

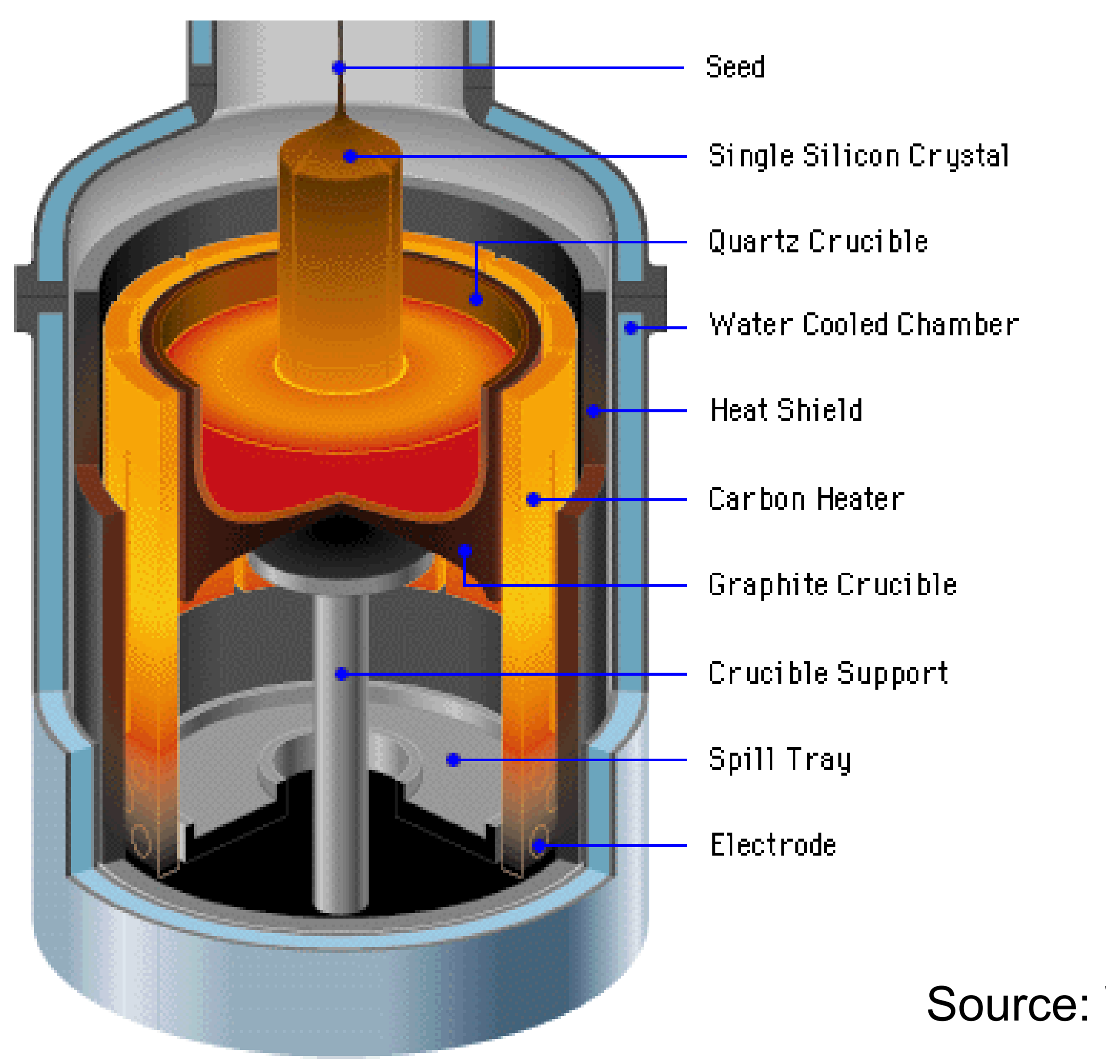


From www.infras.com

Crystal Preparation

Source: WEB

Crystal Preparation



Source: WEB

Crystal Preparation

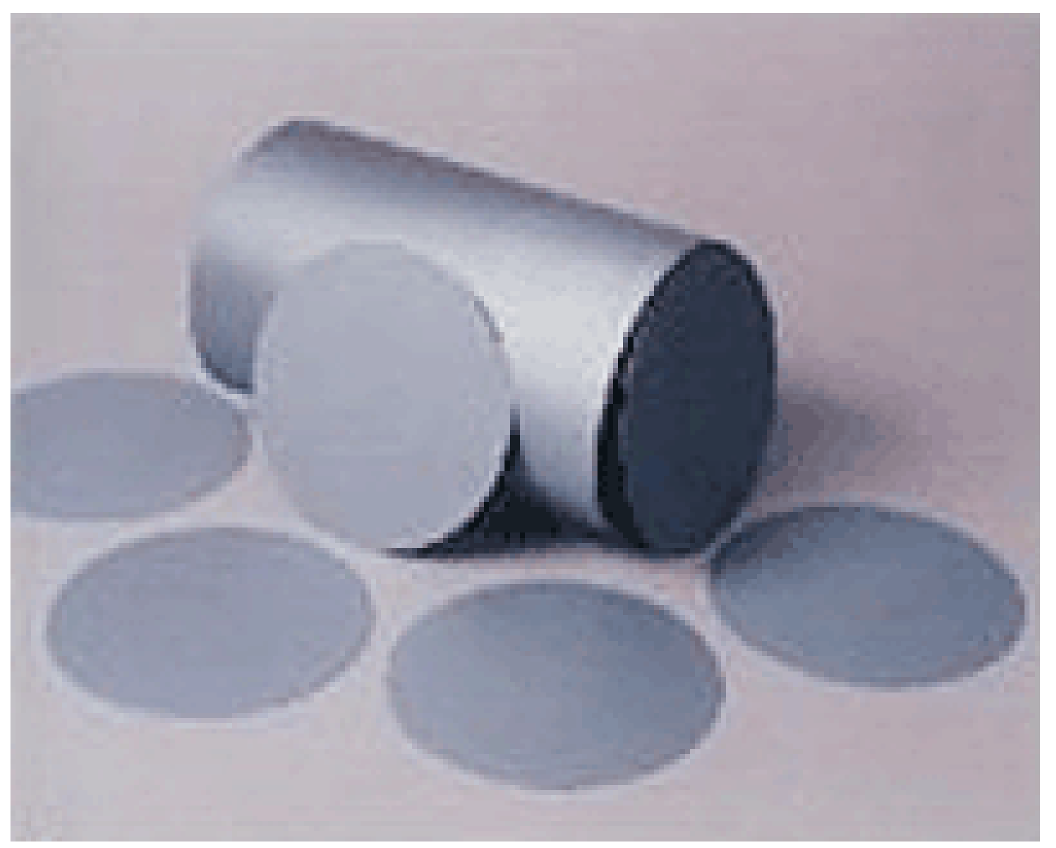
Source: WEB

Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB

Crystal Preparation



Source: WEB