EE 434 Name ____________________
Exam 1
Fall 2002

Instructions. Students may bring two 8.5 x 11 pages of notes to this exam. On the exam, there are a set of short questions and 4 problems. All questions are worth 2 points and each problem is worth 20 points. All work and answers are to appear on this exam sheet. Attach additional sheets only if you run out of room on the examination itself.

Questions

1. What is the difference between Polysilicon and the silicon used to form the substrate of a wafer.

2. What are the two major reasons the continued scaling down of feature sizes we have seen in semiconductor processes for the past two decades can not continue at the same pace for the next two decades.

3. What is the major purpose of the n+ buried collector in a typical bipolar process.

4. Describe the difference between a lateral and a vertical bipolar transistor.

5. Give a qualitative discussion about why the β of a vertical transistor is typically much larger than the β of a lateral transistor.

6. What is the major reason that contacts to a gate of a MOS transistor are made over field oxide rather than over thin oxide.

7. In a general 3-terminal device, how many small signal parameters are needed in the small-signal model.

8. What is the purpose of a bonding pad?

9. How does the area of a minimum sized MOS transistor compare to that of a minimum sized bipolar transistor if they are both fabricated in processes with about the same lithography capabilities?

10. What is the approximate cost of adding a single MOS transistor to a large integrated circuit in a typical CMOS process?

Problem 1 Assume an integrated circuit designed in a .25μ process is comprised of 10,000 minimum-sized transistors (each transistor is 0.25μ on a side) and that the average interconnect area for the circuit is 9 times the actual gate area. Assume further that the device has 24 bonding pads and each bonding pad, including spacing between the pads, is 120μ x 120μ. If this device is fabricated on an 8" wafer that costs $1000 to produce,

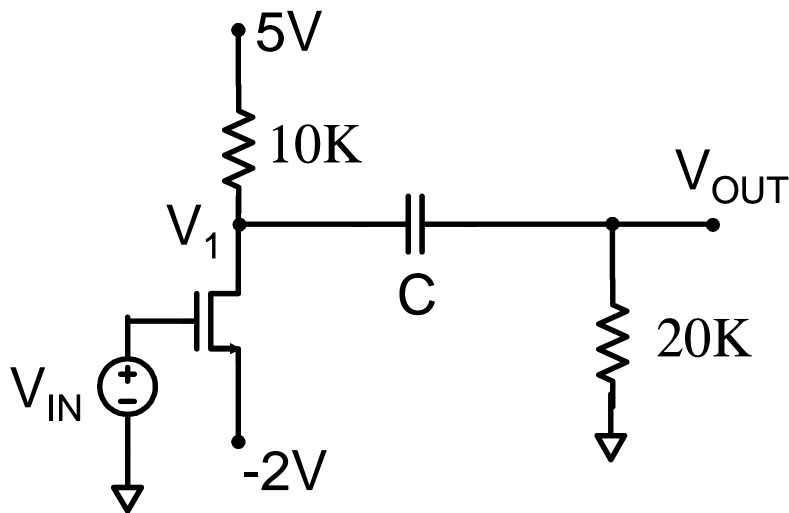
a) Determine how many die are on the wafer
b) Determine the average cost per fabricated die.
c) If the defect density is $1.2/cm^2$, determine the expected yield

Problem 2 Assume the transistor is fabricated in a process with μC_{OX}=100uA/V^2, V_T = 0.75V, λ=0v^{-1}, γ=0 and ϕ=0.6V and that the bulk (not shown) is connected to the source. Assume that the gm of the transistor at the Q-point established in this circuit was measured to be g_m= 5E-4 A/V and the capacitor is large.

a) Determine the small signal voltage gain relating the small signal output voltage to the small signal input voltage.

b) Determine the quiescent value of V_{OUT} and V_1

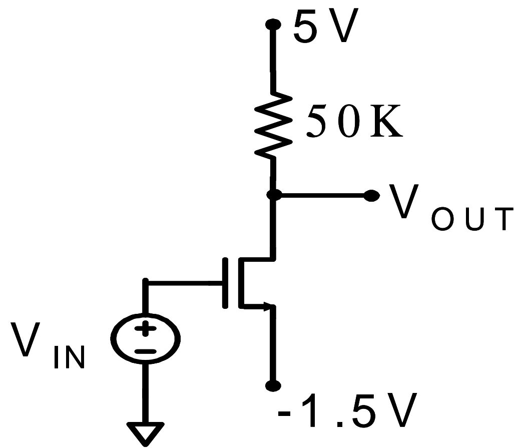
c) Determine the quiescent power dissipation of this circuit.



Problem 3 Assume the transistor is fabricated in a process with μC_{OX}=100uA/V^2, V_T = 0.75V, λ=.01v^{-1}, γ=0 and ϕ=0.6V and that the bulk (not shown) is connected to the source.

a) Size the transistor so that V_{OUTQ}=1V .

b) Determine the small signal device model at the Q-point determined in part a)



Problem 4 Assume the transistor is fabricated in a process with μC_{OX}=100uA/V^2, V_T = 0.75V, λ=.01v^{-1}, γ=0 and ϕ=0.6V and that the bulk (not shown) is connected to the source.

a) Determine the current I_D if Vx=8V

b) Determine the current I_D if Vx=0.25V