EE 434 Name _____
Exam 1
Fall 2003

Instructions. Students may bring two 8.5 x 11 pages of notes to this exam. On the exam, there are a set of short questions and 4 problems. All questions are worth 2 points and each problem is worth 20 points. All work and answers are to appear on this exam sheet. Attach additional sheets only if you run out of room on the examination itself.

If references to a semiconductor processes are needed and are not specified, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=30\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$, and Cbdsw = $2.5fF/\mu$. and all npn bipolar transistors are characterized by the parameters $\beta =100$, $V_{AF} =4$, and $J_S= 3E\text{-}19A/\mu^2$. If more detailed information is needed, consult the process information attached as the last page of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Questions

1. What region of operation in the bipolar transistor is analogous to the saturation region of operation of the MOSFET?

2. What is the major difference between epitaxial silicon and polysolicon?

3. What is the major purpose of the field oxide growth in a CMOS process?

4. In a standard n-well bulk CMOS process the bulk-source voltages of all p-channel transistors can be made 0 to prevent the bulk voltage from modulating the threshold voltage but this can not be done for all n-channel transistors. Why can this not be done for all of the n-channel transistors?

5. What is the gate-source capacitance of an n-channel MOSFET in a 0.5u CMOS process if the channel dimensions are W=5u and L=10u? Selected parameters of a 0.5u CMOS process are attached on the last page of this exam.

6. The parameters NRD and NRS are optional parameters that can be included in the device line for a MOSFET in SPICE. What is the purpose of these two parameters?

7. An interconnect that is 100u long and 0.6u wide is needed on a layout. Compare the resistance of this interconnect if it is made with Metal 3 to what it would be if made with p+ active. Use the process parameters on the last page of this exam to make this comparison.

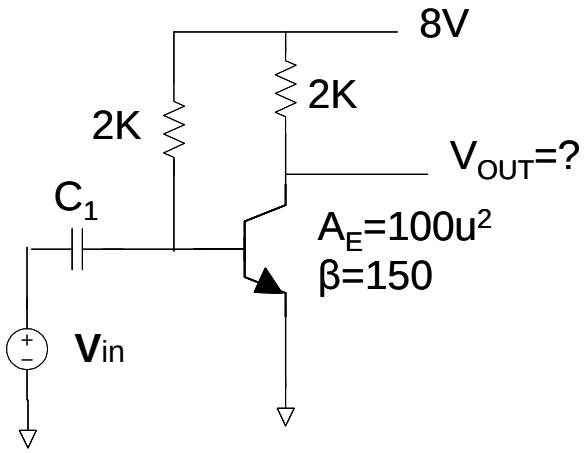
8. Why is the transconductance gain of a BJT typically much larger than that of a MOSFET?

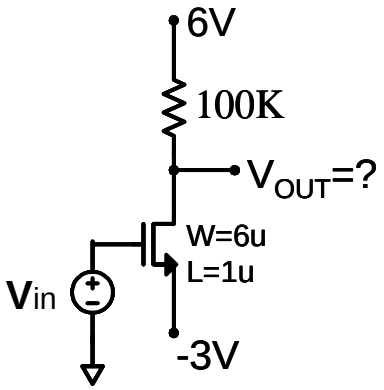
9 In a state of the art CMOS process, the gate oxide thicknesses are in the 30Å range. If SiO_2 is used for the dielectric, about how many molecules are stacked vertically to form this dielectric?

10. The polysilicon processing step that is used to form the gates of MOS transistors is often termed a self-aligned process. Explain what self-aligned means when used in this context.

Problem 1 Determine the approximate cost per good die in a 0.25u process if the die area is $6mm^2$ and the defect density is $1.5/cm^2$. Assume the cost of processing an 8 inch wafer is $1400.

Problem 2 For the following circuits, determine the region of operation and the variable indicated with a ?. The two voltage sources labeled Vin are small signal voltage sources.

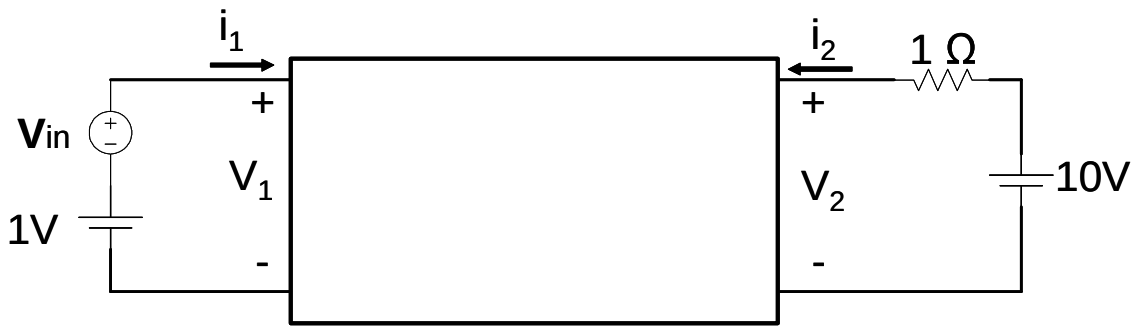




Problem 3 A two-port nonlinear network is shown below. The nonlinear relationship between the port variables is given by the equations

$$I_1 = 0.001V_1 + 0.02V_1V_2^2$$

$$I_2 = 2V_1^3$$



a) Determine the small signal model and a small-signal equivalent circuit in terms of V_{1Q} and V_{2Q}

b) Determine the quiescent operating point for the circuit and numerical values for the parameters in the small signal model obtained in part a)

c) Determine the small signal voltage gain from the Vin input to the V_2 output.

Problem 4 The layout of a transistor is shown. Assume the drain is defined by the top side of the device and the source by the bottom side of the device. Determine the following characteristics of this device:

W/L _____

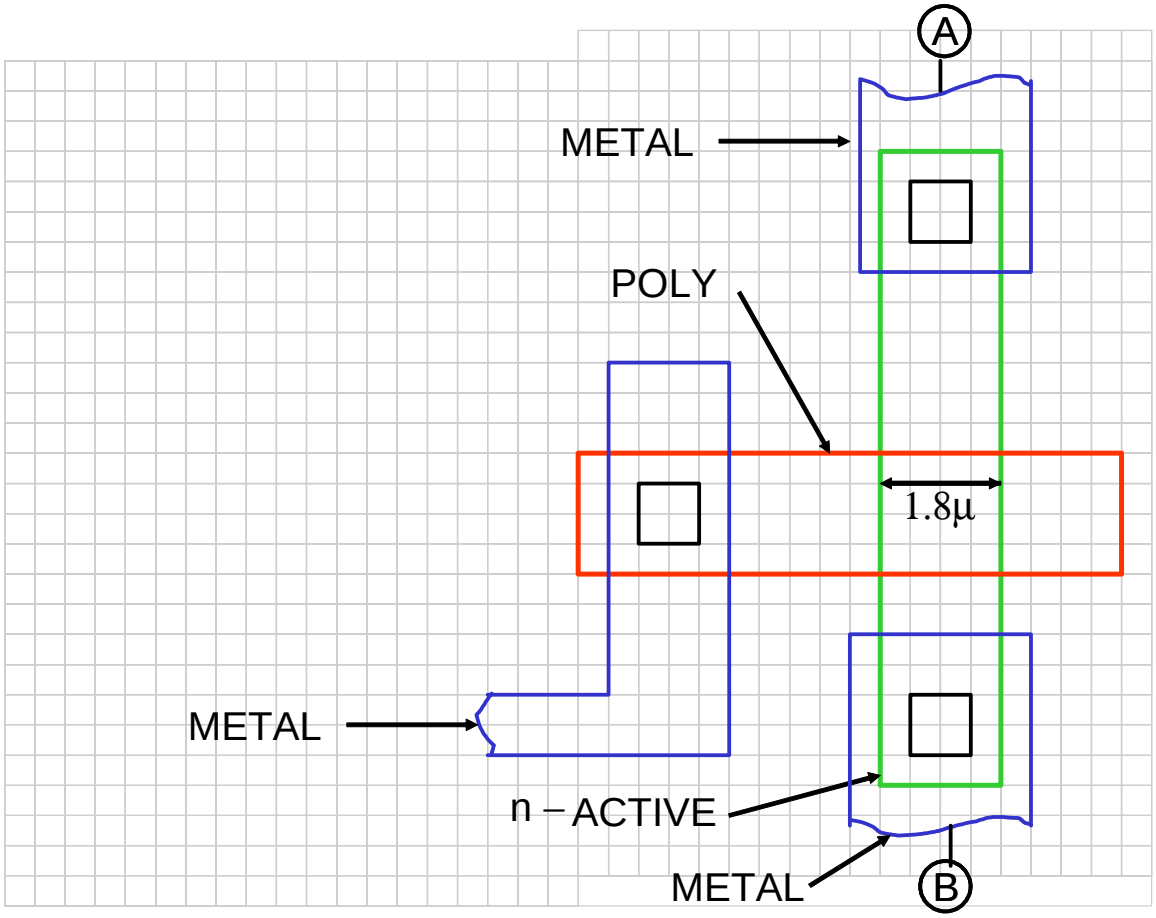
$C_{drain/bulk}$_____

Parasitic Gate Resistance _____

Resistance from Top Metal (designated as Ⓐ) to Drain _____

Small signal g_m if the quiescent gate to source voltage is 3 V _____

Use the process parameters listed on the last page of this exam to solve this problem.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um