EE 434 Name _____
Exam 1
Fall 2004

Instructions. Students may bring two 8.5 x 11 pages of notes to this exam. On the exam, there are a set of short questions and 4 problems. All questions are worth 2 points and each problem is worth 20 points. All work and answers are to appear on this exam sheet. Attach additional sheets only if you run out of room on the examination itself.

If references to a semiconductor processes are needed and are not specified, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=30\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$. If more detailed information is needed, consult the process information attached as the last page of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Questions

1. What is the major reason that depletion transistors are not available in most standard bulk CMOS processes?

2. What is the purpose of the silicide processing step in a CMOS process?

3. If a field oxide is thermally grown on a silicon substrate to a thickness of 8,000 $\mathring{A}$, how deep will the field oxide extend into the original silicon surface?

4. What is the minimum channel length in a state of the art CMOS process?

5. When was the BJT transistor first created?

6. How do the physical properties of an n-type epitaxial layer differ from those of an n-type diffused layer?

7. What are the two major limitations of using reverse-biased pn junctions as capacitors?

8. Why are contacts to poly on top of the channel of a MOSFET usually not permitted?

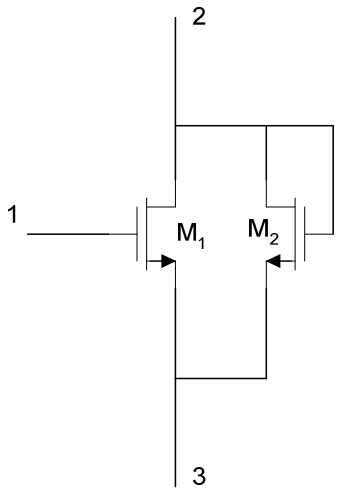
9 What is the small-signal equivalent circuit for a large inductor?

What is the dc equivalent circuit for a large capacitor?

10. What is the long-term failure mechanism associated with aluminum interconnects called and why is this mechanism problematic?

Problem 1 Determine the approximate cost per good die in a 0.25u process in which an 8 inch wafer costs $2600 if the die is rectangular of dimensions 1600µ by 1200µ and if the defect density is 1.25/cm^2.

Problem 2 Determine the small signal equivalent for the following three-terminal device. You may assume that both transistors are operating in the saturation region and that $V_{BS}=0$. Use the simple Sah/Shockley model for the devices.



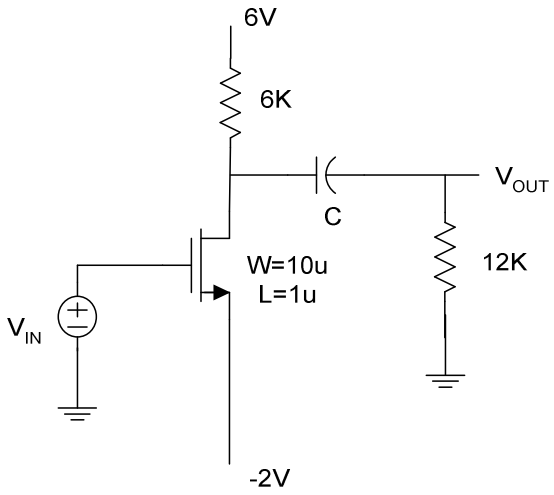
Problem 3 Assume the input to the following circuit is $V_{IN} = .05\sin 4000t$, C is large, and the process is characterized by V_T=1V and μC_{OX}=100μA/V^2.

a) Determine the quiescent drain current and the quiescent output voltage

b) Draw a small signal equivalent circuit

c) Determine the small signal voltage gain $A_V = \frac{V_{OUT}}{V_{IN}}$

d) Give an expression for the total output voltage



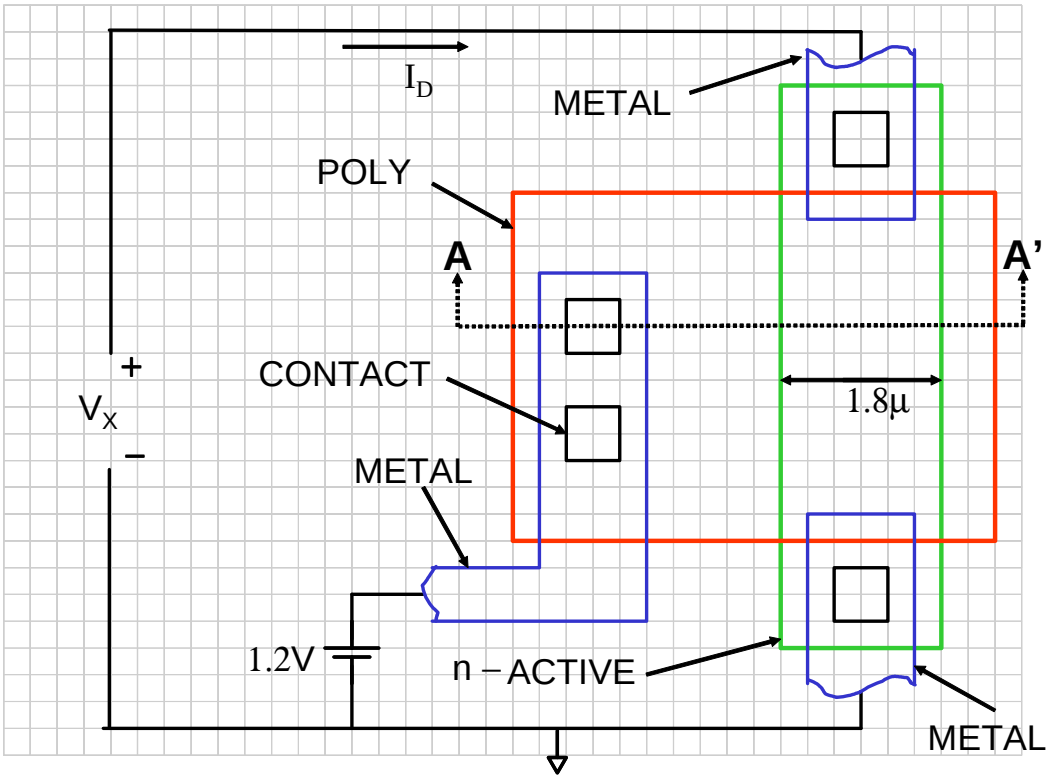
Problem 4 The layout of a simple circuit in an n-well bulk CMOS process is shown below. Assume the substrate is connected to 0V.

a) Sketch a cross-sectional view of the die that will be formed with this layout along the AA' section line

b) Assume the drain of the transistor is the upper diffusion. Determine the drain-substrate capacitance if V_X=0 and if V_X=5V

c) Determine the maximum voltage V_X that will keep the transistor operating in the triode region.

Use the process parameters listed on the last page of this exam to solve this problem.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um