EE 434 Name ____________________

EXAM 1

Fall 2005

Instructions. Students may bring two 8.5 x 11 pages of notes to this exam. On the exam, there are a set of short questions and 5 problems. All questions are worth 2 points and each problem is worth 16 points. All work and answers are to appear on this exam sheet. Attach additional sheets only if you run out of room on the examination itself.

If references to a semiconductor processes are needed and are not specified in the problem, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$ ,$\mu_p C_{OX}=30\mu A/v^2$ ,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$. If more detailed information is needed, consult the process information attached at the end of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Questions

1. About how big is the semiconductor industry (in worldwide sales $/Year)?

2. What is the approximate size of a silicon atom (in micrometers)?

3. Why are the features on a mask in state of the art processes intentionally distorted?

4. How does Physical Vapor Deposition differ from Chemical Vapor Deposition?

5. Why is the $SiO_2$ stripped and then regrown then forming the gate oxide?

6. How deep will the silicon dioxide layer extend into the original silicon surface when thermally growing x microns of $SiO_2$?

7. What is the difference between epitaxial silicon and polysilicon?

8. Why is metal usually preferred over polysilicon for making interconnects?

9 The standard “square law” model of the MOSFET is given below. Identify the process parameters and the design parameters in this model.

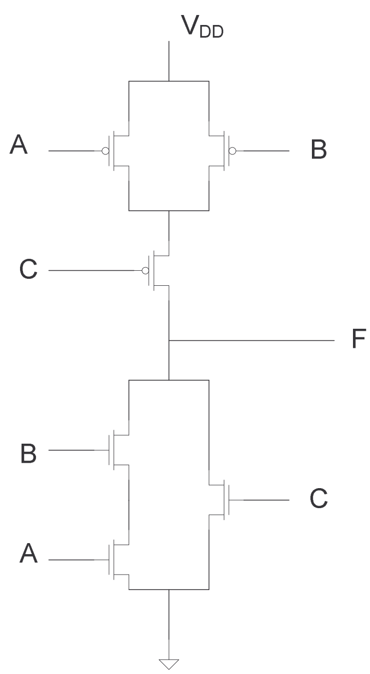
Process Paramaters { }

Design Parameters { }

$$I_D = \begin{cases} 0 & V_{GS} \le V_T \\ \mu C_{OX} \dfrac{W}{L}\left(V_{GS} - V_T - \dfrac{V_{DS}}{2}\right)V_{DS} & V_{GS} \ge V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{OX} \dfrac{W}{2L}(V_{GS} - V_T)^2 \bullet (1 + \lambda V_{DS}) & V_{GS} \ge V_T \quad V_{DS} \ge V_{GS} - V_T \end{cases}$$

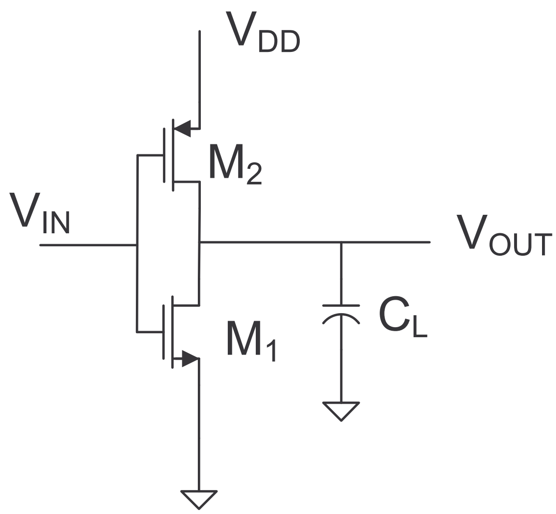
$$V_T = V_{T0} + \gamma\left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right)$$

10. A Boolean gate is shown. Obtain an expression for the output variable F

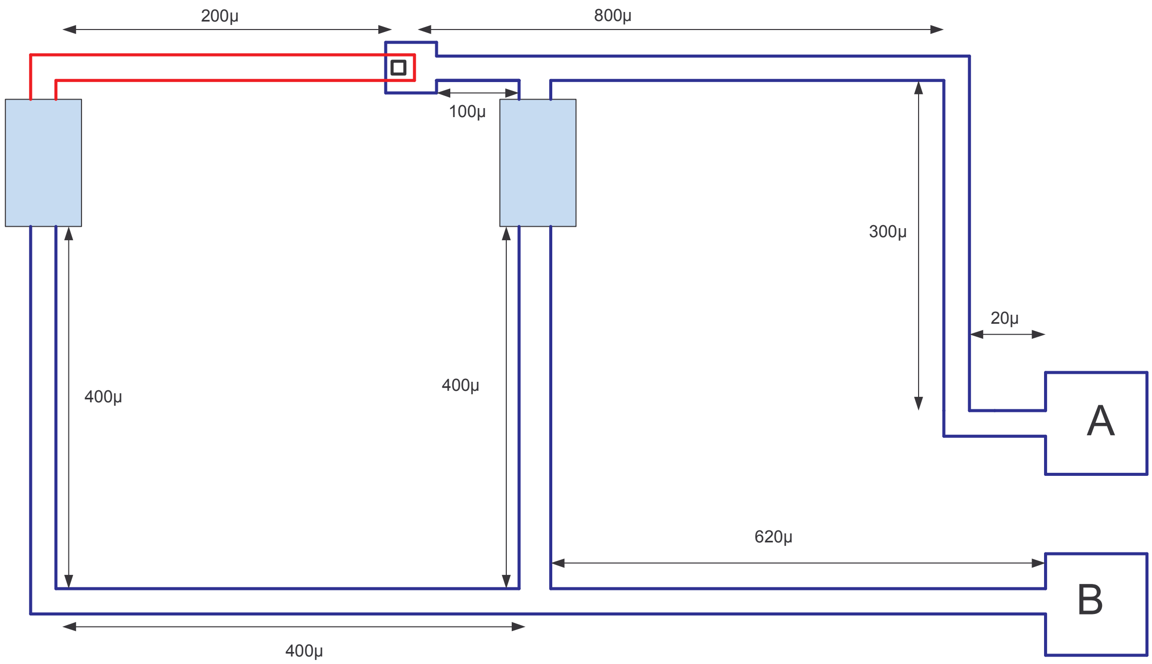


Problem 1  Assume you need to make a decision about whether it is economically viable to fabricate an integrated circuit in a CMOS process with 12inch wafers that cost $2600 each. The customer indicated that the market will can support at most a good die cost of $1.40. What is the maximum die area and that can be used for this design if you must keep the good die cost within the $1.40 budget? Assume the only die loss is due to hard faults and the defect density is $1.5/cm^2$.

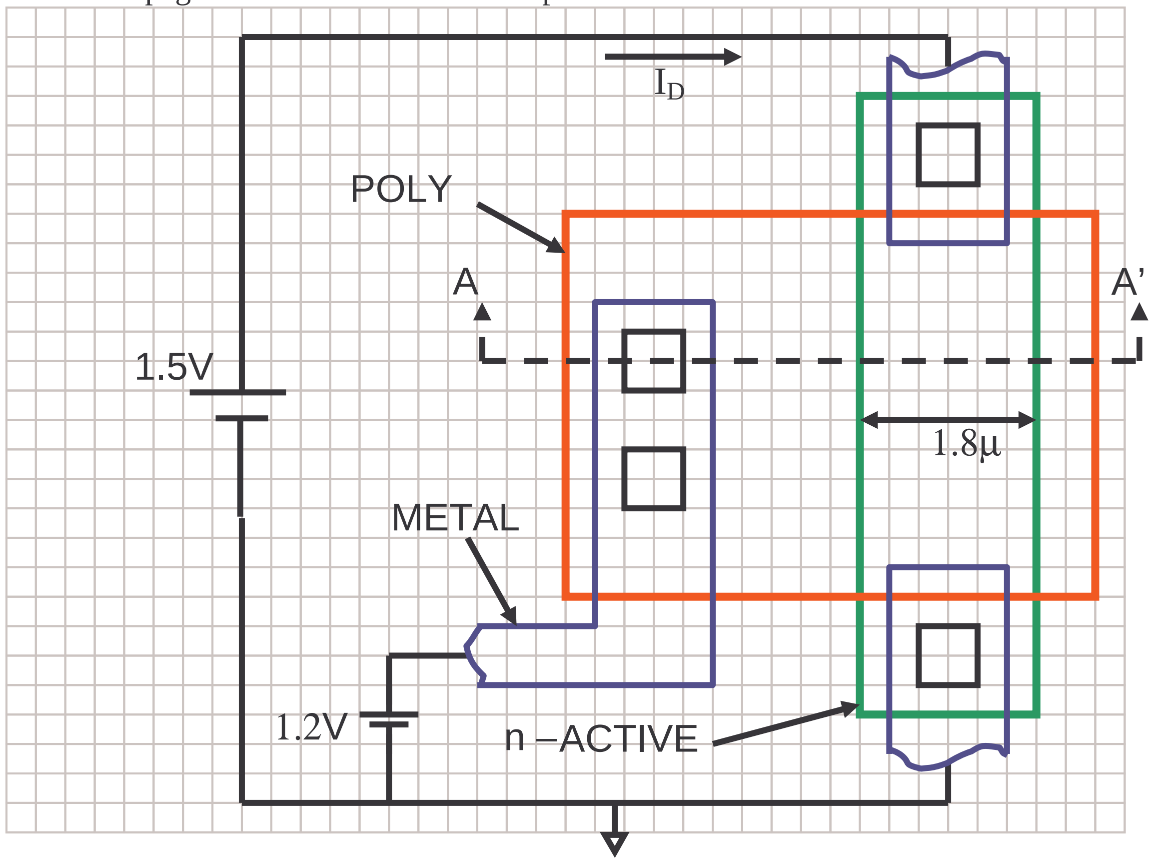
Problem 2 A static CMOS inverter is driving a load capacitance of $C_L$=500fF as shown in the circuit diagram below. If an ideal 5V pulse is applied at the input, determine the rise and fall times of the inverter. Assume the transistor $M_1$ has width of 20μ and length of 1μ and transistor $M_2$ has a length of 2μ and a width of 5μ. The supply voltage is $V_{DD}$ = 5V.



Problem 3 The routing to two circuit blocks (shown in shaded blue) designed in the AMI 0.5u process, is shown. Two bonding pads denoted with the letters A and B are also shown. This routing is not to scale but the key dimensions are given. If a dimension is not given, you may assume it is arbitrarily small or that the feature does not contribute to any interconnect problems. The red is Poly 1 and the blue is Metal 1. Both are 1u wide. The two loads are nominally 500 ohms and the goal of the designer was to distribute a bias of $V_{DD}$ applied to pads A and B of 5V to the two blocks. What will the actual voltage be at the two blocks with this interconnect layout?



Problem 4 The layout of a circuit designed in the AMI 0.5u CMOS process is shown. Determine the current $I_D$ that will flow in this circuit. (the color codes are Red- Poly 1, Green- n-active, Blue – Metal 1 and Black – contact. Use the process parameters listed on the last page of this exam to solve this problem.



Problem 5 Sketch a cross-section view of the layout shown in Problem 4 along the AA’ cross section line.

| TRANSISTOR PARAMETERS | W/L | N-CHANNEL | P-CHANNEL | UNITS |
|---|---|---|---|---|
| MINIMUM | 3.0/0.6 | | | |
| Vth | | 0.78 | -0.93 | volts |
| SHORT | 20.0/0.6 | | | |
| Idss | | 439 | -238 | uA/um |
| Vth | | 0.69 | -0.90 | volts |
| Vpt | | 10.0 | -10.0 | volts |
| WIDE | 20.0/0.6 | | | |
| Ids0 | | < 2.5 | < 2.5 | pA/um |
| LARGE | 50/50 | | | |
| Vth | | 0.70 | -0.95 | volts |
| Vjbkd | | 11.4 | -11.7 | volts |
| Ijlk | | <50.0 | <50.0 | pA |
| Gamma | | 0.50 | 0.58 | V^0.5 |
| K' (Uo*Cox/2) | | 56.9 | -18.4 | uA/V^2 |
| Low-field Mobility | | 474.57 | 153.46 | cm^2/V*s |

COMMENTS: XL_AMI_C5F

| FOX TRANSISTORS | GATE | N+ACTIVE | P+ACTIVE | UNITS |
|---|---|---|---|---|
| Vth | Poly | >15.0 | <-15.0 | volts |

| PROCESS PARAMETERS | N+ACTV | P+ACTV | POLY | PLY2_HR | POLY2 | MTL1 | MTL2 | UNITS |
|---|---|---|---|---|---|---|---|---|
| Sheet Resistance | 82.7 | 103.2 | 21.7 | 984 | 39.7 | 0.09 | 0.09 | ohms/sq |
| Contact Resistance | 56.2 | 118.4 | 14.6 | | 24.0 | | 0.78 | ohms |
| Gate Oxide Thickness | 144 | | | | | | | angstrom |

| PROCESS PARAMETERS | MTL3 | N\PLY | N_WELL | UNITS |
|---|---|---|---|---|
| Sheet Resistance | 0.05 | 824 | 815 | ohms/sq |
| Contact Resistance | 0.78 | | | ohms |

COMMENTS: N\POLY is N-well under polysilicon.

| CAPACITANCE PARAMETERS | N+ACTV | P+ACTV | POLY | POLY2 | M1 | M2 | M3 | N_WELL | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Area (substrate) | 429 | 721 | 82 | | 32 | 17 | 10 | 40 | aF/um^2 |
| Area (N+active) | | | 2401 | | 36 | 16 | 12 | | aF/um^2 |
| Area (P+active) | | | 2308 | | | | | | aF/um^2 |
| Area (poly) | | | | 864 | 61 | 17 | 9 | | aF/um^2 |
| Area (poly2) | | | | | 53 | | | | aF/um^2 |
| Area (metal1) | | | | | | 34 | 13 | | aF/um^2 |
| Area (metal2) | | | | | | | 32 | | aF/um^2 |
| Fringe (substrate) | 311 | 256 | | | 74 | 58 | 39 | | aF/um |
| Fringe (poly) | | | | | 53 | 40 | 28 | | aF/um |
| Fringe (metal1) | | | | | | 55 | 32 | | aF/um |
| Fringe (metal2) | | | | | | | 48 | | aF/um |
| Overlap (N+active) | | | 206 | | | | | | aF/um |
| Overlap (P+active) | | | 278 | | | | | | aF/um |