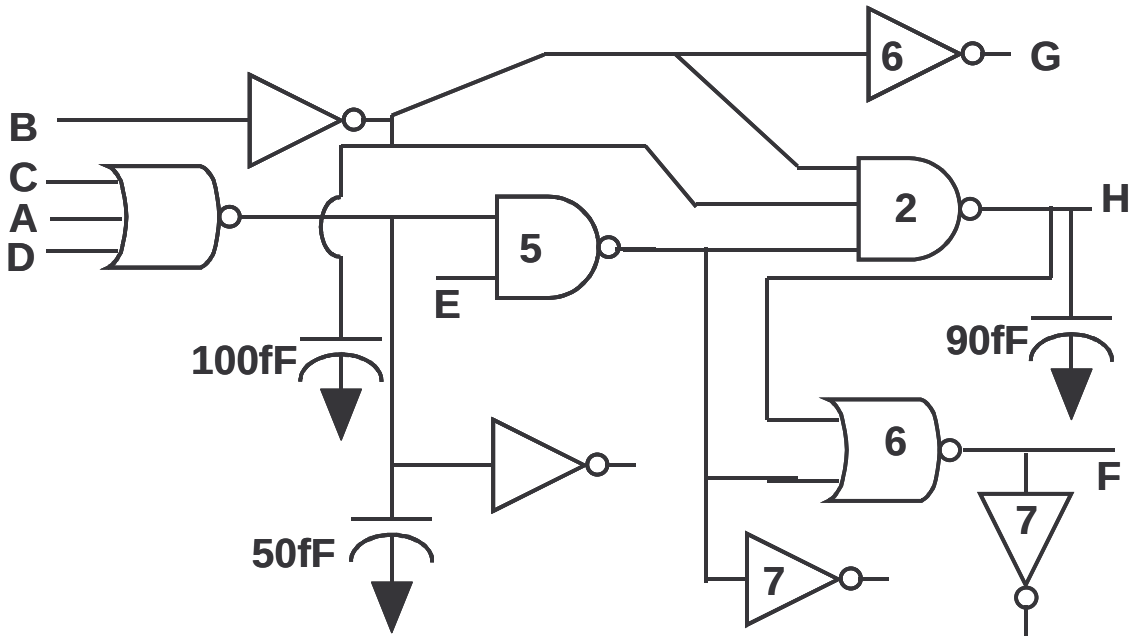
EE 434 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 2
Fall 2001

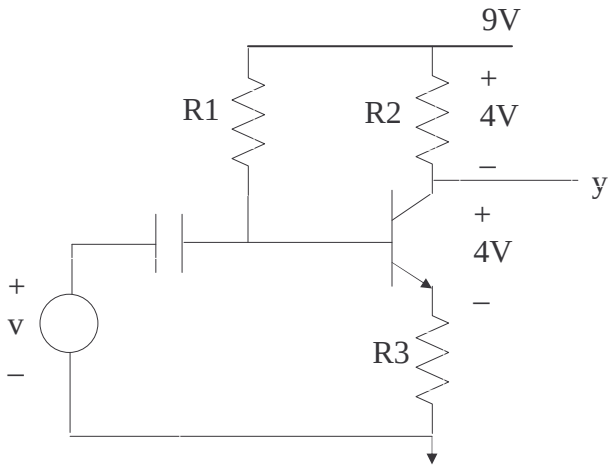
Instructions. This is an open-book, open-notes exam with 6 problems. All are equally weighted. Solve all 6 problems. Please solve the problems and include your answers directly on the exam sheet.

Problem 1 A logic circuit designed in conventional CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the Binput to the F utput
b) Repeat part a) if the three-input NOR gate is minimum sized.



Problem 2. In the following circuit, $\beta = 200$ and the capacitor is of appropriate value to be considered DC open and AC short. Select the resistances so that the quiescent power is about 6 mW and the quiescent voltages are as shown. Then find the small signal voltage gain from v to y.

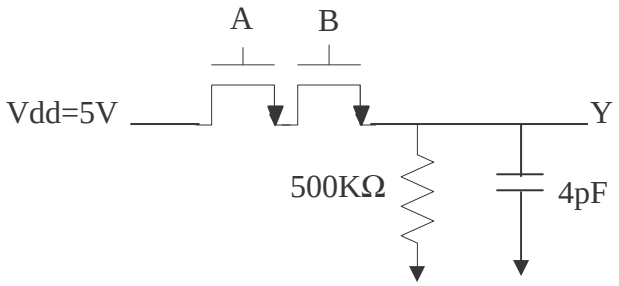


Problem 3. Consider the PTL two input AND gate below. Assume that Y is open, V_{DS} can be neglected in triode, and the logic levels for A and B are 0V for low and 5V for high. Ignore any additional parasitic capacitances.

a) Find the static current I_{low} when Y=low and I_{high} when Y=high, and the corresponding static power $P_{static\text{-}low}$ and $P_{static\text{-}high}$ drawn from Vdd.

b) If A = high and B is clocked to be alternating low and high at f_B = 4 kHz, find the dynamic power consumed in driving the capacitor.

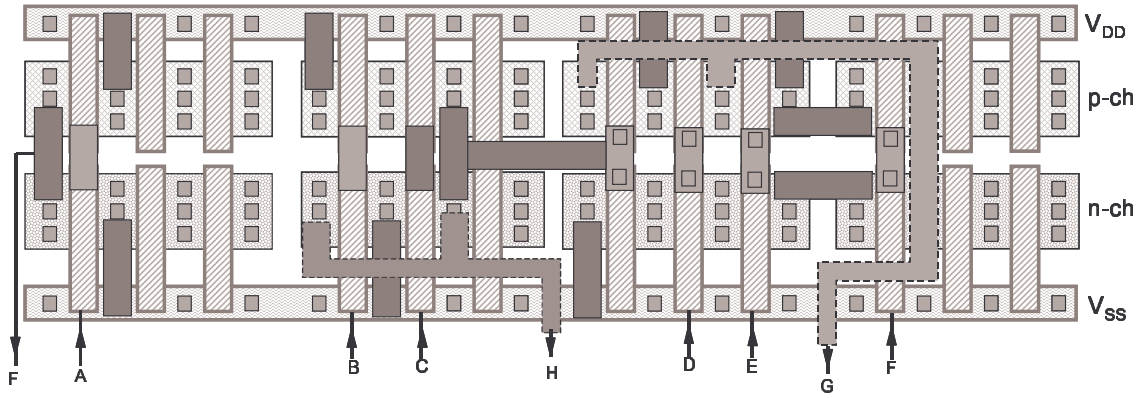
c) Repeat b) if both A and B are synchronously clocked at 4 kHz but in each cycle their levels are independently and randomly set to high or low with equal probability.

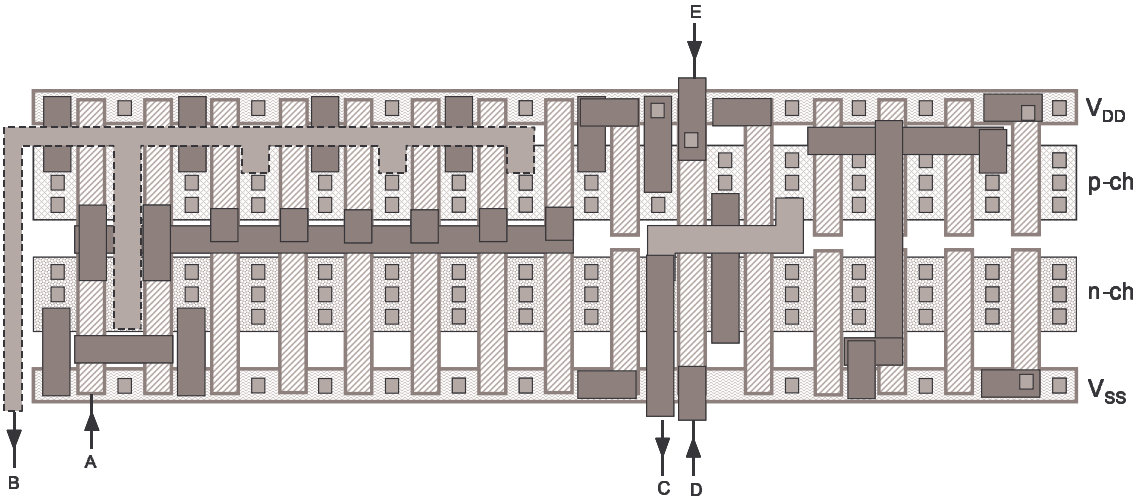


Problem 4. Implement $Y=A\overline{B+C}$ in the following logic styles. Draw schematics to the transistor level but you need not size the devices. No layout is needed. Assume both the input variables and their complements are available.

a) Standard static CMOS logic
b) Complex logic
c) PTL
d) Domino logic.

Problem 5 Two logic structures are shown. Determine the Boolean expressions for all variables indicated with an arrow pointing out. The shaded regions denote metal interconnect. If the boundary is a solid line, the interconnect is with Metal 1. If the boundary is dashed, the interconnect is with Metal 2.





Problem 6 Design a 3input OR gate and a 2 input NAND gate in static CMOS. First size the devices for an overdrive of 1 and then size the devices for an overdrive of 4.