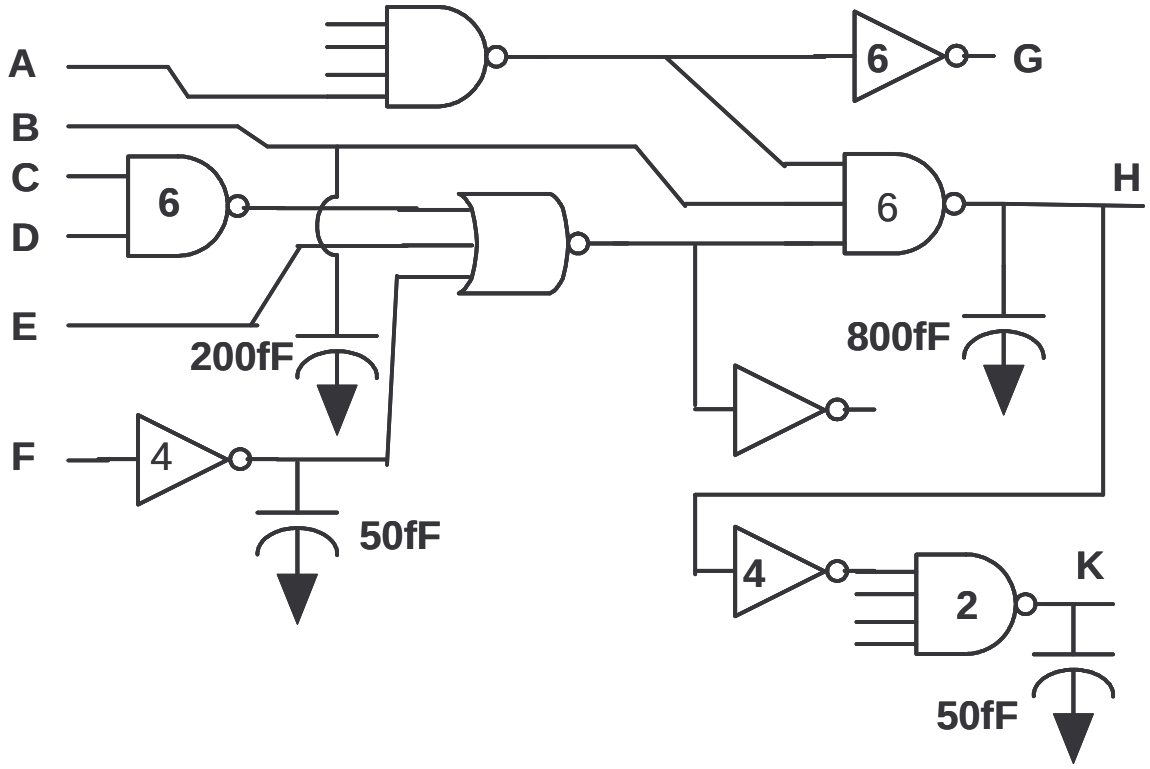
EE 434 Name _____
EXAM 2
Fall 2002

Instructions. You may bring four sheets of notes to this exam which is comprised of 4 problems. The weight for each problem is as shown. Please solve the problems and include your answers directly on the exam sheet.

Problem 1 (20 pts) A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay ($T_{HL} + T_{LH}$) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay ($T_{HL} + T_{LH}$) from the F input to the K output
b) Repeat part a) if all gates are minimum sized.



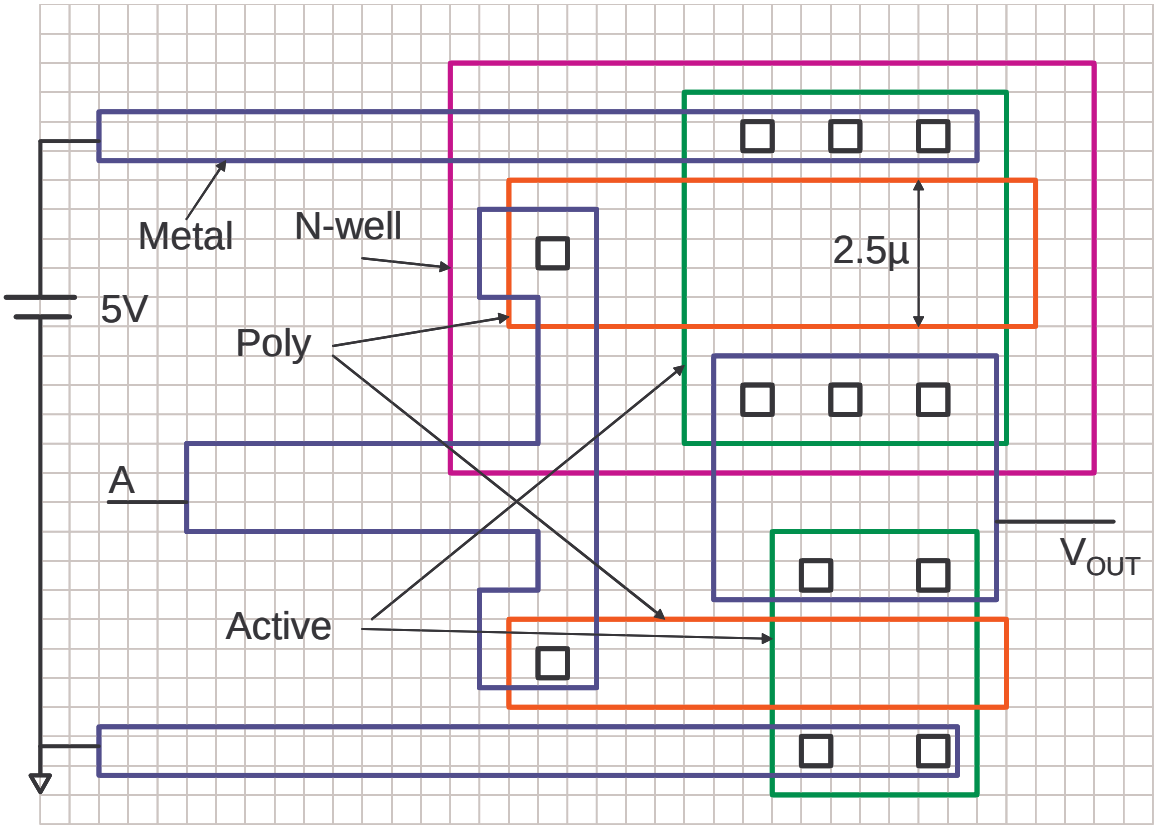
Problem 2. (35 pts) The layout of a digital circuit with an input at the node labeled A and the output labeled V_{OUT} is shown. Assume this is fabricated in the AMI 0.5u CMOS process and that relevant characteristics of the process appear on the second following page. The following page is provided for your solution.

a) Determine t_{HL} and t_{LH} if this inverter is driving an identical device. Neglect any diffusion capacitances in this calculation.

b) Determine the diffusion capacitances on the output node when the output is high and when the output is low.

c) Determine the trip point for this circuit.

d) If the A input is driven by another inverter that has Ln=Lp=1u, Wn=2u and Wp=10u, determine the dynamic power dissipation in the driver that drives the A input if the clock frequency is 4MHz.



TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.78	-0.93	volts
SHORT	20.0/0.6			
Idss		439	-238	uA/um
Vth		0.69	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.70	-0.95	volts
Vjbkd		11.4	-11.7	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.50	0.58	V^0.5
K' (Uo*Cox/2)		56.9	-18.4	uA/V^2
Low-field Mobility		474.57	153.46	cm^2/V*s

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	PLY2_HR	POLY2	MTL1	MTL2	UNITS
Sheet Resistance	82.7	103.2	21.7	984	39.7	0.09	0.09	ohms/sq
Contact Resistance	56.2	118.4	14.6		24.0		0.78	ohms
Gate Oxide Thickness	144							angstrom

PROCESS PARAMETERS	MTL3	N\PLY	N_WELL	UNITS
Sheet Resistance	0.05	824	815	ohms/sq
Contact Resistance	0.78			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	POLY2	M1	M2	M3	N_WELL	UNITS
Area (substrate)	429	721	82		32	17	10	40	aF/um^2
Area (N+active)			2401		36	16	12		aF/um^2
Area (P+active)			2308						aF/um^2
Area (poly)				864	61	17	9		aF/um^2
Area (poly2)					53				aF/um^2
Area (metal1)						34	13		aF/um^2
Area (metal2)							32		aF/um^2
Fringe (substrate)	311	256			74	58	39		aF/um
Fringe (poly)					53	40	28		aF/um
Fringe (metal1)						55	32		aF/um
Fringe (metal2)							48		aF/um
Overlap (N+active)			206						aF/um
Overlap (P+active)			278						aF/um

Problem 3 (30 pts) Assume a signal A serves as the input to a minimum-sized equal rise/fall time inverter and the signal at the output of this inverter must drive a 8pF load capacitance.

a) Determine the propagation delay ($t_{HL}+t_{LH}$) if the load is driven directly.

b) Determine the propagation delay from input to the load if a 3-stage equal rise/fall time pad driver is used (thus a total of 4 inverters, the minimum-sized inverter followed by a 3-stage pad driver) where the overdrive of the first stage in the pad driver is 10, that of the second stage is 100 and that of the third and final stage is 1000.

c) Determine the dynamic power dissipation in the next to the last stage of the pad driver.

Assume the reference inverter has an input capacitance of 4fF and that Rpd =4KΩ

Problem 4 (15 pts) Design a 4input OAI (Or And Invert) gate in static CMOS with equal worst-case rise and fall times on each gate. First size the devices in all gates needed to implement this function for an overdrive of 1 and then size the devices so that the output has an overdrive of 6.