EE 434 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Exam 2

Fall 2003

Instructions. Students may bring 4 pages of notes to this exam. There are 9 questions. The first 8 are worth 2 points each and question 9 is worth 4 points. There are 6 problems. Solve any 5 of the 6. Only 5 of the 6 will be grades and those 5 that are solved are worth 16 points each. Put an X through the problem you do not want graded. If no X is indicated, problems 1-5 will be graded.

If references semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=30\mu A/v^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$, and Cbdsw = $2.5fF/\mu$. If any other process parameters are needed, specify clearly what process parameters are needed and specify a typical value for that parameter.

1. What is the major problem associated with cascading pass transistor logic gates?

2. Sketch the basic SRAM cell.

3. What is the major source of power dissipation in most standard static CMOS circuits?

4. In class we first talked about Static CMOS design and then discussed several other logic design styles. The Static CMOS approach has several very attractive properties. What is the major reason we looked at other design strategies?

5. What problem in a basic dynamic logic gate does the domino logic approach or the zipper logic approach solve

6. What is the major reason a DRAM has a much higher density (bits/unit area) than a SRAM?

7. What application specifically favors the use of pseudo-nmos logic when building a logic circuit in a standard CMOS process?

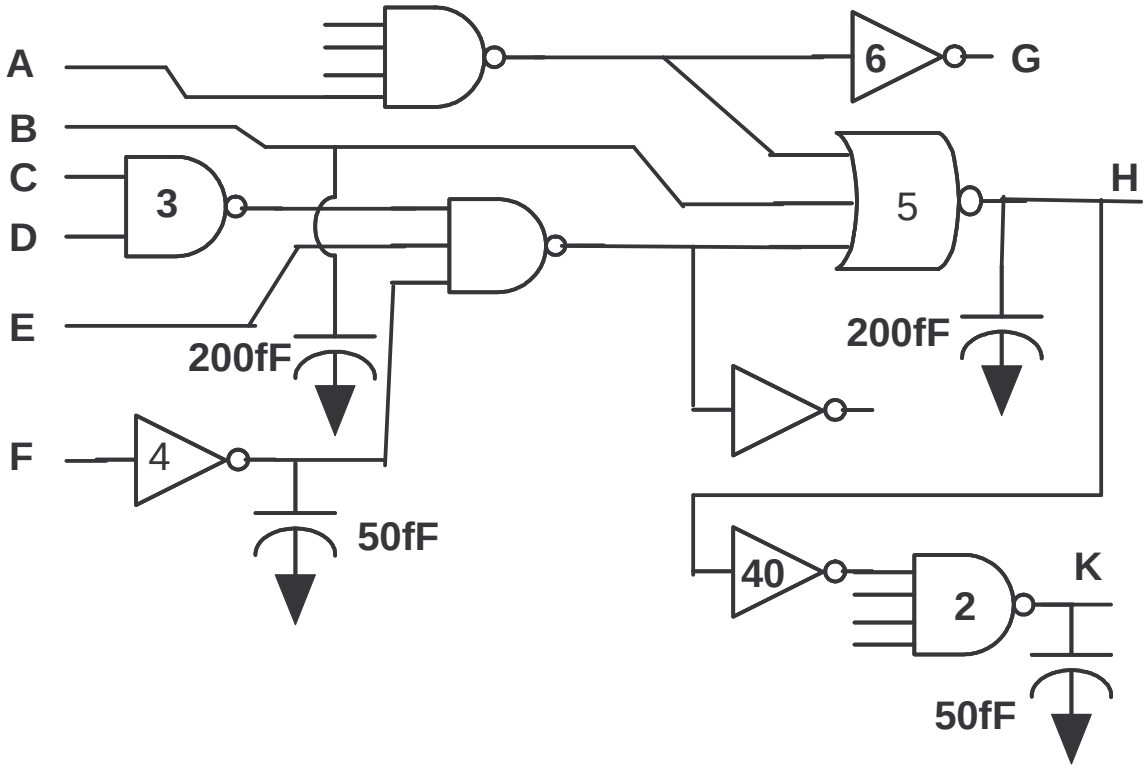
8. Digital logic benefits significantly from scaling of the lateral feature sizes. What increase in density (gates/unit area) can be expected as the process technology scales from 0.25u to 0.05u that will likely be available in the near future?

9. If making a very low power low speed circuit, what improvement in power dissipation would be expected to implement the same logic function using minimum-sized gates relative to that required using equal rise/fall time gates? Be quantitative and neglect reverse leakage current.

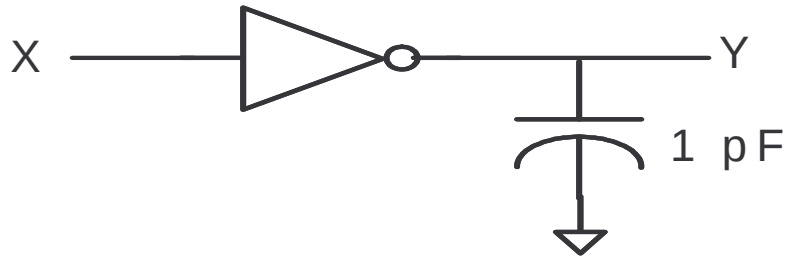
Problem 1 A logic circuit designed in conventional CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times and that the input capacitance of an equal rise/equal fall reference inverter is 2fF and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the C input to the H output

b) Repeat part a) if the three-input NOR gate is comprised entirely of minimum sized devices.

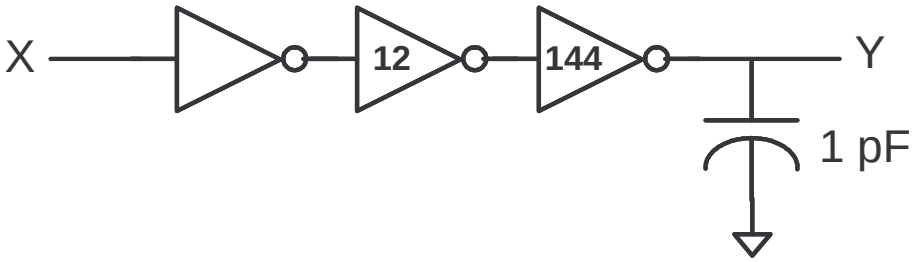


Problem 2 a) What is the maximum speed at which a minimum sized inverter driving a 1pF load can be clocked? Assume the minimum sized inverter is an equal rise/fall time structure with an input capacitance of 2fF and a propagation delay ($T_{HL} + T_{LH}$) of 20psec.



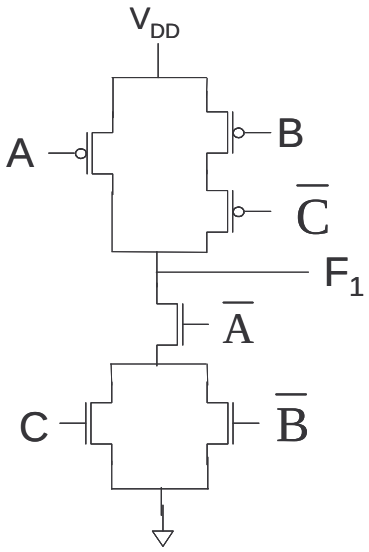
b) What is the static and dynamic power dissipation dissipated by the inverter if clocked at the rate determined in part a)?

c) By how much and in what direction does the maximum clock speed change if the same load is driven by a cascade of 3 inverters, the first being minimum sized, the second with an overdrive of 12 and the third with an overdrive of 144?

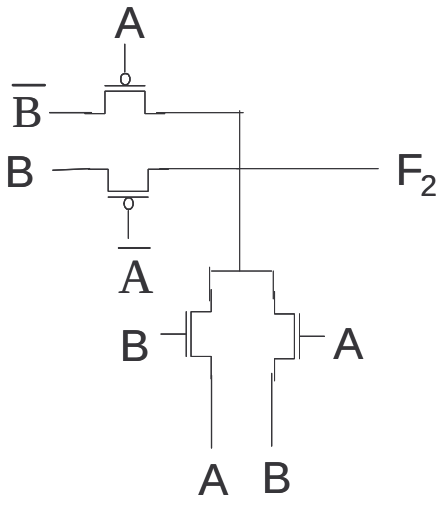


Problem 3. Three circuits are shown below.

a) If the circuit implements a valid Boolean function to the F output, give the function and if not a valid function, state why it is not valid.
b) Which of the valid Boolean circuits are ratio logic circuits?
c) Which of the valid Boolean circuits have zero static power dissipation?



(1)



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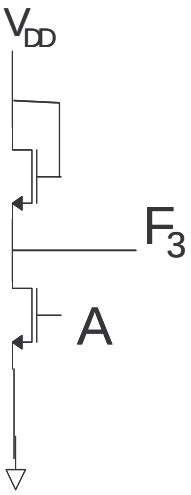


(3)

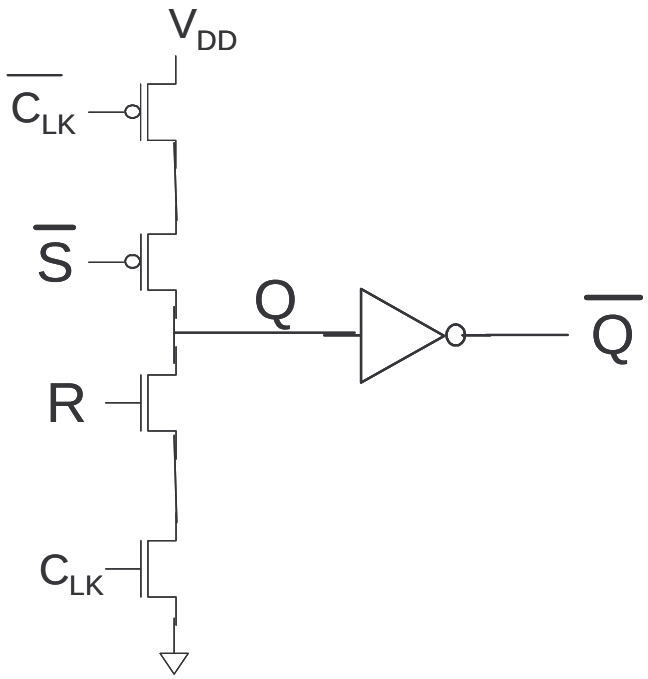
Problem 4. Implement $F = \left(\overline{\left(\overline{A} + B\right) \bullet C}\right)$ in the following logic styles. Draw schematics to the transistor level but deo not size the devices. No layout is needed. Assume both the input variables and their complements are available.

a) Standard static CMOS logic
b) Complex logic gates
c) PTL
d) Domino logic.

Problem 5

a) The following circuit has been proposed as a clocked SR flip flop. Does this circuit serve the intended function and, if not, why?

b) If in the intended application of the RS flip flop it is clocked at 50MHz and it is known that at least once every 1 usec either the Set or Reset function will occur, will it serve as a clocked SR flip flop?



Problem 6 Design a 4 input OR gate and a 3 input NAND gate in static CMOS. First size the devices for an overdrive of 1 and then size the devices for an overdrive of 3 on the final output.

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