Instructions: Answer the following questions and solve the following problems. In problems relating to timing or delay calculations, assume you are working in a process characterized by $C_{\text{REF}}=4C_{\text{OX}}W_{\text{min}}L_{\text{min}}=2 \text{fF}$ and that a minimum-sized equal rise/fall reference inverter has a $t_{\text{REF}}=t_{\text{HL}}+t_{\text{LH}}$ of 20psec. If other parameters are needed, refer to the process description appended to this exam. The relative weighting of all questions and problems are indicated.

Questions

1. (2 pts) What is the purpose of the “keeper” transistor in a dynamic logic gate?

2. (2pts) What are the two major benefits of Static CMOS logic over NMOS logic?

3. (2pts) Pass transistor logic (PTL) can be very compact. What are the two major limitations of PTL?

4. (2pts) What are the two major benefits the dynamic logic gate compared to Static CMOS?

5. (2pts) There are three hierarchical levels identified in the design process. What are they?

6. (2pts) When using synthesis tools for synthesizing logic, what level in the hierarchy will the designer usually work in?

7. (2pts) How does the total propagation delay of an inverter driving an identical inverter compare if the two inverters are both minimum sized compared to the case where they are both minimum-sized equal rise/fall time devices?

8. (3pts) A 3-input NOR gate in Static CMOS is minimum sized. What is the overdrive (OD) for the pull-up network and for the pull-down network?
9. (3pts) How much power is required in the output stage of a pad drier to drive a 1pF load with a 200MHz square-wave clock if the supply voltage is 5V?
Problem 1 (20 pts) Implement the function $F = AB + B\overline{C}$, at the transistor level, in
   a) Static CMOS
   b) Pass Transistor Logic
   c) Complex Logic Gates
   d) Domino Logic

You need not give transistor sizes.
Problem 2 (20 pts) The overdrive factor for each equal rise/fall
Gate is shown. Determine the width of all devices to achieve the given overdrive if
L=L_{min} for all devices. Give the width in terms of the minimum width, W_{min}, of the
process.

\[ W_n = \_ \_ \_ \]
\[ W_p = \_ \_ \_ \]

\[ W_n = \_ \_ \_ \]
\[ W_p = \_ \_ \_ \]

\[ W_n = \_ \_ \_ \]
\[ W_p = \_ \_ \_ \]

\[ W_n = \_ \_ \_ \]
\[ W_p = \_ \_ \_ \]
Problem 3 (20 pts)

a) Determine the propagation delay from F to H for the following circuit. The devices are all sized for equal worst case rise and fall times and the overdrive factors, if different from 1, are as indicated.

b) Repeat part a) if all devices are minimum sized.
Problem 4 (20 pts) The following complex logic gate has one or more errors in the Pull Up Network but the Pull Down Network is correct.

a) What is the Boolean Function this network is trying to implement to the F output?

b) Identify the error or errors in the Pull Up Network and correct them so that it implements the correct function.
MOSIS file ami-c5-t47f-params

MOSIS file ami-c5/t47f-params.txt

MOSIS PARAMETRIC TEST RESULTS

RUN: T47F  VENDOR: AMIS
TECHNOLOGY: SCN05  FEATURE SIZE: 0.5 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS  W/L  N-CHANNEL  P-CHANNEL  UNITS

MINIMUM  3.0/0.6
Vth  0.79  -0.94 volts

SHORT  20.0/0.6
Idss  456  -237 mA/um
Vth  0.68  -0.92 volts
Vpt  10.0  -10.0 volts

WIDE  20.0/0.6
Ids0  < 2.5  < 2.5 mA/um

LARGE  50/50
Vth  0.70  -0.96 volts
Vjbd  11.4  -11.7 volts
Ijlk  <50.0  <50.0 pA
Gamma  0.47  0.59 V^0.5
K' (Uo*Cox/2)  56.8  -18.9 mA/V^2
Low-field Mobility  460.58  153.26 cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology  XL (um)  XW (um)
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SCMOS_SUBM (lambda=0.30)  0.10  0.00
SCMOS (lambda=0.35)  0.00  0.20

FOX TRANSISTORS  GATE  N+ACTIVE  P+ACTIVE  UNITS
Vth  Poly  >15.0  <-15.0 volts

PROCESS PARAMETERS  N+  P+  POLY POLY2 HR POLY2 HR POLY2 M1 M2 UNITS
Sheet Resistance  83.6  104.8  22.1  1106  41.3  0.09  0.09 ohms/sq
Contact Resistance  62.2  155.8  15.8  27.1  0.93 ohms
Gate Oxide Thickness  140 angstrom

PROCESS PARAMETERS  M3  N\POLY  N\W  UNITS
Sheet Resistance  0.05  827  82.0 ohms/sq
Contact Resistance  0.90 ohms

COMMENTS: N\POLY is N-well under polysilicon.
MOSIS file ami-c5-t47f-params

+PDI BL C2 = 2.089469E-3    PDI BL CB = -0.0520065    DROUT = 1.0119898
+PSCBE1 = 6.395601E8    PSCBE2 = 2.051156E-4    PVAG = 0
+DELTA = 0.01    RSH = 83.6    MOBMOD = 1
+PRT = 0    UTE = -1.5    KT1 = -0.11
+KT1L = 0    KT2 = 0.022    UA1 = 4.31E-9
+UB1 = -7.61E-18    UC1 = -5.6E-11    AT = 3.3E4
+WL = 0    WLN = 1    WW = 0
+WWN = 1    L W = 0    LL = 0
+LWN = 1    LW = 0    LWN = 1
+LWL = 0    CAPMOD = 2    XPART = 0.5
+CGDO = 2.01E-10    CGSO = 2.01E-10    CGBO = 1E-9
+CJ = 4.255868E-4    PB = 0.926049    MJ = -0.11
+CI SW = 2.932172E-10    PBSW = 0.8    MJ SW = 0.1728427
+CI SW G = 1.64E-10    PBSWG = 0.8    MJ SW = 0.1728427
+CF = 0    PVT H0 = 0.0255986    PRD SW = 409.0242618
+PK2 = -0.02491

. MODEL CMOSP PMOS (                            LEVEL = 49
+VERSION = 3.1                            TOX = 1.4E-8
+XJ = 1.5E-7                           NCH = 1.7E17    VTH0 = -0.9324587
+K1 = 0.5418241                          K2 = 0.0121443    K3 = 9.1825002
+K3B = 1.0081807                          W0 = 1E-8    NLX = 6.166062E-9
+DVTOW = 0                               DVT1W = 0    DVT2W = 0
+DVT0 = 2.3587659                         DVT1 = 0.6843255    DVT2 = -0.1522404
+U0 = 211.1145904                        UA = 2.893983E-9    UB = 1.79181E-21
+UC = 6.0993E-11                         VSAT = 1.745955E5    A0 = 0.9399837
+AG5 = 0.1602973                         BD = 6.601323E-7    B1 = 7.465535E-7
+KETA = -4.320086E-3                     A1 = 8.373476E-5    A2 = 0.3
+RDSW = 3E3                              PRWG = -0.0147222    PRWB = -0.0192043
+WR = 1                                 WR NT = 2.795144E-7    LN T = 9.155405E-8
+XL = 1.1E-7                            XW = 0    DWG = -1.255072E-8
+DWB = 1.933603E-8                       VOFF = -0.0812374    NFACTOR = 0.6840911
+CI T = 0                               CDSC = 2.4E-4    CDSCD = 0
+DSUCB = 0                             ETA0 = 0.2845389    ETAB = -0.092965
+DSUB = 1                               PCLM = 2.1560106    PDI BL C1 = 0.0404233
+PDI BL C2 = 3.452595E-3                 PDI BL CB = -0.0527157    DROUT = 0.2131398
+PSCBE1 = 5.323834E9                      PSCBE2 = 5E-10    PVAG = 0.0149825
+DELTA = 0.01                           RSH = 104.8    MOBMOD = 1
+PRT = 0                                 UTE = -1.5    KT1 = -0.11
+KT1L = 0                                KT2 = 0.022    UA1 = 4.31E-9
+UB1 = -7.61E-18                         UC1 = -5.6E-11    AT = 3.3E4
+WL = 0                                  WLN = 1    WW = 0
+WWN = 1                                 WWL = 0    LL = 0
+LWN = 1                                 LW = 0    LWN = 1
+LWL = 0                                 CAPMOD = 2    XPART = 0.5
+CGDO = 2.61E-10                         CGSO = 2.61E-10    CGBO = 1E-9
+CJ = 7.286969E-4                        PB = 0.9555601    MJ = 0.4953105
+CI SW = 2.665117E-10                    PBSW = 0.99    MJ SW = 0.2906618
+CI SW G = 6.4E-11                       PBSWG = 0.99    MJ SW = 0.2906618
+CF = 0                                 PVT H0 = 5.98016E-3    PRD SW = 14.8598424
+PK2 = 3.73981E-3                        WKET A = 4.223292E-3    LKET A = -5.28673E-3 )