EE 434 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _
Exam 2
Fall 2005

Instructions. Students may bring 4 pages of notes to this exam. There are 10 questions and 5 problems. The questions are worth 2 points each and the problems are all worth 16 points. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$,$\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF}=\infty$. If any other process parameters are needed, specify clearly what process parameters are give typical values for those parameters.

1. What is the dc equivalent circuit of a large capacitor with an initial voltage of 5V?

2. How does the dynamic power dissipation of dynamic logic compare to that of static CMOS logic?

3. A minimum-sized BJT is typically much larger than a minimum-sized MOSFET if comparable processing equipment is used. What process step in the bipolar process is the major contributor to this much larger size?

4. True or False - The dynamic power dissipation of a pad driver designed to drive a 10pF load is significantly less than that required to drive the 10pF load directly with a minimum-sized inverter.

5. How does the total propagation delay ($T_{HL}+T_{LH}$) for an inverter sized for equal rise and fall times (with minimum-sized n-channel devices) compare to that of an inverter with minimum-sized devices?

6. The inverter pair was used to determine V_H and V_L for a logic family. The inverter pair with feedback from the output to the input is also a very useful circuit. What function does this circuit perform?

7. NMOS logic offers several significant advantages over Static CMOS but has one major shortcoming that has limited the extensive use of NMOS logic in todays state of the art circuits. What is this shortcoming?

8. What power is required to take a 1GHz clock signal off-chip if it is driving a 1pF load with V_H=5V and V_L=0V?

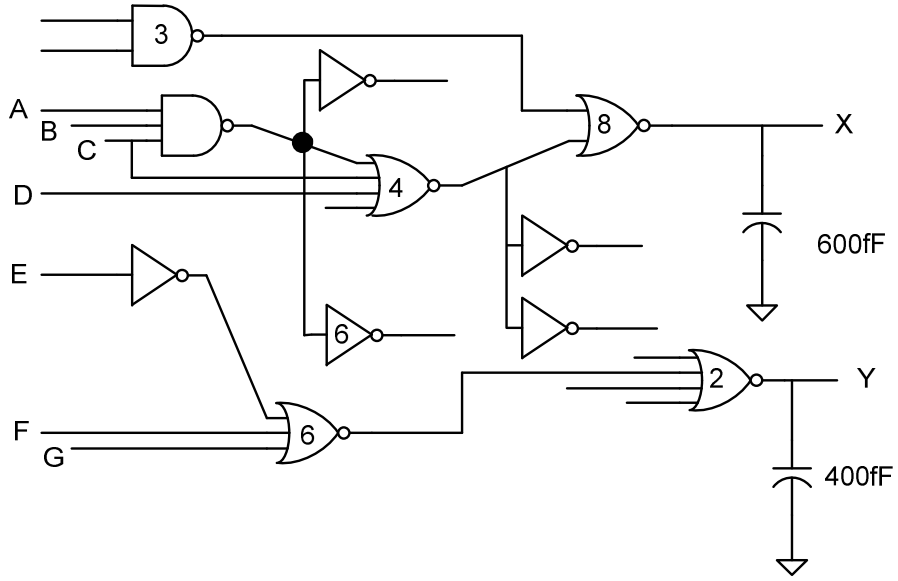
9. There are two major concerns that limit the applications of Pass Transistor Logic. What are they?

10. Digital logic benefits significantly from scaling of the lateral feature sizes. What increase in density (gates/unit area) can be expected as the process technology scales from 0.25μ to 0.05μ ?

Problem 1 A logic circuit designed in conventional static CMOS is shown. Assume all gates are sized for equal worst-case rise and fall times, that the input capacitance of an equal rise/equal fall reference inverter is 2fF, and that it has a propagation delay (T_{HL} + T_{LH}) of 20psec. The overdrive factor, if different than 1, is indicated by the number on the gate symbol.

a) Determine the propagation delay (T_{HL} + T_{LH}) from the A input to the X output

b) Repeat part a) if the four-input NOR gate in the signal path from A to X is comprised entirely of minimum sized devices.

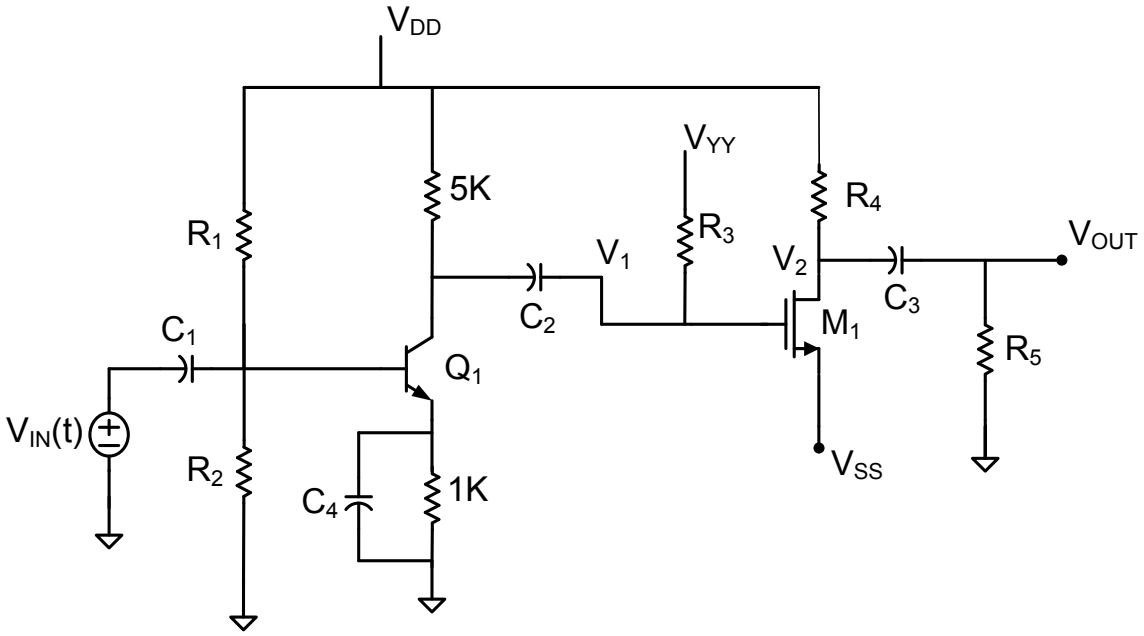


Problem 2 Assume all capacitors in the amplifier shown are very large, that Q_1 has an emitter area of $200\mu^2$ and that M_1 has W=10μ and L=2μ. (The process parameters were given on page 1 of this exam).

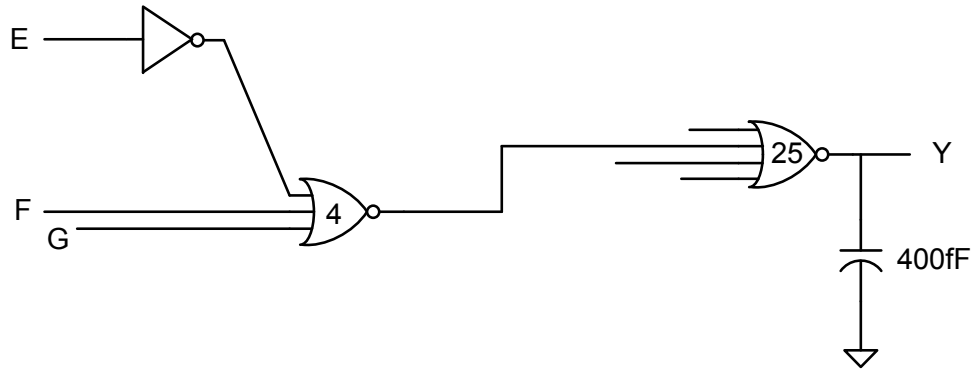
a) Draw the small-signal equivalent circuit for the amplifier shown below

b) Draw the dc-equivalent circuit used for biasing of the amplifier shown

c) Determine the quiescent values of V_2 and V_{OUT} if V_{DD}=10V, V_{YY}=1V, V_{SS}=-1V, R_4=10KΩ and R_5=40KΩ.



Problem 3 Determine the dynamic power dissipation in the 3-input NOR gate and the four-input NOR gate if input signals on E, F and G are supplied to force a 100MHz square wave on the Y output and the unspecified inputs on the 4-input NOR gate are all high. The devices are sized for equal rise/fall times and the overdrive factors, if different than 1, are indicated on the gate symbols. Assume the supply voltage is 5V and that the minimum-sized transistor in this process has Lmin=0.6μ and Wmin=0.9μ.



Problem 4 Implement $F = \left(\overline{\left(\overline{A} \bullet B\right) + C}\right)$ in the logic styles indicated. Draw schematics to the transistor level but do not size the devices. No layout is needed. Assume both the input variables and their complements are available.

a) Standard static CMOS logic
b) Complex logic gates
c) Pass Transistor Logic
d) Zipper logic.

Problem 5 Assume you were giving directions to a part of your design team that resides in another continent about the sizing strategy and that you indicated that to achieve equal rise and fall times in a reference inverter you need to size the devices so that Wn=Wmin, Wp=3Wmin, Ln=Lmin and Lp=Lmin. Because of communication problems, the engineers on the other continent understood your directions to be that Wn=Wp=Wmin, Ln=Lmin and Lp=3Lmin. Assume in this process Lmin=0.6μ and Wmin=0.9μ. Compare quantitatively t_{HL} and t_{LH} that you expected to achieve with the t_{HL} and t_{HL} that will actually be achieved because of the communication error if the reference inverter is driving an identical device.