EE 434 Name _____
Final Exam
Fall 2001

Instructions: This is an open-book, open-notes exam. If references semiconductor processes are needed, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=100\mu A/v^2$ ,$\mu_p C_{OX}=30\mu A/v^2$ ,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$, Cbdbot = $0.5fF/\mu^2$ , and Cbdsw = $2.5fF/\mu$. and all npn bipolar transistors are characterized by the parameters $\beta =100$, $V_{AF}=4$, and $J_S= 3E\text{-}19A/\mu^2$. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Problem ____ Answer the following questions:

a) What is the approximate cost of adding one additional MOS transistor to an integrated circuit in a CMOS process with a minimum feature size of 0.5u ? Be quantitative.

b) There is one parameter of an n-channel transistor that is much "better" than the same parameter for the p-channel transistor. This parameter characterizes the major reason why the n-channel transistor offers better performance than the p-channel transistor in circuits using these devices. What is this parameter and how much better is it?

c) When building MOS amplifiers, the MOS transistor is usually operated in the saturation region. Why do we usually use this region of operation when building amplifiers?

d) Why is it easier to achieve a higher voltage gain with a BJT than with a MOS transistor?

e) What is the name of the layer that is grown in a bipolar process to form the collector region of the vertical npn transistor?

f) Why can't two discrete diodes connected as shown be used to form a practical pnp transistor?

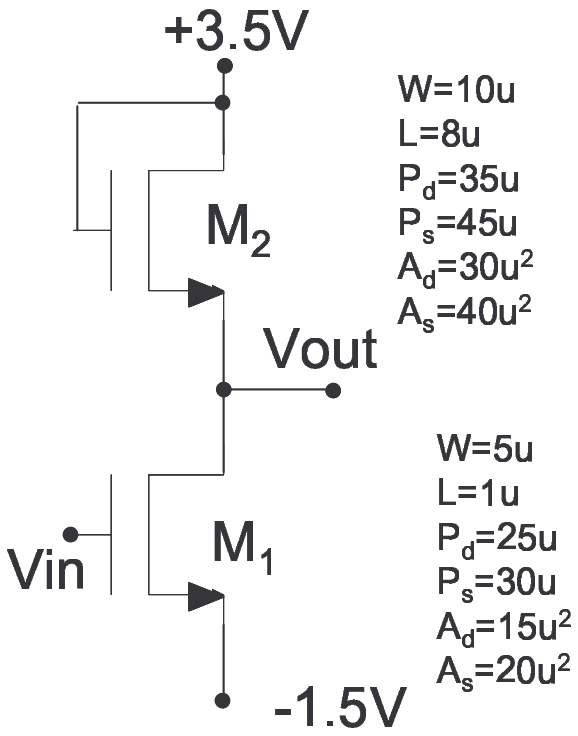

g) How does the area required for fabricating a minimum-sized BJT compare to that required for fabricating a minimum-sized MOSFET in state of the art semiconductor processes? Be quantitative.

h) Pass Transistor Logic often requires considerable less transistors than conventional static CMOS for implementing many logic functions but it is either not practical or not possible to use PTL for some functions that require a large number of inputs. One example where this is apparent is a multiple-input AND gate. Why is a 5-input PTL AND gate not practical?

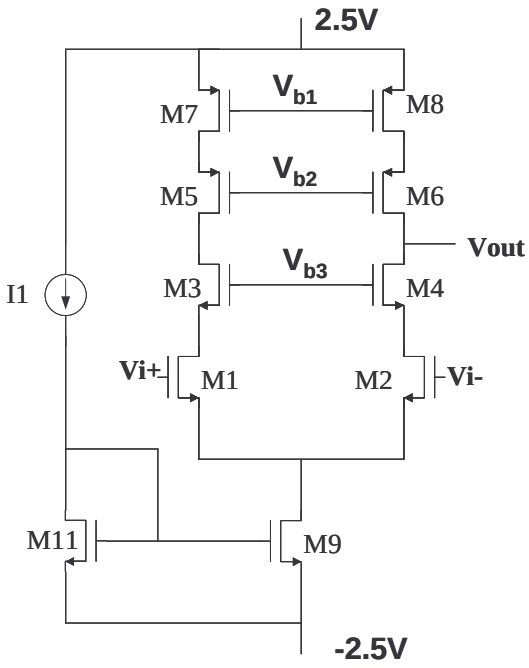
i) Explain the likenesses and differences between an n-doped epitaxial layer, an n-doped drain diffusion and an n-doped polysilicon layer

j) In our VLSI-CAD environment there are several tools from several vendors that must be integrated. Two of these tools are what we call Synopsis and Silicon Ensemble. That is the purpose of these two tools and how are they supposed to interact?

Problem ____ For the amplifier shown, determine the dc gain, the high-frequency small-signal model, and the 3dB bandwidth.



Problem _____ For the amplifier shown, obtain the dc gain, the dc power dissipation and the bias current in M7. Assume Vb1 has been selected to that VoutQ = 0.5V and that the voltages Vb2 and Vb3 have been selected so all devices are operating in the saturation region. In this circuit, I1=200uA, all lengths are 2u, W11=40u, W9=120u,W1=W2=48u,W3=W4=W5=W6=100u,W7=W8=100u. When solving this problem, assume the process is as characterized at the top of this exam except that $\lambda = 0.01V^{-1}$.



Problem _____ Design an amplifier in a CMOS process that has a dc voltage gain of –6 (+/- 10%). You have available any number of MOS transistors, any number of dc voltage sources and any number of dc current sources. Include an analysis of your circuit that shows you meet the gain requirement.